Reflection Coefficient Shaping of a 5-GHz Voltage-Tuned Oscillator for Improved Tuning

Alan Victor, *Senior Member, IEEE*, and Michael B. Steer, *Fellow, IEEE*

***Abstract*—Negative resistance voltage-controlled oscillators (VCOs) are systematically designed to operate with loaded resonator networks that permit stable steady-state oscillation over a specified tuning bandwidth. Circuit parasitics, however, significantly affect tuning behavior and complicate straightforward design. This paper introduces a scheme that compensates for the effect of parasitics by introducing an embedding network that modifies the effective active device reflection coefficient and thus enables conventional one-port oscillator design techniques to be used. A common-base SiGe HBT VCO operating from 4.4 to 5.5 GHz demonstrates the technique. Phase noise is better than −85 dBc/Hz at 10-kHz offset from the carrier and the second harmonic is less than −20 dBc, while higher order harmonics are less than −40 dBc. The voltage-tuned oscillator demonstrates an oscillator figure-of-merit of at least −182 dBc/Hz over a 800-MHz tuning range. The phase-noise-bandwidth (in megahertz) product is −159 dBc/Hz.**

***Index Terms*—Negative resistance, oscillator, resonator, varactor tuning, voltage-controlled oscillator (VCO).**

I. Introduction

DESIGN OF stable negative resistance oscillators traditionally uses the one-port oscillator stability requirement outlined by Kurokawa [1]. In applying the criterion, each of the networks—the active device, resonator load, and device termination—are characterized as one-ports. When a device with admittance $G_d - jB_d$ is connected to a loaded resonator of admittance $G + jB$, the voltage amplitude A and frequency ω of the resulting equilibrium oscillation are determined when $-G_d(A) = G(\omega)$ and $B_d(A) = B(\omega)$. In this procedure, the assumption is that the device admittance at a single frequency is a strong function of voltage amplitude while the resonator admittance is a function only of angular frequency. This condition can be represented graphically by first denoting the locus of the negative of the device's complex admittance as $-Y_d(A) = -[G_d(A) - jB_d(A)]$ (also referred to as the inverse device reflection coefficient or $1/S$ locus) and the locus of the resonator admittance as $Y(\omega) = G(\omega) + jB(\omega)$. For stable single-frequency oscillation, the intersection of these loci in the complex plane then occurs at a single point. Multiple intersections and inappropriate angular intersection of these loci are directly related to several key performance-limiting parameters including spurious or multiple oscillations, oscillator startup problems, and excess noise [2]. In a tunable oscillator designed to cover a large tuning range, the device admittance is also frequency dependent. Therefore, the device admittance is more accurately described as $-G_d(A, \omega)$.

Resonator design requires that the Q be maximized while achieving the desired admittance change with tuning voltage. Furthermore, for a voltage-controlled oscillator (VCO), voltage tuning of the resonator must satisfy the specific stability criteria, including single point of intersection and appropriate angle of intersection, over the tuning range. With emphasis on these characteristics and the presence of parasitic elements, achieving a proper stable resonator–device interface is troublesome. An alternative and equally viable approach to stability analysis of a broad class of oscillators, particularly for those using three-terminal devices, is application of the two-port criteria developed for amplifier stability assessment. However, the one-port approach is preferred by designers because the one-port connection is closer to the intended operation. The one-port wave assessment of oscillator stability is not unlike the Bode criteria applied to two-port feedback systems [3], [4]. However, unlike the two-port open-loop assessment of stability, the one-port characterization technique is conveniently aligned with measurements made by a vector network analyzer (VNA) [5], [6]. As well, the nonlinear limiting effect of the active device is readily measured.

In the oscillator design approach presented in this paper, the design objective is the generation of a frequency-dependent negative conductance $G_d(A, \omega)$ with a prescribed reflection coefficient shape Γ_d using a three-terminal active device in a common-base (series-inductive feedback) configuration. Reactive loading modifies the effective device conductance so that it becomes frequency dependent. Modifications can be incorporated in the resonator load, but then it is seen that the frequency-dependent behavior of the tank circuit is inappropriate, resulting in multiple oscillations and other instabilities. In addition, the resonator Q is compromised. Another issue is that small-signal S-parameters are generally good indicators of oscillator operation, particularly for the frequency of oscillation [7]; however, they do not provide sufficient information to determine if stable oscillation will occur. This paper introduces circuit modifications that facilitate design for correct operation of the active device–resonator combination. The technique uses measured reflection coefficients, and compensates for the effect of parasitics at the interface between the active device and resonator. In Section II, series feedback oscillators are discussed and the design criterion for oscillator startup $|G_d(A, \omega)| > G(\omega)$ is presented in terms of the device

Manuscript received April 23, 2007; revised August 13, 2007.

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Digital Object Identifier 10.1109/TMTT.2007.909140

complex reflection coefficient. Section III presents and demonstrates a device-mapping technique to modify the active device characteristic. The mapping is achieved using a combination of additional capacitive reactive loading at the emitter–base terminals and at the collector. The net result is an effective active device characteristic that is largely a function of signal amplitude, while the frequency-dependent characteristics are properly modified. These modifications consider the resonator plus parasitic elements at the device interface. As such, a conventional approach to oscillator design can be used. Section IV then documents the performance of a VCO designed using the technique presented here. It is seen that the required device mapping is achieved over the frequency range of the VCO.

II. Series Feedback Oscillators

A negative resistance oscillator is normally realized using a series capacitor in the emitter, and a negative conductance oscillator is realized using a series inductor in the base lead. Both oscillator types use feedback to obtain a negative real component. In [8], the value of series feedback reactance required is found in terms of device impedances and, in general, this can be extended for all passive terminations and applied to any terminal of the active device. An interesting observation for both configurations is that the resulting reflection coefficient is optimum over a restricted region of the Smith chart. Here, optimum is in the sense that the resulting real part of the resonator series resistance (or shunt conductance) for a series-tuned (or shunt-tuned) resonator is minimized (maximized) to meet the criteria for oscillator startup. This criteria simply stated is that $|G_d(A,\omega)| > G(\omega)$ or $|R_d(A,\omega)| > R(\omega)$. Compliance with these requirements requires that the complex reflection coefficient of the active device Γ_d be greater than unity. Furthermore, there is a specific angular range of active device reflection coefficient that is found to assist in providing these conditions. However, it is not sufficient to simply have large values of $|\Gamma|$. The reflection coefficient angle must be constrained to minimize the losses associated with the resonator, at least to assure oscillator startup. Thus, a specific angular range of active device reflection coefficients is found to provide these conditions. Fig. 1 plots the equivalent parallel resistance R_p of the resonator as a function of the reflection coefficient angle $\angle\Gamma$ for several values of $|\Gamma|$. Also shown in Fig. 1 is the equivalent oscillator Q expressed as $|B_d/G_d|$ for $|\Gamma| = 2$. Returning to the R_p curves, it is seen that the point where families of Γ values converge for a reasonable range of device $\angle\Gamma$ is approximately 140°. Angles of the reflection coefficient which are less would require resonators with higher unloaded Q, Q_{UL}, in order to satisfy oscillator starting conditions. If a large tuning range is required, then reflection coefficient angles greater than 100° are desired. Thus, it is clear that the design of the tank circuit (or resonator) and the active device interface is a methodical process to provide appropriate admittance (or impedance) variation over the tuning bandwidth of the VCO. It is not possible, therefore, to simply embed parasitics in the tank circuit and design an oscillator with the required attributes.

The common base configuration used here is shown in Fig. 2. The resonator, to the left of $(x$–$x)$ in Fig. 2, uses a tapped transmission line to improve the loaded Q and series

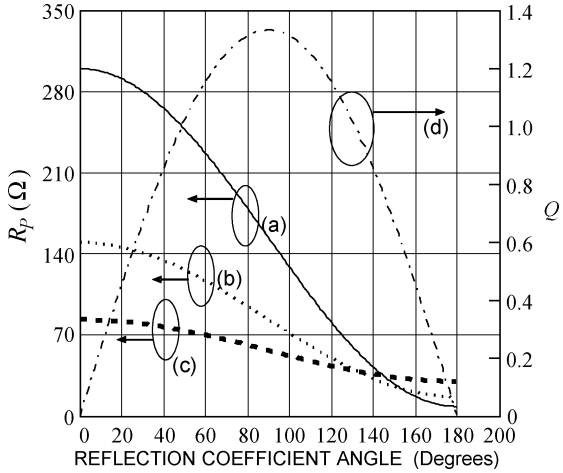

Fig. 1. Resistance R_p of a parallel (or shunt-tuned) resonator required to satisfy the condition of oscillation for: (a) $|\Gamma| = 1.4$, (b) $|\Gamma| = 2$, and (c) $|\Gamma| = 4$ versus the reflection coefficient angle $\angle\Gamma$. Curve (d) is the oscillator equivalent Q for $|\Gamma| = 2$.

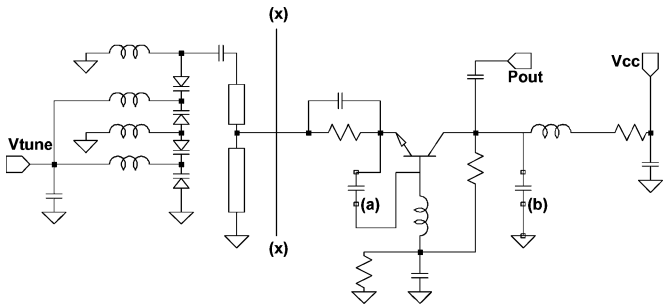

Fig. 2. Common base oscillator configuration. Capacitors at (a) and (b) are modifications of the network compensating for parasitic inductances.

back-to-back varactors to increase the ac breakdown voltage [9] and the unloaded Q. The series feedback inductance, to the right of the $(x$–$x)$ interface, includes device mounting pads, printed board traces, and film inductors. The capacitors at (a) and (b) in Fig. 2 are auxiliary compensating capacitors whose selection and function will now be described.

The values of the capacitors at (a) and (b) are derived using an iterative approach that involves finding the complex load required to obtain the necessary frequency and amplitude dependence of Γ_d, the reflection coefficient required of the device network presented at the $(x$–$x)$ cut. Referring to Fig. 2, the development begins by assigning $\hat{S}$ to be the S-parameter matrix of the active circuit to the right of the $(x$–$x)$ line. This S-parameter network comprises the small-signal parameters of the transistor modified by the addition of series feedback and normalized to 50-Ω source and load terminations. The network at this point does not include the effects of a complex load Γ_L, and does not include the capacitors at (a) and (b). The device input reflection looking to the right of the $(x$–$x)$ cut is then modified to $S'_{11} = \hat{S}_{11} + \hat{S}_{21}\hat{S}_{12}\Gamma_L/(1 - \hat{S}_{22}\Gamma_L)$. S'_{11} is similar to the reflection coefficient used in the oscillator design approach of Gonzales and Sosa [8], except that the terminations are not restricted to 50 Ω. This enables the loci of S'_{11} to be conveniently plotted as the values of the capacitors at location (a) and (b) vary. The effects of the capacitors are incorporated in Γ_L and

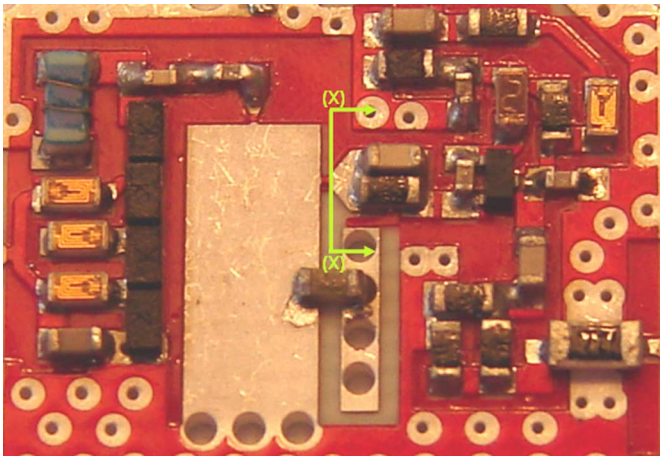

Fig. 3. Resonator, left of cutaway line (x–x), is separated from the active network to the right.

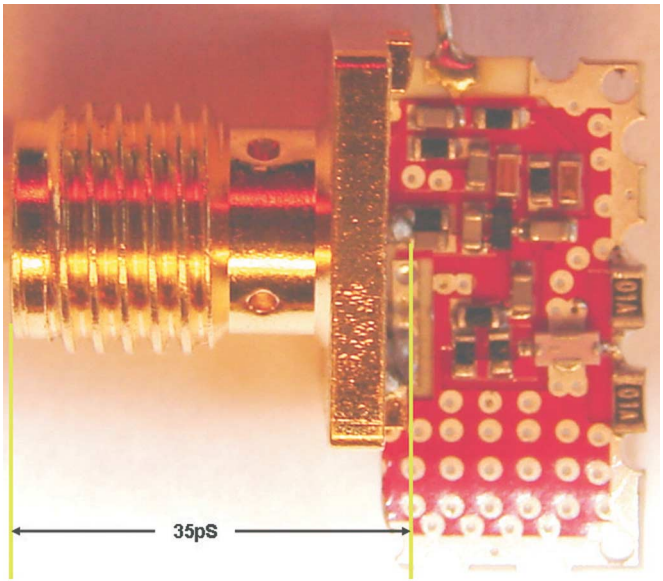

Fig. 4. Negative conductance network loaded with 50-Ω termination. Active device and series feedback are centered on the card. A 35-ps delay is required to reference measurement at the circuit card edge. Scale is 5 : 1.

the source termination. The reflection locus curve that has the proper dependence on amplitude and frequency sets the values of the capacitors and then S'_{11} becomes Γ_d, the device reflection coefficient with the required attributes.

As previously discussed, the oscillator design process uses Fig. 1 as a guide to selecting the required input reflection coefficient of the active circuit. The next step in design is using a VNA to measure the reflection coefficient of the active device network to the right of (x–x) in Figs. 2 and 3, shown again in its measurement configuration in Fig. 4. Measurement of the active device is through the tapered tap line and includes the emitter return resistor and bypass capacitor. Here it is imperative that the correct reference plane be established. Use of short-open-load (SOL) calibration permits the reference plane to be set correctly for a 3.5-mm subminiature A (SMA) connector. The connector center pin is located right of the center cut line (x–x), as shown in Fig. 3, requiring that 35 ps of additional delay be incorporated

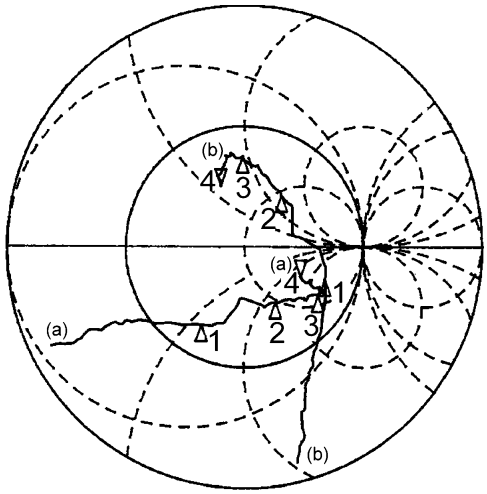

Fig. 5. Small-signal $1/S$ measurement of the active device on a compressed Smith chart. (a) Proper calibration and delay. (b) Delay not applied. Marker 1: $133 - j155\ \Omega$ (uncalibrated) at 3.8 GHz, marker 2: $55.2 + j64.9\ \Omega$ at 4.4 GHz, marker 3: $14.1 + j47.1\ \Omega$ at 4.8 GHz, marker 4: $20.95 + j29.8$ at 5.4 GHz.

in calibration. This delay accounts for the offset location of the SMA open and the length of the connector center pin. The small value of corrective delay is significant, as it represents a major shift in the reflection coefficient phase required of the resonator. The resulting inverse reflection coefficient or $1/S$ active device locus is curve (a) in Fig. 5. From this curve, it is seen that the required resonator load is capacitive.

The resonator or tank circuit is shown to the left of the (x–x) line in the oscillator schematic of Figs. 2 and 3. Measurement of the tank circuit, using a similar procedure to that described above for the active device, yielded the resonator locus shown in Fig. 6. Again, SOL calibration and correct delay adjustment is required. The resonator locus is seen to have significant parasitic series inductance, which is attributed to the varactor interconnection PC traces, as well as the pads. It is this parasitic that prevents straightforward VCO design.

Design of course proceeds by matching the characteristics of the active device (see Fig. 5) and that of the tank circuit (see Fig. 6). First, the small-signal device $1/S$ should provide $|\Gamma_{\rm d}(A,\omega)| < |\Gamma(\omega)|$ of the resonator for all tuned frequencies. Second, the rotation of $B(\omega)$ should be positive and in the opposite direction of the $\Gamma_{\rm d}(A,\omega)$ locus. As device self-limiting occurs with an increase in the drive signal to the active device, the argument of $\Gamma_{\rm d}(A,\omega)$ and $\Gamma(\omega)$ should sum to 0°. This should be unique for each tuning voltage and, thus, oscillation frequency. Finally, the trajectory of the limiting $\Gamma_{\rm d}(A,\omega)$ locus should intersect $\Gamma(\omega)$ at right angles to minimize phase noise [1], [6]. In this study, these requirements are referred to as a "complement" relationship between the active device and the resonator reflection coefficient locus.

Inspection of curve (a) in Fig. 5 and the resonator locus in Fig. 6 illustrates the problem in achieving the single-frequency stable oscillation condition at all tuning voltages, i.e., as limiting occurs, the trajectory of the negative conductance of the device intersects the resonator locus at multiple points, particularly around 5 GHz (marker points 3 and 4 on curve (a) in Fig. 5).

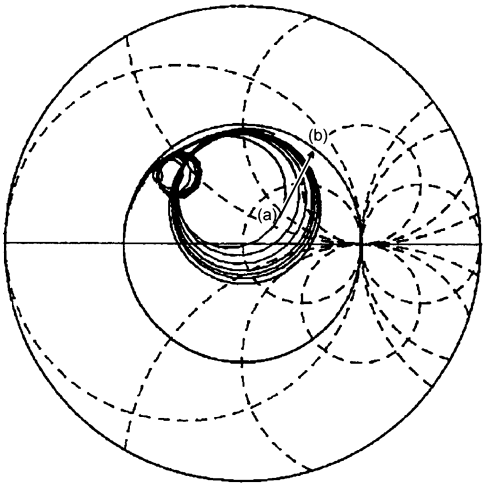

Fig. 6. Resonator locus on a compressed Smith chart showing that the resonator is dominantly inductive over the voltage tuning range. Varactor voltage increases in the direction of the arrow with increasing frequency marked: (a) from 4.5 GHz to (b) 5.3 GHz.

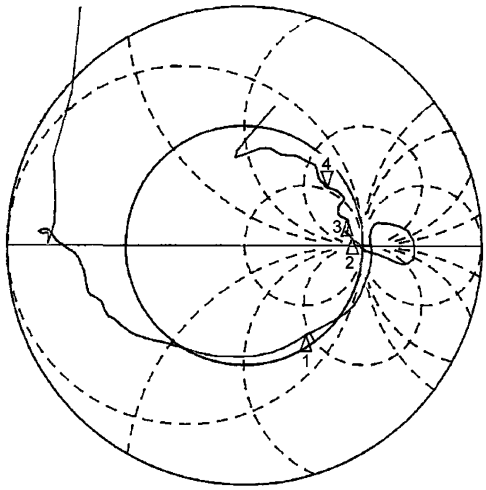

Fig. 7. Modified active device reciprocal reflection $1/S$ curve, which rotates counterclockwise as the device limits. The incident power measurement is at $+10$ dBm. Marker 1: $10.5 - j95.3\ \Omega$ at 3.5 GHz, marker 2: $679 + j535\ \Omega$ at 4.5 GHz, marker 3: $157 + j335\ \Omega$ at 4.8 GHz, and marker 4: $42.6 + j148.5$ at 5.3 GHz.

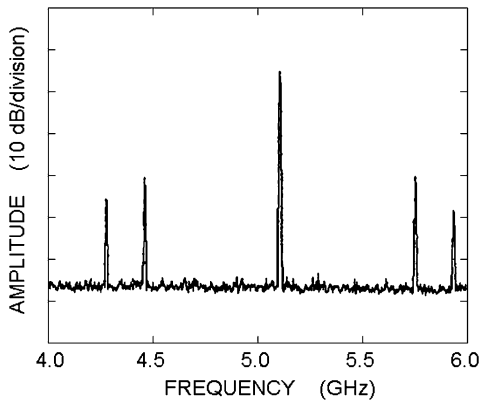

Fig. 8. Multioscillation at 5.1 GHz prior to reflection coefficient shaping. Resolution BW: 3 MHz, video BW: 1 MHz, ref: 10 dBm, ATT: 20 dB.

These conditions lead to multioscillation. A technique for addressing this problem is presented in Section III.

III. Reflection Coefficient Shaping

A technique for modifying the active device network that enables straightforward design of a single-frequency stable wideband VCO is presented here. Previously it was pointed out that the input reflection coefficient of the active device network can be represented as a mapping of $1/S$ of the active device as a function of collector termination. Next, additional device modification is used to modify the map. The input termination is next added to the device. The objective here then is to find the appropriate terminations at the collector and emitter terminals of the active device for a given series feedback impedance. The corresponding $-G_d(A)$ that results must yield a locus $-G_d(A)$ versus frequency, i.e., $-G_d(A, \omega_{\rm tune})$, which provides the proper interface to the resonator. If possible, the network modification should position the reflection coefficient of the modified active device in the region of the chart in Fig. 1 above 100°. The trajectory of the negative conductance as device limiting occurs and where $1/S$ just intersects the unit circle must complement the argument of the resonator. This is the situation shown in Fig. 7 where the new modified device characteristic was achieved by adding capacitive terminations to the collector and the emitter–base terminals. Here, unlike the conventional common base series feedback oscillator situation, the input of the active device network is now capacitive (see Fig. 7). Consequently, a portion of the parasitic inductance of the resonator is successfully absorbed. Thus, the small-signal $1/S$ one-port reflection coefficient is initially inductive.

Normally, with a common-base oscillator, limiting at increasing power levels results in the device's $1/S$ locus moving along lines of constant susceptance as the negative conductance of the active device decreases. Instead, with the modified network here, there is a counterclockwise rotation of the active network's inverse reflection coefficient as limiting occurs.

The discussion can now return to the oscillation condition as determined by matching the resonator locus in Fig. 6 to the modified active device characteristic shown in Fig. 7. Oscillation occurs when a point on the resonator locus in Fig. 6 corresponds to the point of the same frequency on the modified-device locus in Fig. 7. Under small-signal conditions, the loci may not coincide, but the important point is that they do when limiting occurs, as well as providing for the startup of oscillation. The counterclockwise rotation of the modified active device locus, as described above, assures stable single-frequency oscillation. In particular, oscillation over the frequency range from 4.5 to 5.3 GHz follows the trajectory from Point (a) to Point (b) in Fig. 6. Multioscillation, as demonstrated in Fig. 8, is suppressed in this technique. Note that in effect the resonator is operated as a shunt tunable inductance, as opposed to a tunable capacitive reactance. Here is a case where the use of two-port small-signal S-parameters to manage the resonator design would not be appropriate providing little useful design insight.

IV. Oscillator Performance

The oscillator design procedure outlined above was followed in implementing a VCO operating from 4.5 to 5.5 GHz using an SiGe HBT. The oscillator schematic is shown in Fig. 2 and

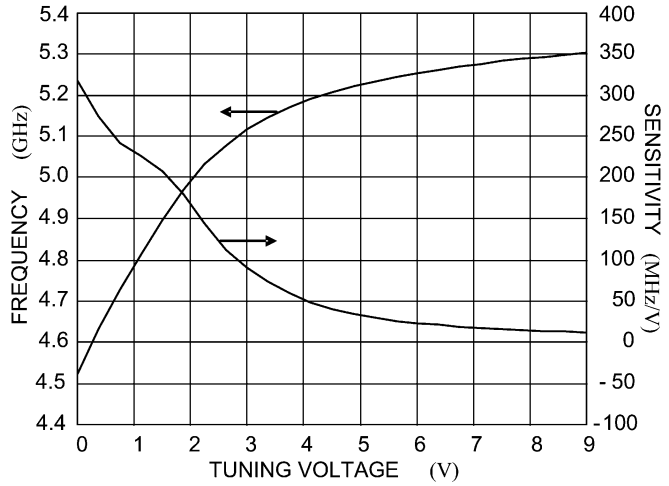

Fig. 9. Tuning curve showing oscillation frequency and VCO sensitivity as a function of tuning voltage.

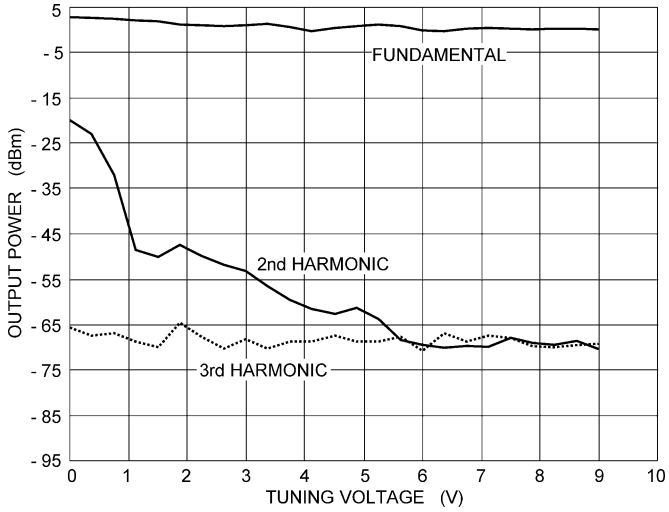

Fig. 10. Output power and harmonics, demonstrating low-level harmonic content.

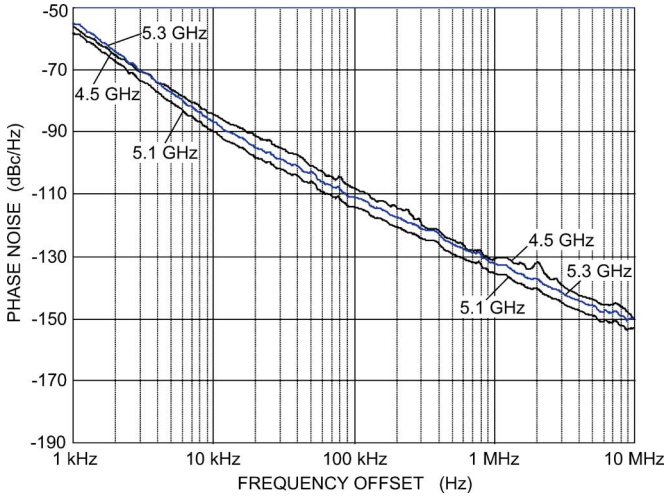

Fig. 11. Phase noise measured at the top and bottom of the tuning range, as well as at 5.1 GHz where phase noise is optimum. Minimum phase noise floor −116 dBc/Hz at 1-kHz offset, −160 dBc/Hz at 10-MHz offset.

includes the active device modified by additional capacitors (a) and (b). Device characterization and circuit operation was at 5 V and 30-mA bias current. In characterizing the oscillator, the varactor tuning voltage was verified against the desired frequency range by comparing the resonator locus with the $1/S$ sweep of the active device. Open-loop one-port measurements were done with +10 dBm of incident power. The resonator tuning characteristics are trimmed against those of the active device. This ultimately sets the oscillator tuning gain K_o. Additional tuning gain adjustment is controlled by the coupling between the varactor stack and the microstrip line. Average tune gain is 120 MHz/V. The tuning performance of the oscillator is shown in Fig. 9. The tune characteristic is monotonic with no jumps or discontinuities in the tuning curve as the oscillator was tuned over the full voltage tuning range. Fig. 10 presents the fundamental output power and harmonics. The fundamental output varies by less than 2 dB over the full tuning range and the harmonic levels are relatively low.

The measured phase noise is shown in Fig. 11 at the ends of the tuning range, i.e., 4.5 GHz (corresponding to a tuning voltage of 0 V) and 5.3 GHz (a tuning voltage of 9 V), as well as at 5.1 GHz where the best phase noise was obtained. Phase noise was measured using a Rohde & Schwarz FSUP26 signal source analyzer and a test set loop bandwidth of 5 kHz. The phase noise is approximately the same across the tuning range with a $1/f$ noise corner frequency of 30 kHz. The phase noise at 10-kHz offset, $\mathrm{L}(f_m)$ (10 kHz), is better than −85 dBc/Hz, while at 1 MHz $\mathrm{L}(f_m)$ (1 MHz), is better than −130 dBc/Hz. The best measured phase noise near band center (5.1 GHz) is −135 dBc/Hz.

Comparison of different oscillators requires that phase-noise measurements be normalized to the same offset frequency, which can be done assuming a $1/f_m^2$ shape of the phase noise where f_m is the offset frequency so that

$$\mathrm{L}(f_m)(1\ \mathrm{MHz}) = \mathrm{L}(f_m)(f_m) - 10\log\left(\frac{1\ \mathrm{MHz}}{f_m}\right)^2. \quad (1)$$

Another commonly used quantitative assessment of oscillator performance is provided by the oscillator figure-of-merit (FOM), which accounts for dc power consumed [10] as follows:

$$\mathrm{FOM}_1 = \mathrm{L}(f_m) + 10\log\left(\frac{f_m}{f_0}\right)^2 + 10\log\left(\frac{P_{\mathrm{DC}}}{P_{\mathrm{ref}}}\right) \quad (2)$$

where P_{ref} is conventionally taken as 1 mW. For Si monolithic VCOs, it is conventional to use just the power drawn by the VCO core, while for other technologies, including hybrid VCOs, it is not possible to separate out a VCO core. While FOM_1 also does not include weightings for tuning bandwidth and RF output power, it serves as a useful metric to compare like VCOs. Another FOM providing bandwidth weighting is

$$\mathrm{FOM}_2 = \mathrm{L}(f_m) + 10\log\left(\frac{f_m}{f_0}\right)^2 - 10\log\left(\frac{f_{\mathrm{BW}}}{f_{\mathrm{ref}}}\right) \quad (3)$$

where f_{BW} is the tuning bandwidth and f_{ref} is the reference bandwidth taken here as 1 MHz. A number of tunable oscillators operating in the range 1–10 GHz are compared in

TABLE I
COMPARISON OF RF VCOs OPERATING AT POWER LEVELS GREATER THAN −10 dBm (APPROXIMATELY). PHASE NOISE AND HARMONIC SUPPRESSION ARE WORST CASE, AND RF OUTPUT POWER IS MINIMUM, ACROSS THE TUNING RANGE. THE SYMBOL (C) INDICATES THAT CORE POWER ONLY (BUFFERS ARE ADDITIONAL). ALL OSCILLATORS ARE HYBRIDS, EXCEPT AS INDICATED

Center Freq. (GHz)	Tuning BW (MHz)	Output Power (dBm) P_{RF}	Minimum Harmonic Suppression (dB) 2nd	3rd	DC Power (mW) P_{DC}	Phase Noise @ Offset dBC@MHz	Ref. Phase Noise, 1 MHz, Eq. (1) (dBC/Hz)	FOM_1 Eq. (2) (dBC/Hz)	FOM_2 Eq. (3) (dBC/Hz)	Reference
4.92	770	0	20	66	150	−130 @ 1	−130	−182	−159	This Work, SiGe HBT, hybrid
5.05	500	0	47	66	150	−130 @ 1	−130	−182	−157	This Work, SiGe HBT, hybrid
5.16	229	−0.43	42	42	24(c)	−111 @ 1	−111	−172	−135	Myoung 2005 [11], InGaP/GaAs HBT
11.5	550	9	20	—	—	−91 @ 0.1	−111	—	−118	Lee 2000 [12], GaAs MESFET
9.33	440	3.3	47	—	30.5	−102 @ 1	−102	−156	−128	Cheng 2007 [13], GaN HEMT
6.40	150	5.5	—	—	173	−105 @ 0.1	−105	−186	−126	Zirath 2005 [14], SiGe HBT
5.94	166	−4.0	42	—	8.1	−110 @ 1	−110	−176	−132	Chu 2003 [15], monolithic CMOS
4.87	70	−4.0	—	—	4.8	−131 @ 1	−131	−198	−149	Meng 2006 [16], GaInP/GaAs HBT
5.38	120	−4.0	—	—	12.8	−127 @ 1	−127	−191	−148	Meng 2005 [17], GaInP/GaAs HBT
5.29	270	−5.5	—	—	14	−106 @ 1	−106	−169	−130	Hancock 2004 [18], SiGe HBT
2.17	385	11.2	—	—	1.9 (c)	−120 @ 0.6	−125	−189	−146	Yoon 2006 [19], 2005, monolithic CMOS
1.72	262	−11.5	—	—	75	−129 @ 1	−129	−175	−153	Yoon 2006 [20], InGaP/GaAs HBT
4.80	1200	4.8	—	—	36	−111 @ 1	−111	−169	−142	Esame 2007 [21], monolithic SiGe BiCMOS
9.35	2500	18.3	—	—	570	−110 @ 1	−110	−162	−144	Maas 2006 [22], GaN/SiC pHEMT
1.72	261	−10.25	—	—	55	−120 @ 1	−120	−167	−144	Yoon [23], InGaP/GaAs HBT
4.17	70	−6.1	—	—	102	−116 @ 1	−116	−161	−134	Meng [24], GaInP/GaAs HBT

Table I. Harmonic suppression is an important parameter with these oscillators, which are designed for direct generation of required RF power levels without subsequent buffering. For the VCO described in this paper, the conventional FOM, i.e., FOM_1, is equal to or better than −182 dBc/Hz. Averaged over the 800-MHz tuning range, 0–9 V, and phase noise at 10-kHz, 100-kHz, and 1-MHz carrier offsets, the average FOM_1 is −184 dBc/Hz. This is among the best reported metrics for VCOs operating between 1–10 GHz. With bandwidth weighting, captured by FOM_2, the oscillator reported here is the best reported for oscillators producing more than −10 dBm operating in the range of 1–10 GHz, as far as the authors are aware. The performance of oscillators in the 1–20-GHz range designed as on-chip oscillators was recently surveyed in [10].

V. CONCLUSION

The standard oscillator design procedure matches the inverse reflection coefficient $(1/S)$ of the active device to the reflection coefficient of a tank circuit. Design, however, is often complicated by resonator parasitics so that the effective negative admittance of the active device satisfies the condition of oscillation at multiple frequency points. The Kurokawa oscillator condition establishes that for stable oscillation at the operating point of a negative conductance oscillator that

$$\frac{\partial G_d}{\partial V_r}\frac{\partial B}{\partial \omega_r} - \frac{\partial B_d}{\partial V_r}\frac{\partial G}{\partial \omega_r} > 0 \tag{4}$$

where subscript r refers to the operating point. In the standard approach to oscillator design, the device susceptance is assumed to be independent of signal amplitude, i.e., $\partial B_d/\partial V_r = 0$, and the loaded resonator conductance to be independent of frequency, i.e., $\partial G/\partial \omega_r = 0$, so that the stability condition becomes the much simpler

$$\frac{\partial G_d}{\partial V_r}\frac{\partial B}{\partial \omega_r} > 0. \tag{5}$$

The focus of this paper was managing the third term of (4), $(\partial B_d/\partial V_r)$, while the fourth term $(\partial G/\partial \omega_r)$ was addressed by proper design of the resonator.

This paper has introduced reactive compensation elements at the device–resonator interface that resulted in the reflection coefficient of the augmented active device having the necessary frequency dependence to compensate for the nonideal resonator characteristic. That is the technique that results in both the effective negative resistance (conductance) and susceptance of the device properly complementing the frequency-dependent admittance of the resonator including parasitics. Equally important is that the standard one-port approach to stable oscillator design can be used. The topology developed is suited to realizing stable spurious-free wideband VCOs using three-terminal devices in a common-base configuration. However, the general concept of an introduced augmentation network should be applicable to the broad class of oscillators using three-terminal active devices. The design of a 4.5–5.3-GHz voltage-tunable oscillator was presented as an example. The conventional FOM of the VCO considered is −182 dBc/Hz. Furthermore, the VCO produces a minimum output power of 0 dBm and has good harmonic suppression exceeding 20 dB over an 800-MHz bandwidth and exceeding 47 dB over a 500 MHz bandwidth.

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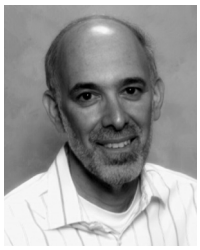

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