A Stackable Silicon Interposer with Integrated Through-Wafer Inductors

J. Carlson, M. Lueck, C. A. Bower, and D. Temple
RTI International, Research Triangle Park, NC 27709
Z. –P Feng and M.B. Steer
North Carolina State University, Raleigh, NC 27695
A.J. Moll and W.B. Knowlton
Boise State University, Boise, ID
temple@rti.org, 919-248-1945

Abstract

Three-dimensional (3-D) device stacking technologies provide an effective path to the miniaturization of electronic systems. These 3-D stacks can be envisioned to contain, in addition to active device layers, interposers with passive devices. The stackable interposer concept is compatible with any integratable passive device architecture, but is particularly well suited to 3-D enabled passives which take advantage of the bulk of the layer and the connectivity on two surfaces. In this paper we report on the design, fabrication and electrical characteristics of a 3-D enabled solenoidal inductor.

Introduction

High performance commercial and military applications demand more and more complex, multifunctional microsystems with performance characteristics which can only be achieved by using best-of-breed materials and device technologies for the microsystem components. Three-dimensional (3-D) integration of separate, individually complete device layers provides a way to build complex microsystems without compromising the system performance and fabrication yield. In the 3-D integration approach, each device layer is fabricated separately using optimized materials and processes. The layers are stacked and interconnected by means of area array through-wafer interconnects (TWIs) [1,2]. These 3-D stacks, shown schematically in Figure 1, can be envisioned to contain, in addition to the active device layers, interposers with passive devices, such as inductors, resistors and capacitors. The placement of passives in the separate interposer layer preserves costly real estate of ICs and decouples the process of the fabrication of the passives from the thermal budget of a completed IC. It also facilitates known-good-die processing for increased yield.

As shown in Figure 1, the interposer may contain 2-D passives, but its use also opens the doors to a device architecture which takes advantage of the bulk of the layer and connectivity on both surfaces. This device architecture is enabled by the use of through-wafer interconnects shown in Figure 1.

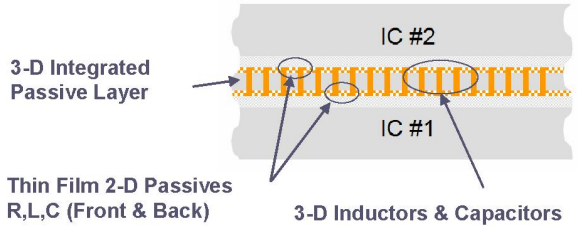

Figure 1. Schematic of a stackable interposer containing both 2-D and 3-D passives.

This paper focuses on an example of a 3-D enabled passive device, a 3-D solenoidal inductor, following an earlier report on TWI-enabled inductors [3]. Traditional thin-film inductors have a 2-D, surface-style architecture, illustrated schematically in Figure 2. Surface inductors fabricated on low resistivity silicon common for RFICs have Q's typically of less than 10 at frequencies up to 5 GHz and inductance values of 1 to 10nH [4,5].

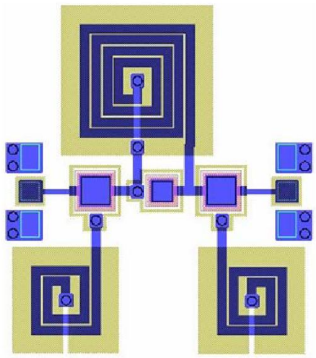

Figure 2. Circuit with surface 2-D Inductors.

Figure 3 shows a schematic of a 3-D solenoidal inductor with windings composed of TWIs and routing lines on both surfaces of the substrate. The 3-D fabrication approach allows for potentially better performance characteristics, coupled with better field control and with connection opportunities on both sides of the die. One important aspect is the definitive provision of multiple current-return paths.

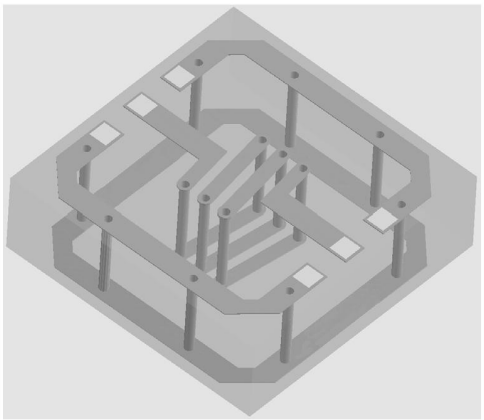

Figure 3. Three-turn solenoid inductor

Design

The 3-D inductor was designed such that the core of the inductor was within a high-resistivity silicon substrate. The inductor windings were a combination of TWIs and copper traces on the top and bottom surface. The 3-D inductor design and layout was structured to facilitate comparison between electrical properties of inductors with the number of turns varying from 1 to 20. Test structures were included on the same die to facilitate measurements and calibration of test equipment.

The devices were fabricated on 4 inch, 400 μm thick high resistivity [>10,000 Ohm-cm] silicon wafers. The diameter of the through-wafer vias was 50 μm and the minimum metal to metal spacing was equal to 25 μm. The inductor windings were made of copper with a Ti layer for adhesion. The TWI vias were left hollow.

The dimensions for a 3-turn inductor are given in Figure 4.

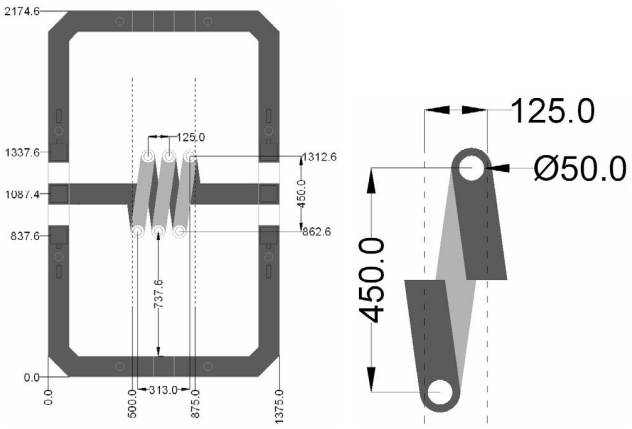

Figure 4. Dimensions for three turn inductor [units in um].

A return path ring was placed on either side of the device. Calibration devices composed of two return rings connected to each other provided a mechanism to null the test equipment. Each inductor winding traversed 125 μm. resulting in the cross sectional area of the inductor of 400 μm x 400 μm.

Fabrication

The starting wafers have the properties given in Table 1.

Table 1. Wafer Characteristics

Feature	Description
Size	4" Diameter, Double-side Polished
Type / Dopant	P/FZ
Resistivity	> 10,000 Ohm-cm
Thickness	400 +/- 15 μm
Orientation	<100>

The 3-D inductors were fabricated using the hollow via TWI process illustrated schematically in Figure 5. The process begins with the fabrication of TWIs (a), followed by the lithography to form the plating template for the Ni/Au

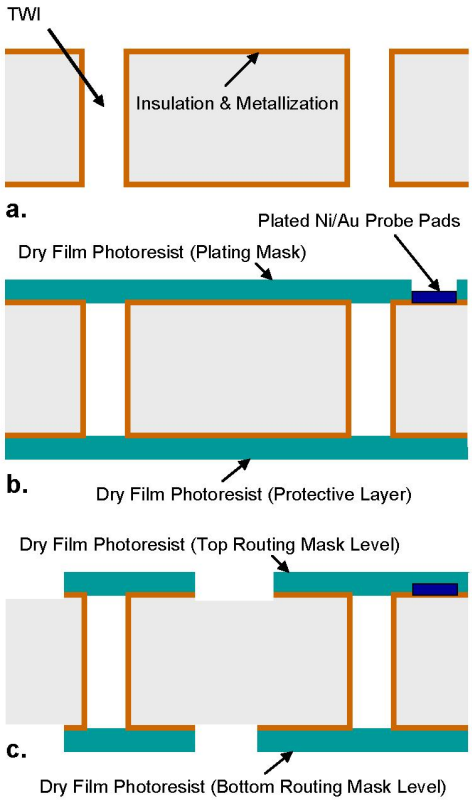

Figure 5. Process flow for the fabrication of 3-D inductors.

probe pads (b) and the patterning of the top and bottom routing (c). The main process steps of the TWI module were described previously [1,2]. The copper thickness in the TWI was 3.5 um. The thickness can be increased if needed to lower the resistance of the inductor windings. It may be undesirable to fill the via completely with copper because of thermomechanical considerations [6]. Figure 6 shows a scanning electron microscopy (SEM) photograph of the top surface of the three turn inductor structure.

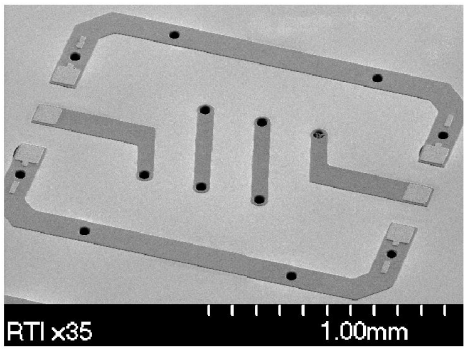

Figure 6. Top side view of the three-turn inductor.

Inductive Element

The quality of an on-chip inductor depends on three factors, namely: 1) the frequency-dependent resistive loss; 2) the self resonance of the inductor; and 3) the substrate-related losses. The frequency-dependent resistive loss is mainly due to the

skin depth resistance, which can be minimized by an appropriate choice of the thickness of the metal winding.

To obtain electrical parameters for the 3-D solenoidal inductors of this work we used the model shown in Figure 7 [7]. The parameters of the model were fitted to the experimentally obtained plots of S-parameters measured as functions of the frequency. Figure 8 shows the comparison of the measurements with the model for a three-turn inductor. The values of the parameters extracted from the fit are listed in Table 2.

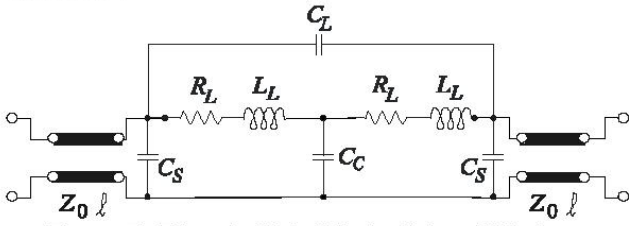

Figure 7. Electrical Model of a Solenoid Inductor

Table 2. Model parameters for the solenoidal inductors.

Turns	L_L(nH)	R_L (Ω)	C_L(fF)	C_S (fF)
1	0.35	0.4	40	35
2	1.2	0.4	45	45
3	1.9	0.5	55	55
4	2.8	0.6	60	55
5	3.8	0.7	60	58

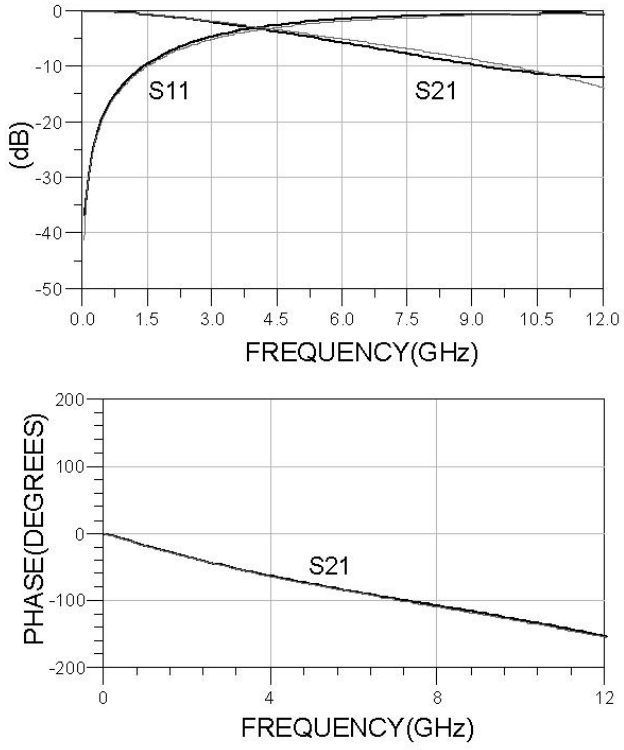

Figure 8. The fit of the model to the S-parameter measurements for frequencies of up to 12 GHz for a three-turn inductor.

For the calculation of the quality factor, Q, of the inductors, we assumed the solenoid being connected in a resonator structure with an ideal shunt capacitor [7]. Figure 9 shows the plots of Q vs. frequency for 1, 2 and 3 turn inductors. The extracted Q's of the tested devices for the frequency of 5 GHz are shown in Table 3. The Q of 30 was obtained at 5 GHz for the one-turn inductor. The value compares favorably with the values characteristic of the spiral 2-D inductors. Corresponding numbers for a 2-turn inductor were 4.6 nH with a Q of 22, and a 10.6 nH inductance with a

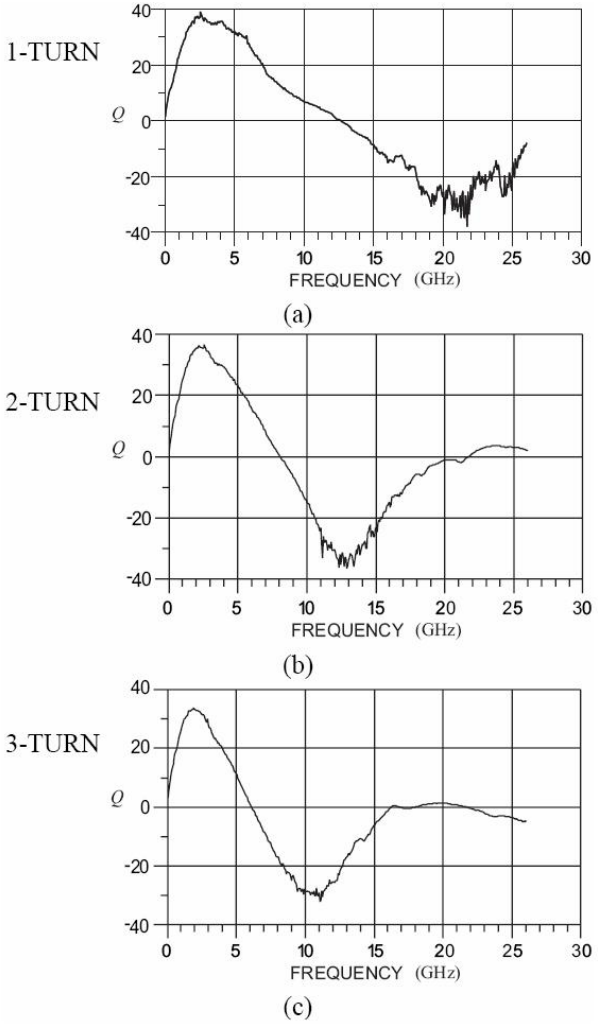

Figure 9. Values of Q plotted as a function of frequency for one-, two- and three--turn inductors.

Table 3. The quality factor, Q, and effective inductance of the one-, two- and three-turn inductors at the frequency of 5 GHz.

Turns	*Leff* (nH/Hz) @5 GHz	*Q* @5GHz
1	1.9	30
2	4.6	22
3	10.6	11

Q of 11. The inductive elements have well-defined signal return paths appearing as slow-wave transmission lines [7].

Conclusions

Three-dimensional inductors utilizing through-wafer copper interconnects for the inductor windings were fabricated. For the one-turn inductor a quality factor of 30 was obtained at the frequency of 5GHz with the effective inductance value of 1.9 nH. The 3-D enabled inductors are being considered for incorporation on interposers in 3-D device stacks.

Acknowledgments

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