Microwave Properties of BST Thin Film Interdigital Capacitors on Low Cost Alumina Substrates

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Abstract — **Barium Strontium Titanate (BST) thin films have a permittivity that is dependent on applied electric-field. As electronically tunable lumped capacitors they can be used as microwave varactors in phase shifters, tunable filters, and delay lines. Generally BST films are deposited on single crystalline substrates. This paper reports on the microwave properties of BST films deposited on low cost alumina substrates by means of metal organic chemical vapour deposition using inexpensive copper metallization. Interdigital capacitors were fabricated yielding capacitors in the sub-picofarad range and tunable by voltages up to 120 V. Low frequency intrinsic Q's of over 100 were obtained. This reduced to external Q's of 17 at 26GHz for 0.5 μm electrodes. The maximum dielectric tunability was found to be about 1.64:1 (40%) for an applied field of 300 kV/ cm at a bias of 120 V.**

I. INTRODUCTION

Barium Strontium Titanate ($Ba_{1-x}Sr_xTiO_3$ or BST) is an attractive candidate for tunable microwave devices as it has high dielectric constant of about 300 for thin films, large field-dependent permittivity, and relatively low dissipation losses [1]. The voltage dependent permittivity of BST enables the fabrication of frequency agile components such as tunable filters, delay lines and phase shifters [2]−[3]. Tunability and loss are traded off in processing and for most microwave applications practical tuning ranges of 2:1 can be achieved with material loss tangents of the order of 0.005. Microwave applications require capacitances in the sub-picofarad range and with three micron lithography interdigital capacitors (IDCs) are required. This is because MIM (metal-insulator-metal) capacitors have a very high capacitance density due to the high dielectric constant of BST thin films. Hence to achieve sub-picofarad capacitance, MIM capacitors require either sub-micron lithography or series connection of capacitors, both of which require expensive multi-layer photolithography. The interdigital varactor lends itself to single layer processing and high Q values.

The substrates generally chosen for BST-based varactors have been sapphire [2]−[3], magnesium oxide (MgO) [4], lanthanum aluminum oxide (LAO) [5], strontium titanate ($SrTiO_3$) and SiO_2/Silicon owing to the high quality BST films that can be grown epitaxially at high temperature on such single crystalline substrates. These substrates are costly and are generally not readily available in large sizes and processing is expensive. Silicon is one possible alternative substrate but it has poor microwave and millimetre wave properties and so-called high resistivity silicon substrate loses its resistivity when processed at the high temperatures required for the fabrication of high quality BST films. However research is being carried out in adapting BST processing to obtain devices compatible with high-resistivity substrates. The focus of the work reported here is the development and characterization of high-quality BST capacitors on low-cost polycrystalline alumina substrates using inexpensive copper metallization and single step processing. Alumina is a well known low-cost substrate and has been used in the microwave industry for decades. It is low loss, readily available and is compatible with most existing fabrication processes.

The quality of the BST thin film is a function of the processing conditions such as temperature, film thickness and thus film integrity, substrate nucleation and other processing conditions [7].These, particularly processing temperature, impose limits on the types and thicknesses of metals that can be used and structures that can be realized. Thus development of BST-based varactors is a trade-off of many factors. In [6] the authors used a 1.8 μm BST film on alumina but with high dielectric losses (with a loss tangent of 0.06) resulting in maximum circuit Q's of about 16. In the work reported in this paper interdigital varactors using 0.3 μm thin film BST were fabricated on alumina substrates and characterized up to 26 GHz. Electrode thicknesses of 0.1 μm and 0.5 μm were considered and intrinsic Q's of more than 100 were obtained. A new model was developed to relate the external and intrinsic Q factors and identify the sources of loss and so guide circuit development.

II. FABRICATION

A metal organic chemical vapour deposition (MOCVD) process at ATMI [8] was used to grow (0.3 μm) ($Ba_{0.5}Sr_{0.5}$) TiO_3 (known as BST–0.5) thin films on 625 µm-thick 99.6 % polished alumina substrates (Intertec Southwest Inc., Tucson, AZ). The MOCVD process provides excellent composition control, good area coverage and conformal coating and hence was used for fabrication of the BST thin films. Film deposition was done at 640°C in the MOCVD chamber. A bilayer liftoff process was used for fabrication of the IDCs. Microchem LOR 5A resist was used in conjunction with Shipley 1813 positive imaging resist to produce a thick bilayer stack. A bilayer liftoff process was chosen since it involves only benign chemicals which do not harm the BST thin film. After a standard photolithography technique the sample was further metallized. Details of the fabrication include a thin (0.03 μm) adhesion layer of chromium deposited by magnetron sputtering at room temperature; this was followed by sputtering of copper which was chosen as the top electrode metal since it provides high conductivity and is also low cost. Finally lift off was completed in a Microchem Remover PG solution. To date copper has not received much attention as electrodes in oxide-based systems (such as BST) due to its inherently poor adhesion property and tendency to oxidize in ambient atmosphere at elevated temperatures. Platinum is the standard electrode material used in BST thin film devices due to its noble metal characteristics but of course it is not low cost. A representative layout of the IDC capacitor is shown below in Fig. 1.

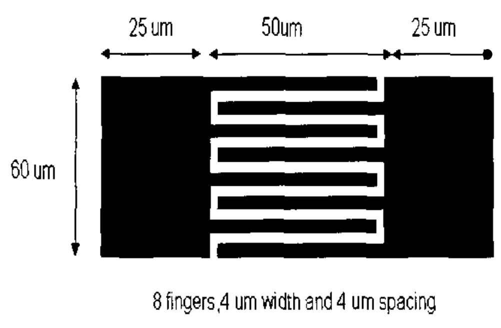

Fig.1. Representative layout of the BST interdigital capacitor.

III.MEASUREMENTS AND RESULTS

Two sets of IDCs with different metal thicknesses were measured in a one-port configuration on a Vector Network Analyzer. One port OSL calibration was performed using 100 μm pitch GS probe and a calibration substrate from GGB Industries (see Fig. 2). Capacitor measurements were done for different number of fingers and also for varying width and spacing of the fingers. The data presented here is for the IDCs with smallest finger spacing since this results in maximum electric field in the BST and hence the largest tuning range. The dimensions of the IDCs for each of the two sets are as follows: $w = 4\ \mu$m, $s = 4\ \mu$m, no. of fingers = 6, 8, 10, length of fingers $\approx 50\ \mu$m. The contact pad size was $25\ \mu$m. Bias was applied to the IDCs using a DC Source/Monitor and a high voltage bias tee. A current limiting resistor network was also used to prevent excess current through the bias tee and network analyzer port in the event of a capacitor shorting out due to the application of high bias voltages.

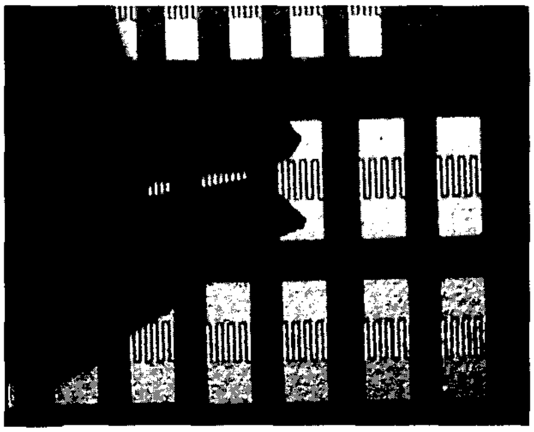

Fig.2. BST interdigital capacitor under test

The reflection data was measured at different voltages up to 120 V. It was found that capacitor breakdown occurred at about 130 V due to air break down. High voltages could be applied if a passivation layer was used as the dielectric breakdown voltage of the BST film was very high. The insulation resistance was found to be of the order of 10 GOhms.

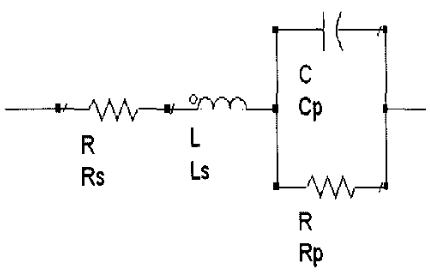

Fig.3. Equivalent Circuit Model of the BST interdigital capacitor.

Using the reflection data, the model of Fig. 3 was extracted using fits of both external Q and reflection data. This proved to be the most reliable way of extracting the model of the device with very high intrinsic Q of the BST. In the process of fitting the parameters to the measured reflection data it was found that the same response could be obtained using different networks resulting in vastly different values of the extracted capacitance. This inconsistency was resolved by simultaneously fitting the model to both reflection data and Q values. As shown in Fig. 5 the agreement between measured and simulated values it quite good. The plot is shown for a capacitor with eight fingers. Though for the sake of clarity the comparison is shown only for zero-bias, the model holds equally well at all bias voltages.

It was found that the extracted series resistance obtained was quite high for the capacitors with $0.1\ \mu$m of metal, in the range of 15–20 Ω ohms, depending on the number of fingers. The values for $0.5\ \mu$m of metal were found to be in the range of $1.5\text{–}2\,\Omega$. These values are quite different from those obtained using simple calculations based on DC resistance and the physical dimensions of the IDC contact pads. Such calculations are based on the assumption that the current distribution in the electrodes is uniform. This is a reasonable assumption up to 26 GHz for the $0.1\ \mu$m electrode and up to 10 GHz for the $0.5\ \mu$m electrode. To investigate this discrepancy further the quality of the sputtered copper was evaluated using a sheet resistance method using the four-point probe technique. It was found that the resistivity of the sputtered copper film was substantially higher than that of bulk copper metal. The resistivity was higher by a factor of 50–60 times that of bulk copper. This explains why such high values for series resistance were extracted. The impact of this on external Q is shown in Fig. 4 for two different electrode thickness.

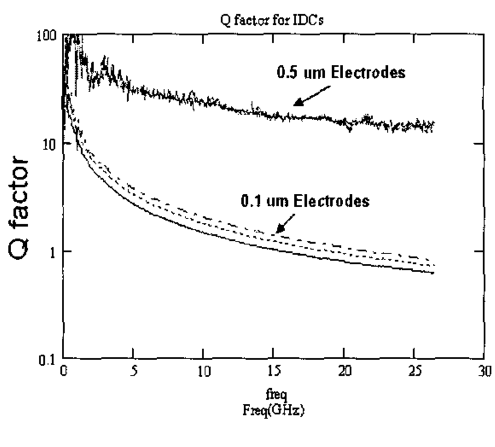

Fig.4. Q factor of the BST interdigital capacitor.

The total device Q factor was obtained using the following formula: $Q = |\Im Z_{11} / \Re Z_{11}|$. It can be seen that using a thicker metal can improve the Q by as much as an order of magnitude. In the microwave region the Q factor is primarily limited by the series conductor losses and hence it is not feasible to use BST-based capacitors as discrete components. In the discrete form the advantages of having a high quality BST thin film is systematically undermined by the series resistance resulting from the contact to the capacitor. Thus the solution is to use BST varactors in an integrated fashion. As seen in Fig. 4 the Q factor for the capacitor with $0.5\ \mu$m of metal is 17 at 26 GHz while that of the capacitor with $0.1\ \mu$m of metal is about 1 at the same frequency. Hence the benefits of using a thicker metal is quite obvious .It should be noted that these values are comparable to or better than that reported in the literature for similar IDC structures. These results have been obtained despite the fact that the copper deposition process is not very well optimized. This clearly indicates that the quality of the BST thin film is quite good and Q factor is primarily limited by the metallic losses in the GHz range.

The tunability was calculated by fitting a model to the measured data across various bias voltages. Unlike the simple parallel RC model widely used in the literature it was found that a good fit was obtained only if the series resistance and the series inductance was taken into account. This is particularly true at higher frequencies when the effect of such parasitic elements is most significant.

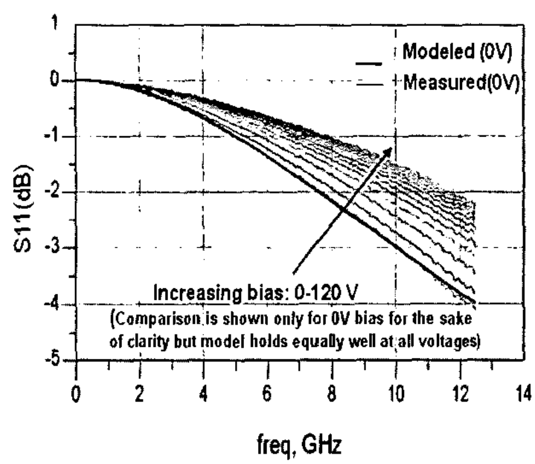

Fig.5. Measured reflection data for the BST interdigital capacitor.

Comparison of the measured and modeled Q is shown in Fig. 6. The typical peaking behaviour of Q factor with frequency is evident in the plot. The peak occurs where the contribution due to metallic losses begins to overtake the losses due to dielectric dissipation, since the former is directly proportional to frequency while the later is inversely related to frequency. The measurement uncertainties correspond to high intrinsic Q of the capacitors. However the frequency of the peak of the external Q is most critical in determining the intrinsic Q rather than the absolute value of the Q at the peak. From this the intrinsic Q of the BST capacitor, without the parasitic series resistance was determine to be in the range of 100 to 250. Tunability for the IDC with electrode thickness of 0.1 μm was found to be about 35% at a bias voltage of 120V, for the 6 finger capacitor the capacitance decreased from 200 fF to 130 fF. For the 8 finger IDCs the capacitance decreased from 252 fF to 154 fF for a 40% tuning or 1.64:1 tuning ratio at 120 V. The extracted capacitance values were compared with values obtained using the analytic model in [9] and the agreement was very good. It should be noted that although Q factor measurements at zero-bias could be performed up to a frequency of 26.5 GHz, the reflection data for different bias voltages was recorded only up to a frequency of 12 GHz. This is due to the upper frequency limit of the high voltage bias tee that was used. Note that the tunability data is expected to be independent of frequency.

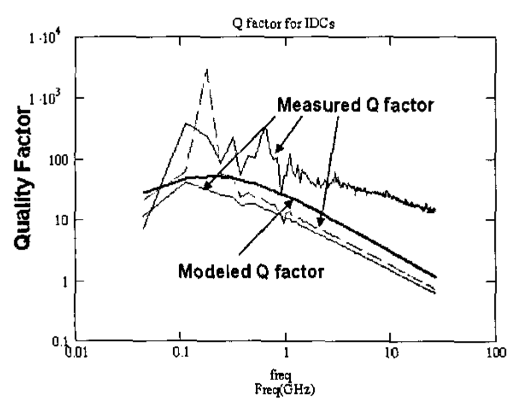

Fig.6. Comparison of the measured and modeled Q factors.

IV. CONCLUSION

Microwave characterization of thin film BST IDCs on low-cost alumina substrates using inexpensive copper metallization has been presented. An accurate model was developed and the capacitance, intrinsic Q and tunability values were extracted. Q at 26 GHz was found to be 17 and tunability of 1.64:1 for an applied field of up to 300 KV/cm observed. This is comparable to results reported in the literature by other groups but on expensive single crystalline substrates. It is expected that with thicker electrodes the external Q factor would be significantly higher. The effect on Q factor was quite dramatic with change in electrode thickness. With optimised copper deposition process the Q values are expected to increase further. It should be possible to obtain higher tunability by using smaller finger spacing to increase the applied electric field and also by using a passivation layer over the electrodes for applying higher voltages.

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