Toroidal Inductors for Radio-Frequency Integrated Circuits

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***Abstract*—Toroidal inductors achieve low loss by constraining magnetic flux to a well-defined path and away from ground planes and semiconducting substrates. This paper presents a micromachined implementation of the toroidal inductor, with focus primarily on microwave integrated circuits on a low-resistivity silicon wafer achieving a Q of 22 and a self-resonant frequency greater than 10 GHz. A verified analytic model is developed.**

***Index Terms*—Inductor, micromachining, monolithic microwave integrated circuit (MMIC), radio-frequency integrated circuit (RFIC), toroidal inductor.**

I. Introduction

LUMPED inductors are essential elements in radio-frequency (RF) and monolithic microwave integrated circuits (MMICs). They are used on-chip in matching networks where transmission-line structures may be of excessive length. More commonly, they are used as RF chokes allowing bias currents to be supplied to circuits while providing broad-band high impedance at RF frequencies and above. They are also used to ensure stability at frequencies below the frequencies of operation—a function that cannot be realized using transmission-line sections. Lumped inductors embedded in packaging and in traditional circuit-board laminates are also used with the same properties.

Traditionally, on-chip inductors are realized as spiral inductors, such as that shown in Fig. 1. With low-resistivity silicon substrates, inductor performance is compromised by loss, resulting from magnetic flux in the semiconducting substrate inducing eddy currents. These induced currents follow a path under the conductors of the spiral and, just as with ground-plane eddy currents, lower the inductance achieved. Eddy currents are also excited in package metallization. Schemes that disrupt the eddy current include tessellated ground planes and doped radial lines (see [1]–[7]). Eddy currents are significantly reduced in high-resistivity substrates (such as high-resistivity silicon, GaAs, ceramic, and glass) resulting in Q's of 20 and higher (see [4] and [8] for further details).

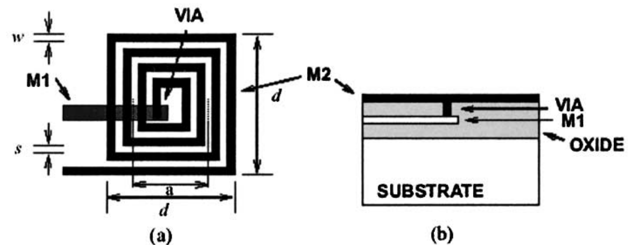

Fig. 1. On-chip spiral inductor. (a) Top view. (b) Side view.

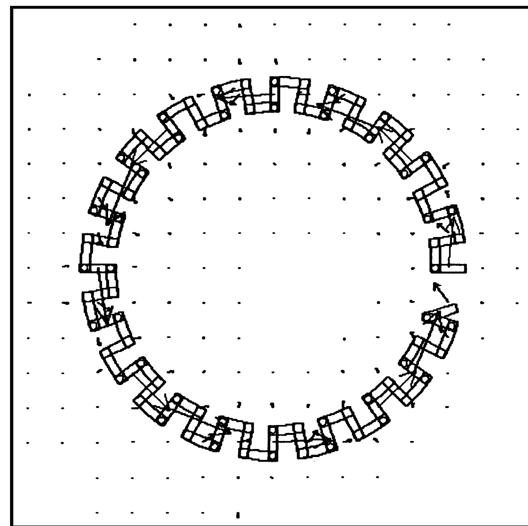

Fig. 2. Simulated magnetic-field distribution of a 21-turn toroidal inductor at 100 MHz, obtained by Agilent HFSS simulation (the rectangles represent the metallized segments. The arrows show the flux lines pointing to the anticlockwise direction).

The toroidal inductor presented here was developed as a post-processing technology for monolithically integrated circuits (ICs) that confines flux (see Fig. 2). The advantages of toroidal structures have recently been demonstrated [9]. Here, a low-frequency inductance of 5.5 nH and a Q of 42 at 4 GHz were successfully obtained from a 15-turn toroidal inductor fabricated in a polymer package. This implementation requires polymer encapsulation and was not intended for direct integration with radio-frequency integrated circuits (RFICs) or microwave ICs. A printed wiring board implementation by the authors and derived from the concept [10] reports an inductor with a low-frequency inductance of 0.95 nH, a peak

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TABLE I
SUMMARY OF PERFORMANCE OF SOME PUBLISHED INDUCTORS THAT CAN BE FABRICATED ON LOW-RESISTIVITY SILICON SUBSTRATES

Micromachining Technology	Inductance (nH)	Peak-Q	Peak-Q frequency (GHz)	Self-resonant frequency (GHz)	Reference	Year
Spiral on silicon cavity, by bulk-micromachining	100	N/A	N/A	3	Chang [18]	1993
	1.1-1.55	15-20	~11	N/A	Sun [17]	1996
	6.3	13.3	4.6	6.6	Nam [19]	1997
	4.8	30	1	> 6	Young [20]	2001
Meander-type straight solenoid, by surface micromachining	4.8	30	1	> 6	Young [20]	1997
	2.7	17	2.4	>10	Yoon [21]	1999
	2.6	21	4.5	>10	Chen [22]	2001
Spiral on polymer, by surface micromachining	10	5.5	1.2	6	Kim [23]	1995
	18	18	10	N/A	Volant [8]	2000
	2.6	17	2.5	N/A	Rogers [24]	2001
Suspended spiral, by surface micromachining	16	16	0.1	> 2	Park [25]	1999
	1.8	50	7	>10	Yoon [26]	1999
	1.4	70	6	>20	Yoon [27]	2001
Meander-type toroidal, by surface micromachining	400	~1.5	<0.001	<0.1	Ahn [12]	1994
	200	~1	<0.01	<0.1	Ahn [13]	1994
	10000	N/A	N/A	<0.1	Ahn [14]	1999

Q of greater than 40 at approximately 100 MHz, and a cutoff frequency of less than 1 GHz. On-wafer toroidal inductors integrated with a magnetic core have been demonstrated for low-frequency (up to 1 MHz) power electronic applications [11]–[13]. The main feature of the toroidal inductors is that the flux is confined and little eddy current is induced.

This paper is concerned with realizing high-performance inductors on low-resistivity substrates. In this paper, issues relating to integrated inductors on low-resistivity silicon substrates are first reviewed. This is followed by an exposition of micromachining technology developed by the authors for on-chip RF toroidal inductors and then by the development of a verified analytic model.

II. INDUCTORS ON LOW-RESISTIVITY SILICON

The quality of an on-chip inductor depends on three factors, namely: 1) the frequency-dependent resistive loss; 2) the self-resonance of the inductor; and 3) the substrate-related losses. The frequency-dependent resistive loss is mainly due to the skin resistance, which can be reduced by thick metallization. Another dominant loss mechanism related to resistive loss is current crowding [14], [15]. This is a particular problem with multiturn spiral inductors, which are required to realize high inductance values. Current crowding results when the magnetic field produced by one turn penetrates an adjacent trace creating eddy currents so that current peaks on the inside edge of the victim trace (toward the center of the spiral) and reduces on the outside edge. This constricts current and results in higher resistance than would be predicted from skin effect and dc resistance alone [14]. The best Q that can be achieved for conventional spiral inductors on low-resistivity silicon is around six with a self-resonant frequency of 3.5 GHz [8].

Parasitic capacitance of the fabricated inductor results in resonance of the on-chip structure and, hence, limits the frequency of operation. The self-resonant frequency can be controlled by a careful choice of design parameters, such as the number of turns, turn-to-turn spacing, and metal width. The effective permittivity of the medium can be reduced by adding a polyimide layer ($\varepsilon_r = 3.2$) and using metallization on top of this layer [2]. While this result was obtained with a GaAs substrate, the same benefit would be obtained with an Si substrate. With thick metallization to reduce resistance, a Q that is 50% larger and a self-resonant frequency that is 25% higher [2] can be obtained.

The substrate-related losses, however, are largely process dependent and cannot be minimized by layout optimization alone. In the case of a silicon substrate, the induction of charges in the silicon and the insignificant skin depth of the silicon substrate has the effect of increasing the capacitance of an interconnect line over silicon as the electric field lines are terminated on the substrate charges. This effect is superimposed on the effect of eddy currents in the substrate. The magnetic-field lines penetrate some distance into the substrate so that the LC product is greater if the substrate was insulating (as with GaAs). The effect is that the velocity of propagation along the interconnect $(= 1/\sqrt{LC})$ is reduced, leading to what is called the slow-wave effect.

In an attempt to minimize the substrate-related problem, many micromachining techniques targeted at microwave ICs were introduced beginning in 1990. In general, micromachining can be classified as being bulk micromachining or surface micromachining. In bulk micromachining, low substrate-related losses are achieved by etching away the underlying substrate [16], [17]. Bulk micromachining, at the moment, is limited to planar spiral inductor designs. In surface micromachining, substrated-related losses are reduced by separating the inductive parts of the inductor from the substrate plane either with an air gap or with a low-dielectric material. Surface micromachining allows more topological flexibility in inductor design [11]–[13], [19]–[26], [32]. Due to its low-temperature requirement, surface micromachining can be applied to almost all IC processes. Table I summarizes the performance of

inductors obtained using various micromachining approaches compatible with current bulk CMOS technologies.

Our design goal was the development of a micromachining process that could be utilized with fabricated silicon wafers without requiring changes to the silicon process. A surface-micromachining technology was developed that controls the Q of inductors by confining the magnetic flux lines to a defined path and ensuring that they do not intersect with metals and semiconductor materials where they would induce eddy currents. Magnetic flux leakage lowers the inductance that can be achieved since the eddy currents reduce flux coupling. The proposed toroidal inductor not only confines the magnetic fields, but optimizes the tradeoff between flux linkage and turn-to-turn parasitic capacitance that limits the frequency of operation. For the same inductance, toroidal structures also consume significantly less area than the straight solenoid inductors, even though the fabrication processes for planar toroidal and solenoid structures are largely similar. More importantly, the magnetic field in a toroidal inductor is largely concentrated along the core, as revealed in the HFSS[1] simulation result shown in Fig. 2. A concentrated magnetic field along the core results in less noise coupling and electromagnetic interference with the neighboring components [9].

III. Micromachined Implementation

The micromachined implementation of the toroidal inductor is based on a procedure for fabrication of suspended meander-type structures on a processed silicon wafer. Our fabrication procedure is similar to other published methods [11]–[13], [19]–[27] in that a photoresist is used to temporarily form a layer that isolates the metallization to be suspended above the substrate. However, in our technique, the anchoring points are fabricated together with the turns of the inductor in this process. The whole process eliminates the need for a separate step to electroplate vias at the anchoring points to obtain the same air-bridge functionality. Unlike many other techniques [19]–[27], our process does not require a photoresist of very high aspect ratio. The fabricated toroidal structures can withstand violent mechanical vibration, as opposed to suspended spiral inductors and membrane-supported inductors, which are, in general, relatively fragile.

The toroidal inductor was fabricated on a low-resistivity (20 $\Omega \cdot$ cm) silicon substrate with a thickness of 500 μm corresponding to current bulk CMOS technology. (Low resistivity silicon has a resistivity ranging from 0.1 to 20 $\Omega \cdot$ cm and, by comparison, silicon is available with resistivities as high as 100 k$\Omega \cdot$ cm.) One turn of the inductor is shown in Fig. 3. A scanning electron microscopy (SEM) image of the completed structure is shown in Fig. 4 and it has an outer diameter of 1 mm.

The steps in the fabrication process are as follows.

Step 1) To begin with, the metal strips representing the input/output lead lines and the bottom metal segments of the inductor are photolithographically defined and metallized by either evaporation or ion sputtering, with preferably chromium and then gold. See Fig. 5(a).

Step 2) A thin layer of silver is then selectively deposited so that it covers the whole area of the inductor. This layer is intended as a seed layer for electroplating in Step 7. See Fig. 5(b).

Step 3) A layer of thick photoresist is then deposited onto the wafer, with the thickness of the photoresist defining the suspension height of the metal bridge. AZ4620, AZ9260, or SJR5740 can be used to attain a good thickness. See Fig. 5(c).

Step 4) The anchoring points are photolithograhically patterned onto the layer of photoresist formed in Step 3. See Fig. 5(d).

Step 5) Another layer of gold or gold/palladium is then deposited onto the top of the photoresist that defines the anchoring points, preferably by ion sputtering. See Fig. 5(e).

Step 6) Another thin layer of photoresist defining the metal bridges is then photolithographically patterned, forming the etch mask for the suspended bridges. The photoresist for this step is preferably different from the one chosen in Step 3. See Fig. 5(f).

Step 7) The bridges of the inductor are etched off using a suitable gold etchant. The unexposed photoresist deposited in Step 6 is now exposed under ultraviolet light and developed away. The metal bridges of the inductor are then thickened significantly by electroplating, preferably with copper first and then gold. The presence of the gold coating protects the toroidal

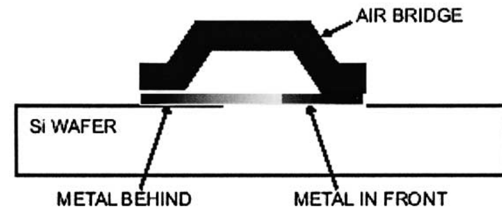

Fig. 3. Coiled cross section showing air bridge constructed using micromachining.

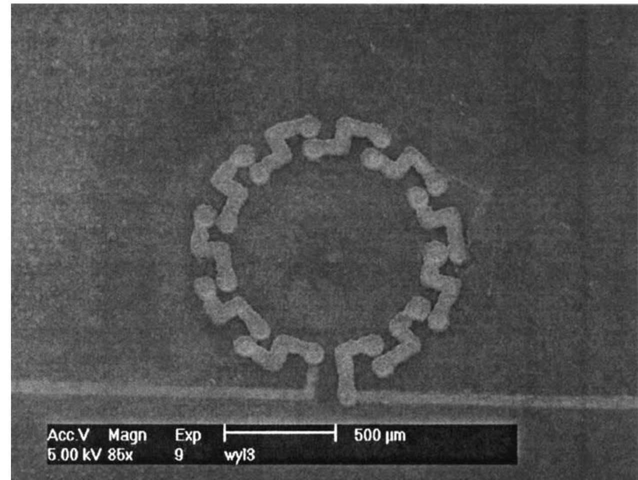

Fig. 4. SEM image of the on-chip toroidal inductor fabricated on a low-resistivity silicon wafer.

[1]Agilent Technol., Santa Rosa, CA.

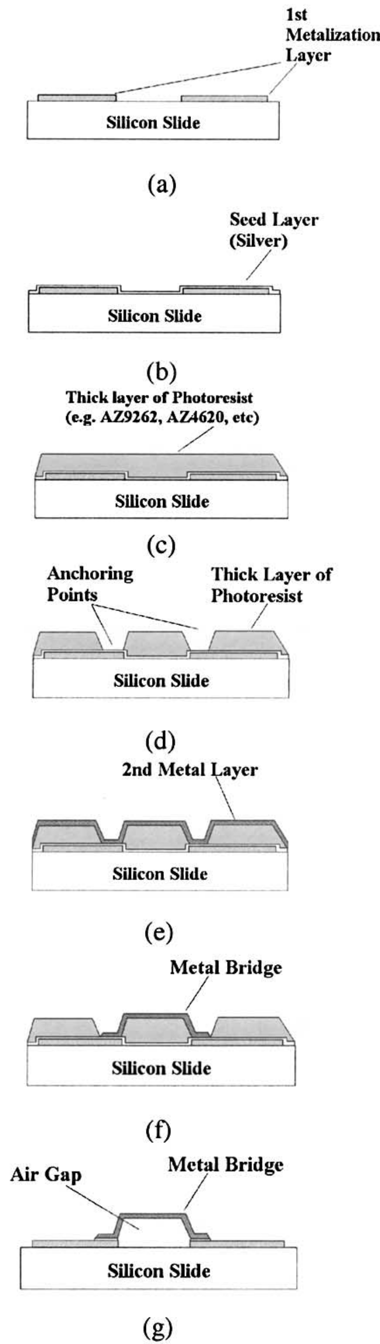

Fig. 5. Process flow for fabrication of on-chip toroidal inductor.

structure from oxidation and any other chemical attack during the process. See Fig. 5(g).

Step 8) Finally, the photoresist that remains in the wafer is stripped off using isopropyl alcohol (IPA) and acetone. The residues of the photoresist not removable by solvents can be dry etched by oxygen plasma. Finally, the silver seed layer deposited in Step 2 is etched away using iron III nitrate.

IV. Analytical Treatment

The conventional inductance formula ($L = \mu_o N^2 A/l$) for an air-core toroidal inductor is based on an assumption that all the flux links all the turns. In many cases, however, a microwave

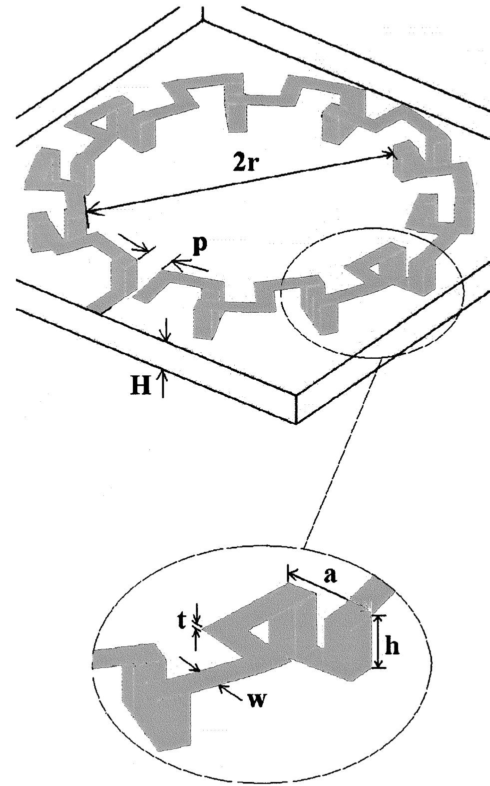

Fig. 6. Three-dimensional (3-D) illustration of on-chip toroidal inductor (the circled section represents a unit turn).

toroidal inductor is designed to have appreciable spacing between turns so that the turn-to-turn capacitive coupling and substrate parasitic between two successive turns are minimized. With the turns loosely coupled, partial flux linkage is unavoidable [28]. Incomplete flux linkage leads to additional filamentary inductance between two neighboring turns. The conventional formula alone, therefore, does not reliably predict the low-frequency inductance of on-chip or packaged meander-type solenoid structures. In our toroidal structures, for example, the inductance obtained from the conventional formula is generally at least 20% below the realized value. Hence, there is a need to develop a reliable empirical model applicable to the inductor design operating at microwave frequencies.

Instead of adjusting the conventional formula ($L = \mu_o N^2 A/l$) to apply to the real physical world, we can view the toroidal structure on a turn-by-turn basis. The toroidal structure, as shown in Fig. 6, can be envisioned as a finite periodic structure having a chain of loosely coupled rectangular turns connected in series, as illustrated in Fig. 7. In Fig. 7, Z represents the series reactance contributed by two effects, which are: 1) the substrate-independent effect due to the longitudinal current flow and 2) the substrate-related effect due to the transverse current flow. The substrate-independent effect in Z is modeled by the loop resistance R_t, the loop inductance L_t, and the turn-to-turn capacitance. The substrate-related effect in Z is modeled by the substrate resistance R_{sub} between two successive turns and the oxide capacitance C_{ox} underneath each bottom metal segment. Y represents the lumped admittance to ground due to oxide capacitance C_{ox}, stray capacitance

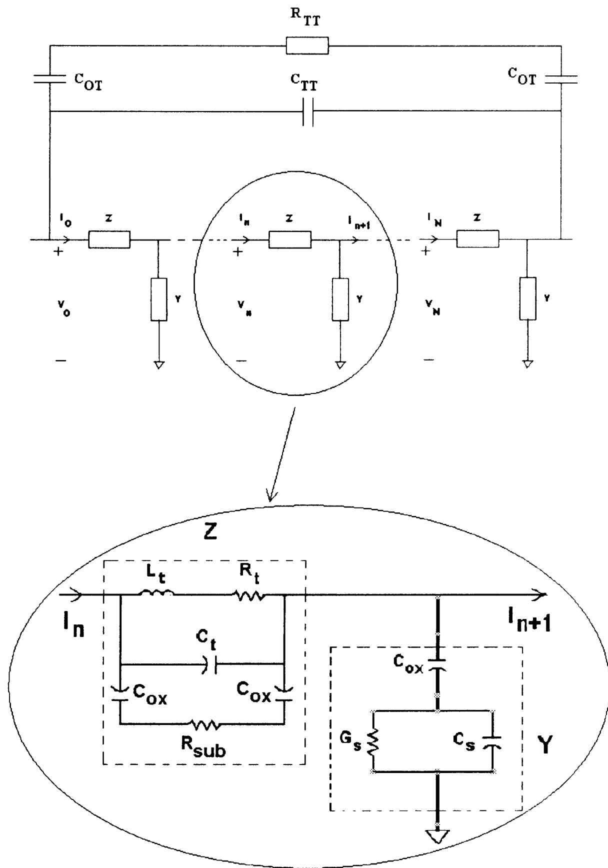

Fig. 7. Equivalent circuit of a toroidal inductor (the circled region represents a unit turn and is highlighted).

C_s, and stray conductance G_s underneath each bottom metal segment. Attached to the input/output ports of the inductor are predominantly the parasitic elements, including the oxide capacitance attached to the terminals $C_{\rm OT}$, the terminal-to-terminal capacitance $C_{\rm TT}$, and the terminal-to-terminal substrate resistance $R_{\rm TT}$ due to the physical closure between the two terminals.

In the analysis that follows, the variables used in Fig. 7 are empirically derived and expressed using the physical parameters given in Fig. 6, i.e., separation between two terminals $= p$, average metal thickness $= t$, metal track width $= w$, inner radius of the toroidal ring $= r$, core width $= a$, substrate thickness $= h_s$, oxide thickness $= h_{\rm ox}$, and total number of turns $= N$ (the spacing between the two terminals is also considered as a turn).

For each turn of the inductor, the loop inductance L_t can be considered as a combined contribution of: 1) self-inductance of each turn; 2) filamentary inductance caused by the strip metal connecting neighboring turns; and 3) mutual inductance due to the closure between neighboring turns. The self-inductance of each turn is approximated using the rectangular loop inductance formula given in [29] as

$$L_{\rm self} = \frac{\mu}{\pi}\left[a\ln\left(\frac{2a}{t}\right) + h\ln\left(\frac{2h}{t}\right) + 2\sqrt{a^2+h^2} - a\sinh^{-1}\left(\frac{a}{h}\right) + h\sinh^{-1}\left(\frac{h}{a}\right) - 1.75(a+h)\right]. \quad (1)$$

Connecting two neighboring turns is a filamentary conductor that also contributes appreciable filamentary inductance to the whole structure [27]. Being highly dependent on the metal thickness, length, and width, the filamentary inductance between turns becomes particularly dominant for the inductor fabricated on a wafer in microscale. This is because the metal of an on-chip inductor is normally thin. The filamentary inductance of the strip metal connecting two neighboring turns can be calculated using the formula in [20] with some modifications as

$$L_{\rm fila} \approx 2l_x\left\{\ln\left(\frac{2l_x}{w+t}\right) + 0.500\,49 + \left(\frac{w+t}{l_x}\right)\right\} \quad (2)$$

where $l_x = (a+2r)/N$. The mutual inductance between two neighboring turns can be approximated using the formula given in [30] as

$$L_m \approx \frac{\mu}{2\pi(0.5a+r)^3}(ah)^2. \quad (3)$$

The total loop inductance per turn is then

$$L_t = L_{\rm self} + L_{\rm fila} + 2L_m \quad (4)$$

where $L_{\rm self}$, $L_{\rm fila}$, and L_m are, respectively, given in (1)–(3).

The substrate resistance $R_{\rm sub}$ between two neighboring turns is due to the transverse current flow and can be determined by conformal mapping [31]

$$R_{\rm sub} = \frac{\rho_s}{aF}\exp\left(\frac{-t}{2\sqrt{\frac{\rho}{f\pi\mu}}}\right) \quad (5)$$

where ρ_s and ρ are, respectively, the resistivity of the substrate and the resistivity of the metal segments. f is the operating frequency. F is a geometric factor and can be approximated as

$$F = \frac{1}{\pi}\ln\left(\frac{2(1+\sqrt{k})}{1-\sqrt{k}}\right) + \left\{\left[\frac{1}{\pi}\ln\left(\frac{2(1+\sqrt{k'})}{1-\sqrt{k'}}\right)\right]^{-1} - \frac{1}{\pi}\ln\left(\frac{2(1+\sqrt{k})}{1-\sqrt{k}}\right)\right\} \times \frac{1}{1+\exp\left(\frac{k-0.707}{0.0001}\right)} \quad (6)$$

where

$$k = \frac{aN}{aN+4(a+r)\pi} \text{ and } k' = \sqrt{1-k^2}. \quad (7)$$

Assuming that the metal segment on the substrate plane is sufficiently thick (i.e., $t > \sqrt{\rho/(\mu f\pi)}$), we can approximate the oxide capacitance $C_{\rm ox}$ underneath each bottom metal segment as

$$C_{\rm ox} = \frac{4\varepsilon_o}{h_{\rm ox}}aw. \quad (8)$$

Based on [32, eq. (12)], the turn-to-turn capacitance C_t is approximated as

$$C_t = \frac{2\pi(a+h)\varepsilon_o}{\ln\left(\frac{a+r}{Nt}\pi + \sqrt{\left(\frac{a+r}{Nt}\pi\right)^2 - 1}\right)}. \tag{9}$$

For one turn, the parasitic stray capacitance is approximately

$$C_s = \frac{\varepsilon_r \varepsilon_o}{H} aw \tag{10a}$$

and the parasitic stray conductance is approximately

$$G_s = \frac{aw}{(\rho_s H)}. \tag{10b}$$

Here, we assume that the parasitic stray conductance to the ground plane is independent of operating frequency.

By Wheeler's formula, which assumes that the metal thickness is at least four times the skin depth, the loop resistance R_t per single turn is

$$R_t = \frac{\rho\left(\frac{\pi(a+2r)}{N} + 2(a+h)\right)}{wt - (w-2\delta)(t-2\delta)} \tag{11}$$

where δ is the skin depth of the metal strip and is given by $\delta = \sqrt{\rho/(\pi\mu f)}$.

By analogy to (9), the terminal-to-terminal capacitance C_{TT} can be approximated according to the spacing between the two terminals p, and can be approximated as

$$C_{\mathrm{TT}} = \frac{2\pi(a+h)\varepsilon_o}{\ln\left(\frac{p}{t} + \sqrt{\left(\frac{p}{t}\right)^2 - 1}\right)}. \tag{12}$$

Also, by analogy to (5), the terminal-to-terminal resistance R_{TT} can be similarly approximated by conformal mapping as

$$R_{\mathrm{TT}} = \frac{\rho_s}{aF_p} \exp\left(\frac{-t}{2\sqrt{\frac{\rho}{f\pi\mu}}}\right) \tag{13}$$

where the geometric factor F_p is similar to F, defined in (6), where k is replaced by k_p and now

$$k_p = \frac{a}{a+2p} \text{ and } k_p' = \sqrt{1-k_p^2}. \tag{14}$$

The series impedance Z contributed by R_t, L_t, C_t, C_{ox}, and R_{sub} (see Fig. 7) is given by

$$Z = \frac{1}{j\omega C_t + \left(\frac{1}{R_t + j\omega L_t}\right) + \left(\frac{1}{R_{\mathrm{sub}} + \frac{2}{(j\omega C_{\mathrm{ox}})}}\right)}. \tag{15}$$

Y is the lumped admittance to ground (see Fig. 7)

$$Y = \left(\frac{1}{j\omega C_{\mathrm{ox}}} + \frac{1}{G_s + j\omega C_s}\right)^{-1}. \tag{16}$$

The toroidal inductor model is completed by developing the propagation characteristics of the finite periodic structure. From Fig. 7, the characteristic impedance Z_o of the periodic structures is

$$Z_o = \sqrt{\frac{Z}{Y}} \tag{17}$$

where Z and Y are given by (15) and (16). Using general transmission-line analysis, the propagation constant of the said periodic structures can be approximated as

$$\gamma d = \sqrt{ZY}. \tag{18}$$

For N periodic structures connected in series and terminated in a load impedance Z_L, the input impedance is found as

$$Z_i = Z_o \frac{Z_L + Z_0 \tanh(N\gamma d)}{Z_0 + Z_L \tanh(N\gamma d)}. \tag{19}$$

The task now is to calculate the terminal-to-terminal impedance of the toroidal structure. This can be found by substituting $Z_L = 0$ into (19). When the terminating impedance is zero, we have

$$Z_i = Z_0 \tanh(N\gamma d) = \sqrt{\frac{Z}{Y}} \tanh\left(N\sqrt{ZY}\right). \tag{20}$$

As emphasized earlier, the terminal-to-terminal capacitance and resistance need to be taken into account. The terminal-to-terminal capacitance C_{TT} and the terminal-to-terminal resistance R_{TT} are, respectively, given by (12) and (13). The resultant impedance of the inductor Z_L is then

$$Z_L = \sqrt{\frac{Z}{Y}} \tanh\left(N\sqrt{ZY}\right) // \left(\frac{1}{j\omega C_{\mathrm{TT}}} // \left(\frac{2}{j\omega C_{\mathrm{OT}}} + R_{\mathrm{TT}}\right)\right). \tag{21}$$

From this, the important characteristics of an inductor can be determined including the low-frequency inductance Q and self-resonant frequency.

V. Results

A toroidal inductor was fabricated on low-resistivity silicon (20 $\Omega \cdot$ cm) with the following geometrical parameters: separation between two terminals, $p = 100$ μm, average metal thickness $t = 8.3$ μm, average metal track width $w = 70$ μm, inner radius of the toroidal ring $r = 440$ μm, core width $a = 170$ μm, substrate thickness $h_s = 500$ μm, oxide thickness $h_{\mathrm{ox}} = 0.5$ μm, and the number of turns $N = 11$.

The vector-network-analyzer measurement has been carried out for the fabricated inductor. The bond pad parasitic and the feed transmission line deembedded from the measurement with

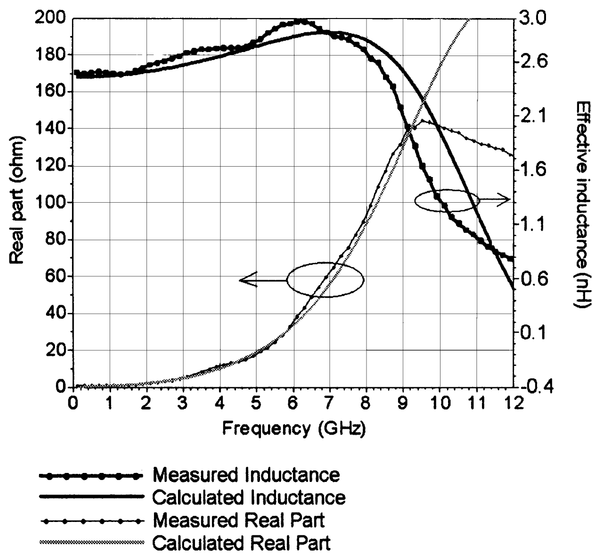

Fig. 8. Calculated and measured response of the micromachined toroidal inductor. The real part of the impedance is shown together with the effective inductance.

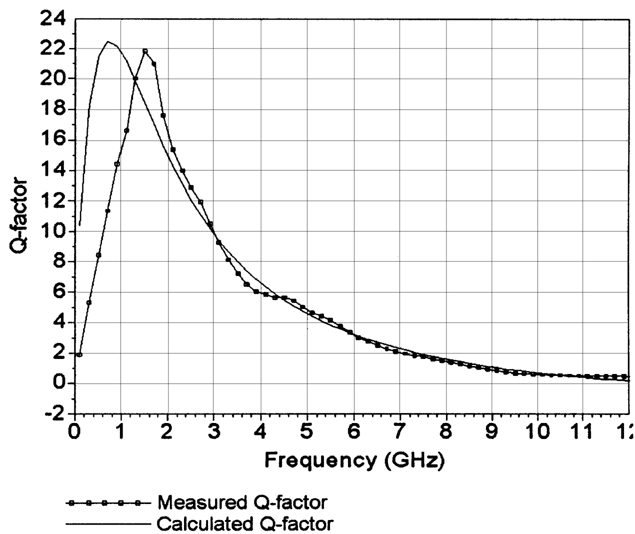

Fig. 9. Calculated and measured Q versus frequency.

the help of two-dimensional electromagnetic simulation to characterize the line. The resulting deembedded measurement is noticeably similar to the calculated result. The measured and calculated characteristic of the micromachined toroidal inductor are shown in Fig. 8. Below the self-resonant frequency (here, greater than 10 GHz), the measured inductance is 2.5 nH, compared to the calculated low-frequency inductance of 2.45 nH. The finite real part is due to the frequency-dependent conductance of the silicon substrate. Fig. 9 shows the calculated and measured Q factor versus frequency. The measured peak Q was found to be 22 at 1.5 GHz, while the calculated peak Q was around 22.5 at 0.75 GHz. The calculated and measured refection coefficient are shown in the Smith chart of Fig. 10. The discrepancy in the measured and calculated frequency of peak Q is attributed to the great sensitivity to the measurement of low-resistance values. However, as can be seen in Figs. 8 and

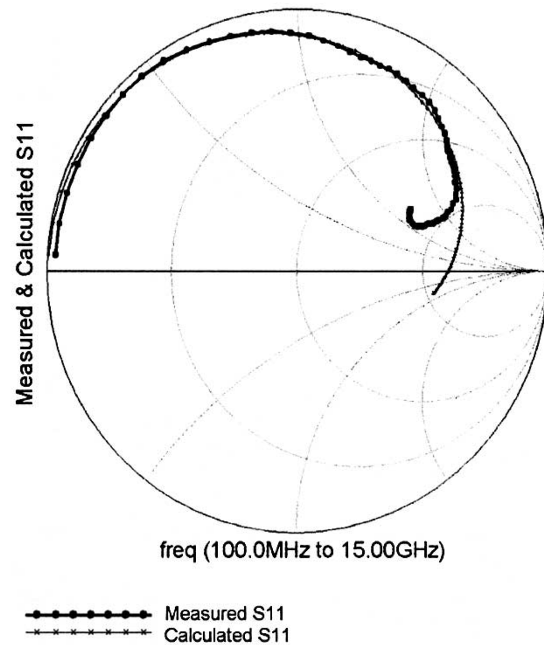

Fig. 10. Smith chart of the calculated and measured S_{11} of the micromachined toroidal inductor.

10, the absolute values of inductance and resistance are calculated accurately.

According to our observation, the substrate parasitic, in general, outweighs the effect of turn-to-turn capacitance and resistance. It is expected that fabricating the toroidal inductor on a tessellated ground plane can alleviate the substrate parasitic burden and further improve the performance of the inductor.

VI. Conclusion

This paper has presented the toroidal inductor as an enabling technology for use in RF and microwave ICs. Measurement reveals that an inductance of 2.45 nH, a peak Q of 22 at 1.5 GHz, and a self-resonant frequency greater than 10 GHz were obtained from an 11-turn toroidal inductor fabricated on a low-resistivity silicon substrate. These are the best reported results for integrated toroidal inductors on low-resistivity silicon substrates. An analytic model was developed and verified with measurements. Part of the significance of this study is that it may not be necessary to utilize a high-resistivity silicon process to realize efficient high-performance silicon RFICs.

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