A NOVEL ENVELOPE-TERMINATION LOAD-PULL METHOD FOR ACPR OPTIMIZATION OF RF/MICROWAVE POWER AMPLIFIERS

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Abstract *A novel load-pull method for envelope-termination characterization is presented. The method enables the source and load envelope terminations to be easily evaluated to further optimize the linearity/efficiency tradeoff of RF/microwave power transistors used in digital wireless communication systems with time-varying envelopes. Results are presented for a 53 mm low-voltage LDMOS transistor at 850 MHz. It is shown that the optimal envelope termination may in general be complex, in contrast to the commonly held belief that the envelope-termination must be approximately zero. A simplified Volterra series analysis is used to qualitatively explain how the envelope termination impacts linearity.*

I. INTRODUCTION AND MOTIVATION

Adjacent channel power ratio (ACPR) is the standard figure of merit for linearity characterization of RF power amplifiers used in digital wireless communication systems [1]-[4]. Though it is possible to correlate intermodulation of an arbitrary order to ACPR, direct source/load-pull measurement of ACPR is the most useful method for large-signal linearity characterization of RF/microwave transistors [5]-[7]. The three most common methods of load-pull are, respectively, passive-mechanical, passive-solid-state, and active [8]-[10]. First reported in 1995, each of these methods are now capable of supporting automated ACPR characterization [11]. More recently, each of these methods have been extended to support multi-harmonic source/load-pull characterization. Multi-harmonic source/load-pull characterization allows optimization of harmonic terminations to further improve the linearity/efficiency tradeoff of a transistor.

Most digital wireless standards are based on PSK modulation, which requires band-limiting for acceptable spectral efficiency. Band-limiting imparts a time-varying envelope, necessitating quasi-linear amplification of the modulated carrier. After quasi-linear amplification, intermodulation products of various order, composed of nonlinearities of various degree, will be present in the output spectrum. Odd-order intermodulation products are a function of the source/load impedance at the envelope frequency due to the low-frequency even-degree nonlinearity. Consequently, the envelope impedance of the bias-network directly impacts the linearity/efficiency tradeoff of the transistor. Although the importance of the envelope termination is well know, very little has been done to investigate empirical large-signal methods of optimization [12].

To investigate the impact of the envelope-termination, a novel load-pull method is proposed. The present method is based on a semi-automatic variable impedance network in series with each of the two bias networks for the transistor. Each network is capable of presenting an arbitrary impedance at the envelope frequency, while being simultaneously de-coupled from the impedance at the fundamental and harmonics. Results are presented for a 53 mm Si LDMOS transistor operating at 850 MHz and 3.4 V under IS-95 excitation [3]. Results show that an optimal termination can be empirically determined by the present system to minimize ACPR asymmetry, thus improving the linearity/efficiency performance of the transistor. This result is in contrast to the commonly held belief that the envelope-termination must be approximately zero. It is also shown that some asymmetry may be desirable in order to minimize ACPR near maximum output power, thereby optimizing the linearity/efficiency tradeoff.

II. MEASURED RESULTS AND DISCUSSION

The present implementation of the proposed envelope-termination load-pull system is designed for 1 MHz, which is the approximate envelope frequency for the IS-95 standard. Figure 1 shows the envelope-termination load-impedance domain used for this work. The variable impedance network is semi-automated and fully de-coupled from the fundamental and harmonic terminations.

A standard load-pull was performed first to identify the optimal source and load impedances for best simultaneous linearity and efficiency. Following this, swept power data was recorded at each of the impedances shown in Figure 1. The device was characterized at 850 MHz with a bias of 3.4 V and 4 mA/mm (Class AB). A return loss of better than -10 dB was maintained over the load-pull domain.

Figure 2 compares transducer gain versus load power for each of the several states. Note that the impact of envelope termination is nearly insignificant in the back-off region, as expected. In the compression region, however, significant changes are observed for different envelope terminations. Load states 5 and 6 exhibit approximately a 3 dB to 4 dB increase in the modulated 1 dB compression point of the transistor, resulting in drastically improved linearity/efficiency performance.

Figure 3 shows the difference in upper and lower ACPR versus load power for each of the envelope termination load states of Figure 1. The envelope termination impact on ACPR asymmetry is clearly evident here. Certain envelope-termination load-states can be chosen which minimize ACPR asymmetry and simultaneously reduce upper and lower ACPR. Using this criterion shows that load-state 2 is optimal. Note that this load state is not zero, nor is it real-valued, as is the common practice for bias network design. Figure 3 also shows that in the asymptotic limits of operation that the envelope termination has no effect, as expected.

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Figure 4 shows PAE versus ACPR. The required average output power of 28 dBm is indicated by the asterisk symbol. These results show that depending on where the transistor is required to deliver maximum power that some asymmetry may be desirable since the overall efficiency/linearity performance may be improved. In this case, load-state 5 provided the best overall efficiency for the required ACPR specification of -30 dBc. This was achieved at the expense of some asymmetry in the region immediately below maximum required output power. Note also that load-state 5 provides over a 10% point improvement in PAE over the worst-case envelope-termination, for a constant load power.

III. SIMPLIFIED VOLTERRA SERIES ANALYSIS OF COMPLEX IM

A simplified Volterra series analysis, previously presented, can be used to qualitatively describe how the envelope termination influences ACPR [13]. This analysis can also be used to qualitatively describe the mechanism for asymmetry in upper and lower ACPR.

Consider a quasi-linear system excited by a two-tone signal. The output spectra will consist of linear combinations of the two input spectral components. In general, even degree nonlinearities will contribute to odd-order nonlinearity. Up to order $N = 3$, the normalized upper and lower in-band IM_3 intermodulation products are expressed as

$$V_{IM3}^{Upper} = \tfrac{1}{2}\mathrm{real}\left\{\begin{array}{l} H_2(\omega_2-\omega_1)H_1(\omega_2)\exp[j(\omega_2-\omega_1)]\exp[j\omega_2]+ \\ H_2(2\omega_2)H_1(-\omega_1)\exp[j2\omega_2]\exp[-j\omega_1]+ \\ H_3(2\omega_2-\omega_1)\exp[j(2\omega_2-\omega_1)] \end{array}\right\} \quad (1a)$$

$$V_{IM3}^{Lower} = \tfrac{1}{2}\mathrm{real}\left\{\begin{array}{l} H_2^*(\omega_2-\omega_1)H_1(\omega_1)\exp[j(\omega_1-\omega_2)]\exp[j\omega_1]+ \\ H_2(2\omega_1)H_1(-\omega_2)\exp[j2\omega_1]\exp[-j\omega_2]+ \\ H_3(2\omega_1-\omega_2)\exp[j(2\omega_1-\omega_2)] \end{array}\right\} \quad (1b)$$

where the H refer to the first-order, second-order, and third-order nonlinear transfer functions, respectively. Furthermore, (1b) has been simplified by recognizing for a general nonlinear transfer function, $H(-f) = H^*(f)$ [14]. This relationship shows that the second-order difference frequency contribution to lower IM_3 is 180° out of phase with respect to the second-order difference frequency contribution to upper IM_3. Noting that the nonlinear transfer functions (1a) and (1b) are functions of bias and power, as well as frequency, we see that there exists the possibility for asymmetry in IM_3 due to the anti-parallel direction of the second-order difference frequency term.

This idea is demonstrated with a vector intermodulation diagram, as illustrated in Figure 5. Each of the three components of (1a) and (1b), respectively, are shown qualitatively. The effect of the second-order difference frequency term's phase reversal on the magnitude of the aggregate IM_3 (i.e. as measured on a spectrum analyzer) is evident by the relative difference in magnitude of the lower and upper aggregate IM_3 vectors. The magnitude and phase of the second-order difference term is directly related to the impedance at the difference frequency, thus allowing vector optimization of its value to optimize IM and/or mitigate asymmetry. The extension to ACPR is simple, though higher-order effects may also require consideration [5]. It is important to realize that since each of the individual terms of (1a) and (1b) are complex, merely setting to zero the envelope termination impedance does not guarantee that IM_3 is minimized. Some impedance may exist where the second-order difference term effectively cancels the remaining terms, thus optimally minimizing IM_3.

IV. CONCLUSION

A novel load-pull technique has been proposed to investigate the impact of envelope termination on the linearity/efficiency tradeoff of RF/microwave power transistors. The proposed method represents a further refinement in the state-of-the-art of load-pull, and can be used to mitigate the ACPR asymmetry problem that inhibits the linearity/efficiency tradeoff vital to transistors used in portable wireless applications. It was illustrated that the common practice of setting the envelope termination to approximately zero is not necessarily optimal. Instead, an alternative, possibly complex impedance can improve the 1 dB compression point significantly. It was also shown that some asymmetry may be desirable. A simplified Volterra series analysis was used to illustrate vector IM cancellation. The proposed method will also find application for transistors used in infrastructure applications and for model verification applications.

V. REFERENCES

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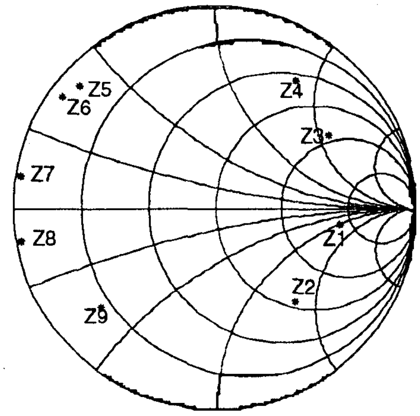

Figure 1. Envelope load states, which are the impedances presented to the device at 1 MHz. Data is normalized to $Z_o = 10\Omega$

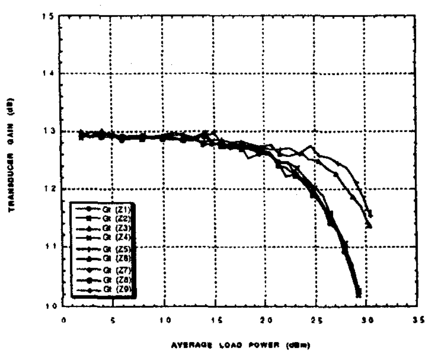

Figure 2. Transducer gain versus average load power.

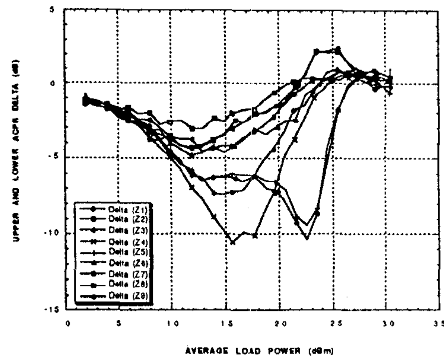

Figure 3. Delta in upper and lower ACPR v. average load power.

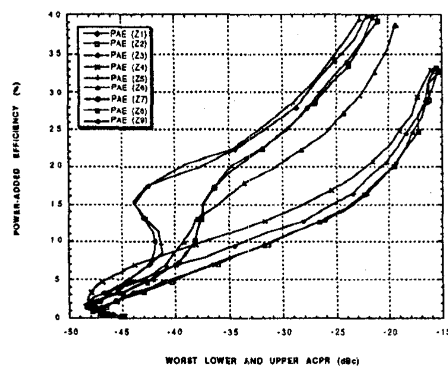

Figure 4. PAE v. worst-case ACPR. Asterisk indicates 28 dBm average load power.

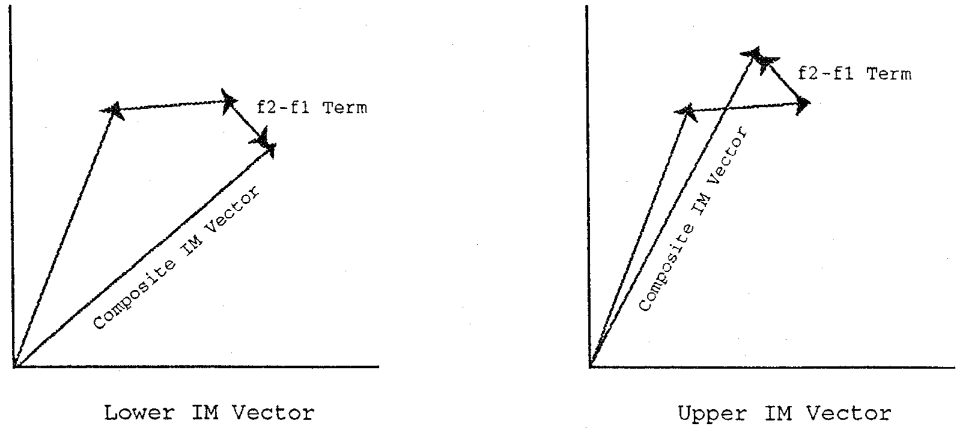

Figure 5. Vector intermodulation diagram showing the effect of the second-order difference frequency phase on total intermodulation. the phase reversal changes the overall IM magnitude for each IM response.