Hierarchical Simulation of High Speed Digital Interconnects Using a Packaging Simulator

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Abstract

An hierarchical strategy is presented which permits the tradeoff of modeling and simulation accuracy with simulation speed in the simulation of high speed signals on interconnects in multichip modules and printed circuit boards. Using a point modeling paradigm for discontinuities and impulse response thresholding a smooth transition is achieved between delay modeling and full circuit simulation.

1 Introduction

The high speed performance of most digital systems is now limited by distributed discontinuities and transmission line effects of packaging and interconnects, and not by the switching speed of semiconductor devices. Monolithic IC's designers would like to be able to simulate an entire populated MCM or PCB including transmission line effects, packaging parasitics and the circuits on the IC's themselves. It is not possible to do this at this time because of the excessive computation involved. Instead a reasonable alternative is to simulate the interconnect with behavioral models for the the drivers and receivers on the ICs. The problem is still very large and a strategy must be developed for handling the very complex interrelated system. In this paper we present a hierarchical simulation and modeling approach which has been incorporated in a specialised packaging simulator.

The fundamental difficulty encountered in integrating transmission line simulation in a transient circuit simulator arises because circuits containing nonlinear devices or time dependent characteristics must be characterised in the time domain while transmission lines with loss, dispersion, and interconnect discontinuities are best simulated in the frequency domain. Many people are working on aspects of electronic packaging simulation but for the most part the work amounts to developing techniques for modeling various transmission line structures and developing simulation strategies that can be incorporated in SPICE-like simulators. The distinguishing features of the work presented here is the hierarchical modeling and simulation paradigm.

Novel aspects of the work include:

1. Hierarchical representation of an interconnect network permitting various levels of complexity of interconnect simulation. This provides a tradeoff of simulation accuracy and simulation time.

2. A point modeling paradigm is developed for discontinuities.

3. The entire linear interconnect network is modeled by first finding the Y parameters of the reduced network with external ports being the interface between the linear network and the nonlinear drivers and receivers. The network is first augmented by a network that ensures band-limited and finite time response of the network. This enables an impulse response to be obtained, without aliasing error. This impulse response is used with conventional convolution in transient analysis.

4. Impulse response thresholding is used to obtain efficient simulation by reducing the number of bins in the impulse response. In the limit with high level thresholding, there is a single bin corresponding to a delay line model of the interconnect. This leads to very efficient simulation but at the price of low accuracy. Impulse response thresholding also leads to DC offset errors in the simulated response. An algorithm will be presented to eliminate these errors.

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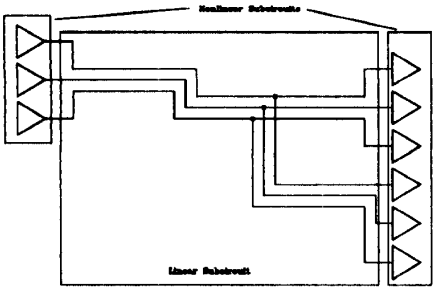

Figure 1: Partitioning of general interconnection circuit into linear and nonlinear subcircuits.

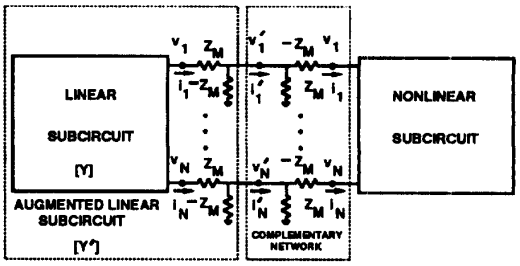

Figure 2: N port distributed network partitioned into linear and nonlinear subcircuits.

5. Drivers and receivers are incorporated as behavioral models. From the interconnect impulse response it can be determined if these are instantaneously coupled or not. If they are instantaneously decoupled, which is often the case, then the behavioral models can be solved independently.

6. A novel sparse matrix analysis technique dramatically reduces model evaluation time by using a single call to an element to evaluate the element characteristics at all frequencies. This reduces the time spent in descending the routine tree and maximises efficiency with vector computers.

The above techniques have been implemented in a specialised packaging simulator called TRANSIM.

2 Distributed Network Modeling

Considering Fig. 1, each time-domain y parameter (being the Fourier transform of the corresponding frequency-domain y parameter) is then the response of the current with respect to an impulse voltage at one of the ports of the network, i..e. $y_{ij}(t) = i_i(t)/v_j(0)$. This impulse response is developed for the entire linear distributed network and not just for individual transmission line segments. This is one of the main reasons why this implementation of convolution-based analysis is efficient. The technique has previously been described in [1].

Whenever convolution and Fourier transforms are used to interface time-domain and frequency domain analyses aliasing errors are introduced. This is of particular concern in the method described for interfacing the distributed network as aliasing effects manifest themselves as noncausal responses and convergence problems in transient analysis. These problems are eliminated in this work by using an augmentation network that ensures that the augmented network is both time-limited and frequency-limited. Time limiting is achieved by terminating each port (of the distribute network) in the augmentation network shown in 2.

3 Frequency Limited Response

When the augmentation network described above is combined with package parasitics a low pass filter results. As seen in figure 3, there is an I/O pad terminating the transmission line and a bond wire connecting the pad to the integrated circuit. This packaging structure associated with the pad and bond wire can be modeled as a simple lumped element LC model, Fig. 4

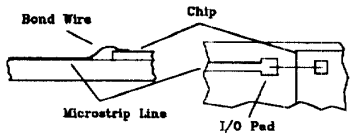

Figure 3: Chip to substrate bondwire connection

For the case of a simple microstrip line connecting two devices, the actual structure is figure 5 with the corresponding electrical model of figure 6. The admittance parameters of this new structure (both y_{11} and y_{12}) go to zero as frequency increases, Fig. 7.

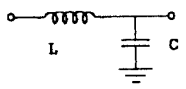

Figure 4: Lumped element model of bondwire parasitics.

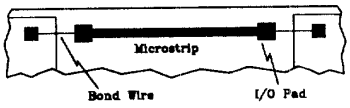

Figure 5: Simple two port interconnect

The first subcircuit contains all of the linear elements and the other contains all of the nonlinear ones. An example of this is shown in figure 8.

By using admittance parameters instead of scattering parameters and by including packaging effects, the network parameters used by TRANSIM are naturally bandlimited and don't require nonphysical filtering.

The interconnection network including the parasitic elements has a bandlimited response like that shown in figure 10. This graph shows the frequency domain admittance parameters for a simple low loss line Note that the responses of both $|y_{11}|$ and $|y_{12}|$ tend toward zero at the upper frequency end. The parasitic inductances and capacitances were 0.1nH and 0.2pF respectively.

4 Time Limited Impulse Response

While these packaging parasitics' bandlimit the frequency domain admittance parameters and minimize the aliasing problem the problem of long impulse response functions remains. With the network shown in figure 9 an augmentation network like that in figure 11 can be used to reduce the impulse response length. With the addition of the augmentation network the impulse response of the original network augmented by the augmentation network is time limited. With this additional impedance connected to the ends of the

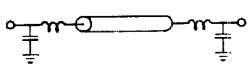

Figure 6: Simple interconnect with parasitics

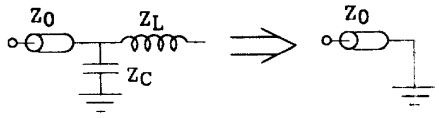

Figure 7: Effect of parasitics at high frequencies.

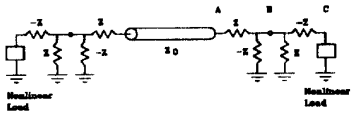

Figure 8: New augmentation networks applied to simple interconnect circuit.

transmission line a short circuit applied to one end results in the impedance being connected to ground and in the case of a perfect match ($Z = Z_0$) no reflection occurs and the impulse response length is minimized.

5 Discontinuity Characterization

Discontinuities in nets generally appear as localized discontinuities with connecting transmission lines. Using the via of Fig. 12a as an example, the conventional CAD model includes sections of the connecting transmission lines (Fig. 12b) in which the ends account for most of the effect of a CAD via model. Including the transmission line sections guarantees good agreement between measured and calculated results. In layout extraction the concept of a net incorporating a via is to route from point A to point B, change metalisation layers at point B, and then to route to point C. The conceptualization is not to route a line from point A to the reference plane of the via, then insert a spatially

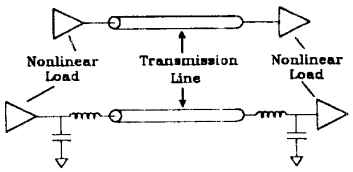

Figure 9: Interconnect circuit with addition of simple lumped element parasitic model.

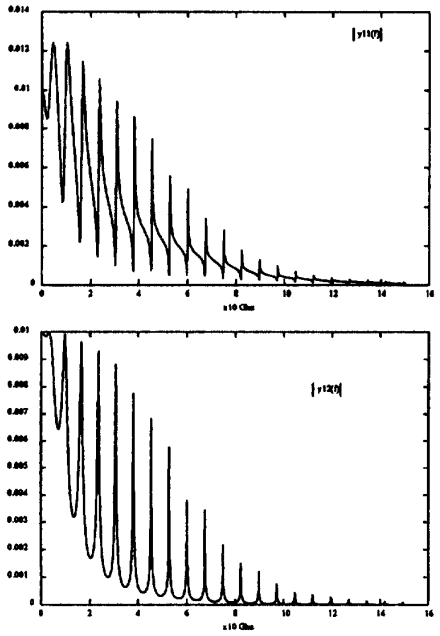

Figure 10: Naturally bandlimited admittance parameters with packaging parasitics included.

Figure 11: Single element augmentation network.

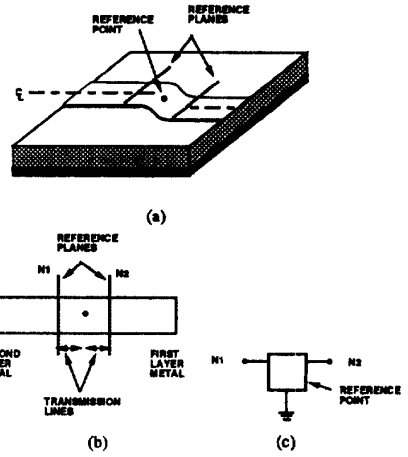

Figure 12: A conformal via discontinuity: (a) view of measurement structure showing via reference planes for a model of the via; (b) conventional via model; and (c) point discontinuity model.

distributed element, and then continue routing from the other reference plane of the via. In a standard measurement set the parameters of a point discontinuity are measured anyway. It is far more reasonable to model the structure as a point discontinuity as in Fig. 12c.

6 Thresholding

One of the drawbacks to convolution techniques has always been the large number of floating point operations used for each time step and for most kinds of transfer functions there is no way around this fact. However with a physically based impulse response as used here, small contributions to the impulse can be neglected with the effect of a resolution reduction in the calculated transient response. The idea behind thresholding is to select some relative value (v_r, $0 \leq v_r < 1$) such that any points in the impulse response who's absolute value is greater than this amount are kept for use in the convolution and any points falling below this value are discarded. Mathematically this can be expressed as:

$$y'(t) = y(t), |y(t)| \geq \epsilon \quad (1)$$
$$= 0, |y(t)| < \epsilon \quad (2)$$

where $y'(t)$ is the new impulse response and ϵ is related to the relative threshold level v_r by $\epsilon = v_r y_{\max}(t)$.

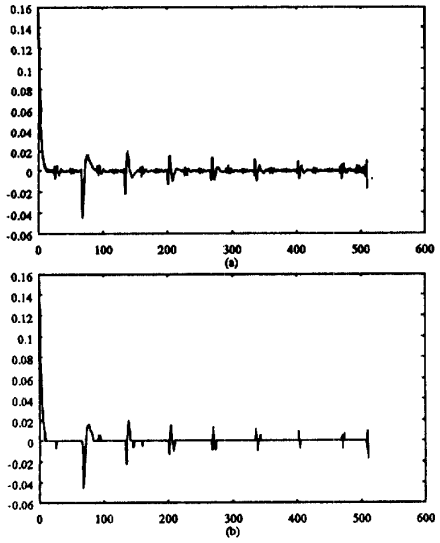

Figure 13: Example of typical impulse response, y(t), original (a) and with thresholding.

with $y_{max}(t)$ being the maximum absolute value of $y(t)$.

An example of a typical impulse response is shown in Figure 13. Thresholding dramatically reduces the number of impulse response bins but it can lead to significant DC errors as shown in Fig. 14. If these errors are not removed convergence problems can result. Indeed DC errors can exist even without thresholding due to the finite discretization of the impulse response. These errors can be removed using algorithms presented in [2].

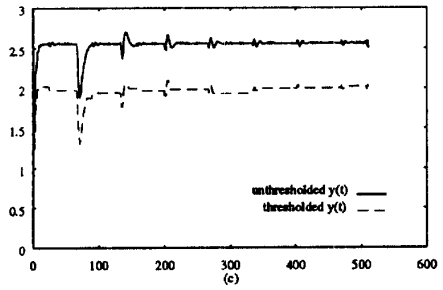

Figure 14: Unit step convolved with the unthresholded and thresholded impulse response.

7 Results

Clock Distribution Circuit

In the clock distribution network shown in figure 15, the clock driver (U1) drives a distribution network consisting of two rows of devices. This circuit demonstrates microstrip tee and bend models along with the planar transmission line and nonlinear loads. The output voltages for selected external ports are shown in figure 16 (V_1 and V_8) for both the SPICE and TRANSIM simulations.

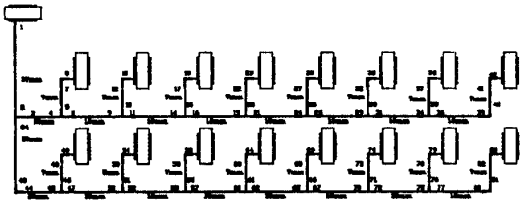

Figure 15: Clock distribution circuit.

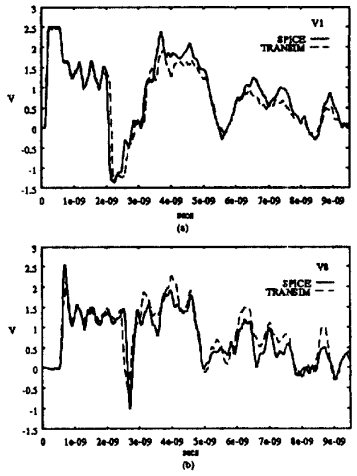

Figure 16: Waveforms at ports 1 and 8 for clock distribution circuit.

SPICE (both 3E2 and a commercial version) had convergence problems on this and most complicated interconnect circuits. Convergence was eventually obtained after several runs tweaking some parameters (including subtle variations in line lengths) to obtain convergence. Execution times for various runs

Table 1: Comparison of execution times for SPICE 3e2 and TRANSIM. The drivers and receivers were modeled as behavioral models in TRANSIM and as linear loads in SPICE 3e2 since this type of nonlinear models is not supported.

Description	SPICE 3e2	TRANSIM No Threshold	TRANSIM 95% Threshold
Single Microstrip	1.8s	16s	3s
Single Microstrip w/bends	86.7s	23s	12s
Clock Distrib.	3637s (60.5min)	2219s (37min)	1369s (23min)

are shown in table 1. The three timing information columns show execution speed for SPICE 3E2, TRANSIM without thresholding, and TRANSIM with thresholding.

Coupled Lines

The coupled line example shown in figure 17 represents a section of data bus connecting two integrated circuits (represented by the sets of gates). The resulting waveforms are illustrated in figures 18 and 19.

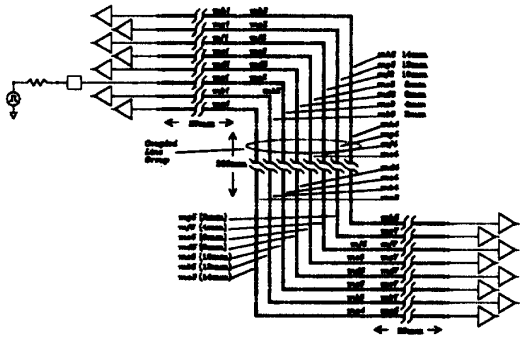

Figure 17: Demonstration circuit, data bus.

8 Conclusion

A method for modeling arbitrarily complex transmission line networks in a transient circuit simula-

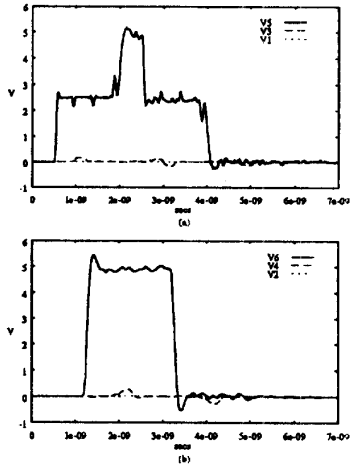

Figure 18: Near (a) and far (b) end bus waveforms showing culprit and victim lines.

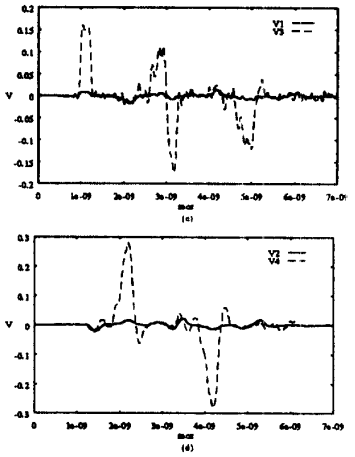

Figure 19: Near (c) and far (d) end bus waveforms, victim lines only.

tor was presented. The model uses a time-domain Green's function derived from scattering parameter descriptions of the transmission line circuit. Implementation of the model in a transient circuit simulator was described and it was experimentally verified. A smooth tradeoff between accuracy and simulation speed is achieved by varying the impulse response threshold.

References

[1] M.S. Basel, M.B. Steer, P.D. Franson and D. Winkelstein, "High Speed Digital System Simulation using Frequency Dependent Transmission Line Network Modeling," *1991 IEEE MTT-S International Microwave Symposium Digest*, pp. 987-990, June 1991.

[2] M.S. Basel, *Simulation of High Speed Digital Circuit Interconnection Networks*, Ph.D. Dissertation, North Carolina State University, 1993.