A Signal Integrity Advisor for Automated Packaging Design

Slobodan Simovich, Sharad Mehrotra, Paul Franzon, and Michael Steer,
PICOLAB
Department of Electrical and Computer Engineering,
North Carolina State University.

Zaki Rakib and Garrett Simpson
Cadence Design Systems.

Abstract

A new methology is presented in which the signal integrity engineer and the design engineer interact with automation tools to produce a PCB or MCM layout. The focus is on how the signal integrity engineer uses these tools for greatest success.

1 Introduction

In this paper we describe a new methodology to the problem of laying out Printed Circuit Boards and Multichip Modules so that timing and reflection noise requirements are met.[1] [2] The core tool is called the Signal Integrity Advisor (SIA). In many respects, the concepts embodied within SIA are an automated version of the highly succesfull signal integrity management approach practiced for many years at IBM [1] and elsewhere. As well as outlining the overal methodology supported by SIA, this paper focuses on how the signal integrity engineer must work with SIA in order to maximize its effectiveness.

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[2]The authors can be reached at Department of Electrical and Computer Engineering, Box 7911, North Carolina State University, Raleigh, NC 27695-7911. Contact: Paul Franzon, Ph. (919) 515-7351, Fax. (919) 515-7382, and Cadence Design Systems, 2655 Seely Rd., MS 6B1, San Jose, CA 95134, Contact: Zaki Rakib, Ph. (408) 894-2278, Fax. (408) 894-2299

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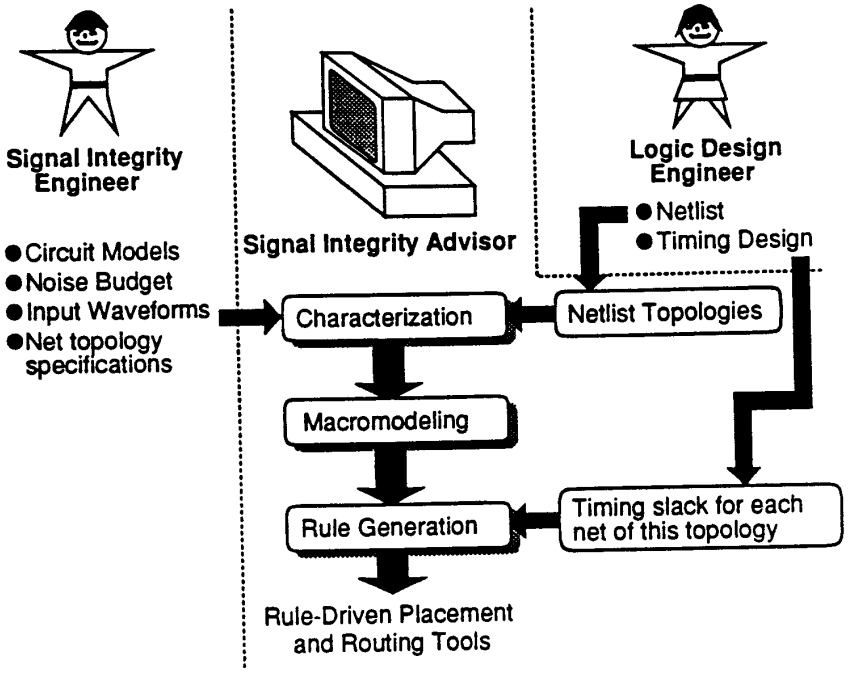

Figure 1: Design flow in the methodology implemented in the Signal Integrity Advisor.

2 Design Flow

The overall design flow within SIA is shown in Figure 1. For each particular technology combination, the signal integrity engineer specifies the circuit models for the drivers, receivers and interconnect structures. Worst and best case models can be specified if desired, at the expense of an increase in SIA run time. Models specifying simultaneously switching circuits can be specified if desired. The Signal Integrity (SI) engineer also specifies the typical input waveforms for the drivers, indicating the maximum repetition rate, and either specifies a typical data sequence or requests the generation of a pseudo-random sequence. The noise budget is also specified.

Meanwhile the logic designer supplies the netlist file to SIA. From the netlist file, SIA extracts all of the unique connectivities, e.g. all nets with the same type and number of driver(s) and receiver(s). A typical design has 10-30 unique connectivities.

The SI engineer has to specify what topology/ies are available for each connectivity (defaults are available). For example, a one-driver, two-receiver net can be connected as a daisy chain, as a near-end cluster, or as a far-end cluster [1]. The SI engineer must then specify the minimum and maximum lengths on the branches and stubs within the nets (or accept defaults). Any reasonable length can be specified as the operation of SIA is insensitive to this level of detail. Maximum and minimum via counts can also be specified, if considered electrically important.

The automatic procedures coded in SIA then take over. First, SIA characterizes the

electrical responses of each topology over the range of lengths, via counts, etc. specified. Responses characterized include 50% delay, undershoot, overshoots, metastates (or porches) on the transitions, rise and fall times, and settling delay (delay until the signal is stable enough for latching). The techniques used in the characterization phase are presented in references [2][4].

The macromodeling step converts the characterizations to a piecewise linear equation. Upper and lower bounds are fitted, instead of a mean value, so that the resulting designs are guaranteed safe. One approach to macromodeling is presented in reference [3]. However, a faster, but simpler, approach is used in SIA.

In the final step, the wiring rules (allowed length ranges) are generated for each net in the design. To generate the wiring rules, the allowed delay for each net is automatically extracted using a timing verifier. First incident switching criteria are used for clock and clock-like nets and either settling delay or first incident switching criteria used for data nets.

3 Discussion

The most difficult tasks in this methodology are determining the appropriate circuit models and managing the characterization step. Faster run times will be achieved if the signal integrity engineer does not specify huge length ranges for each branch and stub and controls the number of independant variables. For example, a 8 load daisy chain has 16 dimensions, 8 branches and 8 stubs. The characterization step will be faster if the engineer keeps the stub lengths short and treats all the stub lengths as one variable, reducing the dimensionality down to 9 variables. Additional physical insight can be used to control run-time and the degree of conservatism of the results.

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