A Simple Method for Noise Tolerance Characterization of Digital Circuits

Slobodan Simovich, Paul Franzon, Michael Steer
Department of Electrical and Computer Engineering
North Carolina State University
Raleigh, North Carolina 27695-7911

Abstract

A new method for characterizing dynamic noise tolerance of digital circuits is discussed. In this method noise impulses are characterized by their energy, voltage and width. The method is intended for use in simulation-based noise analysis and design of receiver circuits in digital systems.

1 Introduction

Noise tolerance is the term most commonly used to describe the ability of logic circuits to operate correctly in the presence of noise[1]. The concept of noise margin is used to characterize that ability. There is no unique definition of noise tolerance, and therefore, there is no "best" method for its characterization. One common notion among researchers is that different types of noise require different characterization methods [7][6][2]. Conventional approaches for characterizing noise in digital circuits distinguish between two types of noise - static noise and dynamic noise, depending on the rate at which the noise signal changes. Accordingly, static and dynamic noise tolerance and margins are defined [7].

The static noise margin approach assumes that the width of the noise impulse at the observed point in the circuit is infinite, so only the voltage amplitude of an impulse is of interest. Therefore, static noise margins are given in terms of allowed voltage ranges which guarantee correct operation under certain assumptions.

A general definition of the static noise margins and static noise tolerance of digital circuits have been an object of extensive investigation among researchers. Besides the conventional "unity slope" approach, there are a number of different definitions of the worst-case static noise margins [1][7][10][8][9]. Most of those definitions are proven to be equivalent under certain assumptions [5].

In contrast to the steady voltage levels, noise in digital circuits may also appear in the form of spikes. This is especially true in the case of off-chip circuitry where large spikes can appear on both, input terminals (crosstalk) and power/ground terminals (simultaneous switching noise). Accordingly, dynamic noise margins are defined. In the case of dynamic noise margins, not only the voltage amplitude of an impulse is considered, but also its width (in time units).

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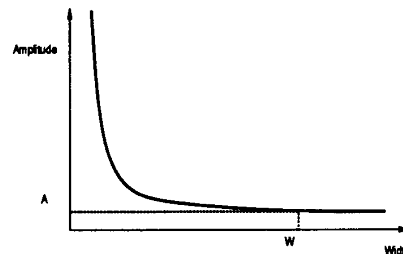

Figure 1: Noise immunity curve

As noted in [7], [6] and [2], worst-case static noise margins are a very conservative measure of noise tolerance of logic circuits. Due to a gate's finite response time, short duration impulses can have a larger amplitude than that predicted by the worst-case static noise margin and still not cause a malfunction of the system.

To characterize the aforementioned phenomenon, a curve, usually called the noise immunity curve [6][2], capturing the dependencies between the width and the amplitude of critical noise impulses can be constructed (figure 1). The region in the diagram "below" the curve represents the region of safe operation. For long duration impulses, the dynamic noise margin becomes the static noise margin. Obviously, the dynamic noise margin approach will yield less conservative, yet still accurate results than the static one.

This is one of the reasons why the concept of dynamic noise margins is very appealing to high-speed system designers. Overconstraining the electrical design space of a high-speed system, where every nanosecond/millivolt is carefully budgeted, can make the design process unnecessarily cumbersome or even impossible.

The noise immunity curve can be obtained either through simulations [2] (see figure 2) or experimental measurements [11]. This paper discusses a new simulation-based method for characterizing dynamic noise immunity based on a procedure described in [6]

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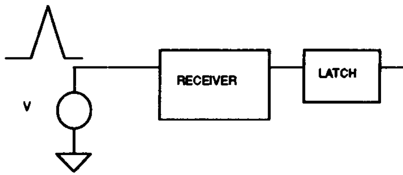

Figure 2: Circuit for obtaining noise immunity curve

and [2].

Section 2 of the paper discusses the need for a dynamic noise immunity approach. Additional reasons for utilising this approach, besides those already mentioned, are discussed. In section 3 we present the approach and discuss its implications. Section 4 concludes the paper.

2 Dynamic Noise Tolerance

The major problem with the dynamic noise margin approach, either simulation based or experimental, is its non-uniqueness. That is, the noise immunity curve depends on the conditions under which it is obtained. That concerns not only the conditions in the gate's output circuitry (e.g. loading conditions of the gate's output), but the conditions in its input circuit as well (e.g. details of the interconnect circuit connected to the input). To illustrate how the conditions in the gate's input circuit may affect the noise immunity curve, simulation experiments have been conducted. The bidirectional CMOS receiver circuit of figure 3 is considered. As the sensing latch of figure 2, an asynchronous latch composed of typical sized gates (for on-chip logic circuitry) is used. The latch is designed so that it is less immune to noise than the receiving circuit. Standard MCNC (Microelectronics Center of North Carolina) 1.25 micron CMOS process parameters are assumed. Simulations are performed using the SPICE-like simulator CaZm [3].

A standard simulation-based procedure for obtaining the noise immunity curve involves applying impulses of different width and amplitude to the receiver's input and observing the output of the latch (see figure 2) [6][2]. Points on the curve in the amplitude-versus-width space of figure 1 are determined by the moments when the latch changes state (e.g. from initial low to high). These points correspond to the cases where the disturbance at the input propagates through the on-chip circuitry (represented by the latch), causing the on-chip logic to enter an erroneous state. The width of the impulse is measured at the 50% points of the impulse.

However, the amplitude and width of an impulse do not describe noise impulses completely. In other words, impulses of different shape may have the same amplitude and width, as shown in figure 4, and yet cause different switching events.

The shape of a noise impulse depends on the conditions in the receiver's input circuit. These conditions are determined by the numerous factors: interconnect characteristics, characteristics of the driver, chip at-

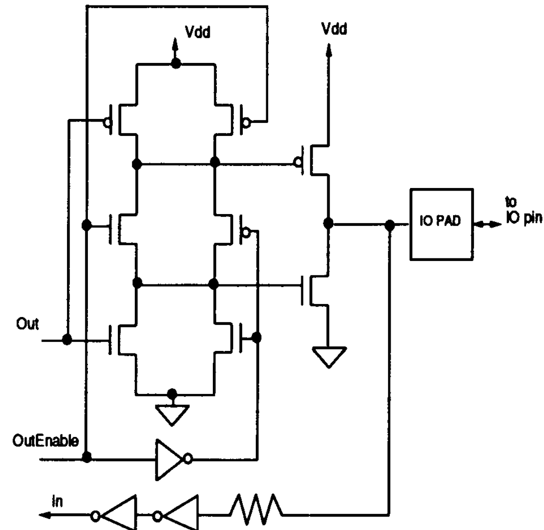

Figure 3: Bidirectional I/O pad circuitry

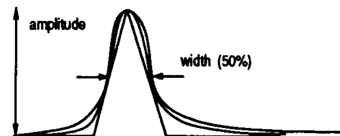

Figure 4: Different impulses of the same amplitude and width

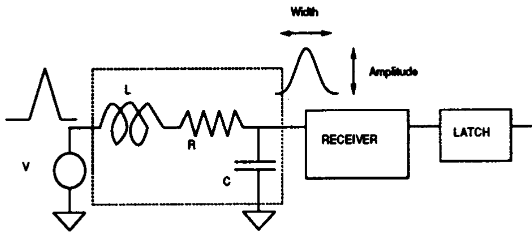

Figure 5: Obtaining noise immunity curve for different conditions in the input circuit

tachment and I/O pad parameters, number of neighboring receivers in the cluster (if any), etc.

The equivalent impedance "seen" by the receiver's input may be represented by the R-L-C network, as shown in figure 5. A set of simulations of the circuit of figure 5 is performed under different conditions in the receiver's input circuit, i.e. different values for R, L and C. Indeed, results show that impulses of the same amplitude and width, obtained under different input conditions, do not cause the same switching events. For example, an ideal triangular impulse of 3.23 Volts amplitude and 0.66 nanoseconds width (obtained for: R = 0, L = 0, C - omitted), will not cause the latch to switch, while the impulse of the same amplitude and width, obtained for R = 100 Ohms and C = 1pF will cause switching. Note that the dimensions of an impulse are measured at the receiver's input (not the voltage source output). Furthermore, an ideal triangular impulse's amplitude must increase to 3.37 Volts (same width) to cause switching. Obviously, different noise immunity curves will be obtained for different conditions in the input part of the test circuit.

Therefore, having only one noise immunity curve, obtained under certain test conditions, might lead to false conclusions in a general case. To avoid this, a set of noise immunity curves obtained under different test conditions could be obtained. However, problems with this solution arise at design/analysis time when the system operations are evaluated, because the system designer must know the conditions in the receiver's input circuit in order to use the corresponding curve from the previously obtained set. Instead, a better definition of noise margin is needed.

3 Noise Immunity Surface Method

To avoid aforementioned problem, we suggest a new definition of dynamic noise margin where the noise pulse is characterised by its voltage, time and energy characteristics. In this section, we first define what is meant by the energy of a noise pulse. The method used to capture the noise immunity is then presented and preliminary results briefly discussed.

3.1 Energy of An Impulse

Considering the energy of an impulse in noise tolerance analysis is discussed in [7]. There it is shown that no specific energy noise margin can be defined as a sole measure of noise tolerance of logic circuits. To overcome this problem, we consider the energy of an impulse along with voltage and timing information. We also define the noise energy as the energy consumed by the receiving gate rather than the energy delivered to the system by the noise source, as done in [7]. The energy of a noise pulse is given as:

$$E = \int_0^{Tw} u(t) i(t)\, dt,$$

where Tw is the duration of an impulse measured at the reference voltage level, $u(t)$ is the voltage measured at the observed terminal in reference to the ground terminal, and $i(t)$ is the impulse current measured at the input terminal. For practical reasons some finite threshold value above/below the reference level should be used to measure Tw.

Implementation of the noise immunity surface method is discussed next.

3.2 The Method and Implementation

The method involves conducting a set of computer experiments each performed under different conditions of the test circuit, i.e. different values for R, L and C of the input circuit (figure 5). Ranges for R, L and C should be chosen such that all the expected cases for the equivalent impedance "seen" by the input of the receiver in any future system configuration are represented.

For each particular condition of the test circuit, the same experiment is performed. The latch is initially reset. Impulses of different amplitude and width are applied to the input and the behavior of the latch is observed. Those impulses which set the latch are the "dangerous" ones. The following parameters of those impulses are observed: (a) amplitude, (b) width at the 50% points and (c) energy measured at the receiver's input terminal.

The described set of experiments will yield a noise immunity surface (figure 6). The region "above" the surface is the region of unsafe operation of the receiver. That is, the receiver is not immune to noise impulses represented by the points in the amplitude-energy-width space which fall into this region. From figure 6 it can be noted that the orthogonal projection of the noise immunity surface contours onto the amplitude-width plane represent an envelope of standard dynamic noise immunity curves obtained under different conditions.

One possible procedure for determining if the impulse is "above" the surface or not - i.e. if it is "dangerous" or not, is as follows:

1. check if the impulse has amplitude and width which falls into the "dangerous" region for all of the amplitude versus width curves of the surface.
   If yes - impulse is "dangerous",
   else,

2. check if the impulse has amplitude and width which falls into the "safe" region for all of the amplitude versus width curves of the surface.
   If yes - impulse is "safe",
   else,

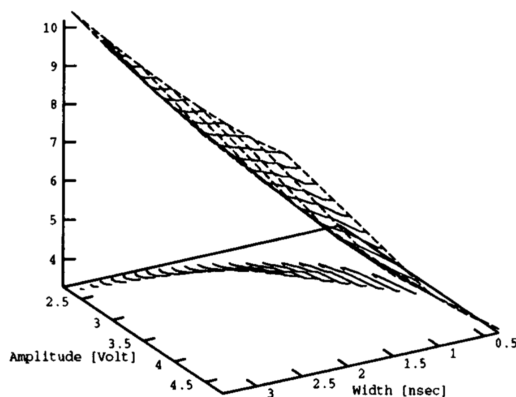

Figure 6: Noise immunity surface

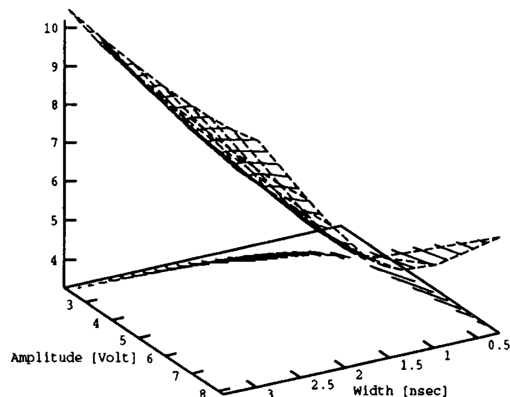

Figure 7: Noise immunity surface for diode-terminated receiver

3. check if the obtained energy value of an impulse - for a given amplitude and width, is greater than the energy value for a corresponding interpolated point on the surface.
   If yes - impulse is "dangerous"
   else - impulse is "safe".

In the same fashion it is possible to obtain dynamic noise immunity surfaces for power supply and ground noise. The described procedure concerns the noise tolerance to positive going noise impulses referenced to the ground level. The same procedure can be applied to obtain the noise immunity surface for negative going noise impulses referenced to the power supply level.

3.3 Discussion

Experiments show that the noise immunity surface is a more accurate measure of noise tolerance of logic circuits than the noise immunity curve. Simulations performed for the receiver of figure 3 show that the noise immunity curves obtained under different conditions in the receiver's input circuit vary by up to 8% in voltage values, depending on the pulse shape. That is, for two extreme test cases and fixed values of pulse width, predicted "dangerous" voltage amplitudes vary by a maximum of 8%. These variations are captured in a single noise immunity surface.

Improved noise immunity prediction of this method, in comparison to the noise immunity curve approach, is achieved at the expense of increased simulation costs in obtaining the surface and increased utilization complexity at design time. Since the noise immunity surface is obtained just *once*, and then used for all future designs, we believe that the accuracy of this method outweighs its simulation time costs. Furthermore, the use of the described method at design time is highly automatable. We have implemented this method as an integral part of a switching analysis program of the MetaSim [4], a design automation tool for simulation-based interconnect/package characterization and design.

The shape of the surface will depend on several different factors, such as logic family, receiver type, termination, etc. Although the conducted experiments shows that energy versus width dependency is almost linear (see figure 6), this is not true in the general case. For example, experiments conducted for diode-terminated receiver of figure 3 yields the noise immunity surface of figure 7. In this case, amplitude of narrow impulses which cause false switching is large enough to cause one of the diodes to conduct, thus introducing a non-linearity in the energy versus width dependency.

4 Summary and Conclusions

A new method for characterizing the dynamic noise tolerance of digital circuits is presented. In this method, we considered voltage amplitude, timing and energy of noise pulses to characterize noise immunity of receiving gates in digital systems. The method is intended for simulation-based noise analysis and design of receiver circuits in digital systems. The described noise immunity surface approach is more accurate than the conventional noise immunity curve approach.

We are focusing our future work on quantifying the differences between this approach and its alternatives. Issues, such as the impact of this approach on achieving less constrained, but still correct designs will be addressed.

Acknowledgments

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