Improving Behavioral IO Buffer Modeling Based on IBIS

Ambrish K. Varma, Michael Steer, *Fellow, IEEE*, and Paul D. Franzon, *Fellow, IEEE*

***Abstract*—High level behavioral modeling is widely used in lieu of low level transistor models to ascertain the behavior of input/output (IO) drivers and receivers. The input output buffer information specification (IBIS) is one of the most widely used methodologies to model IO drivers as it satisfies the basic requirements of a behavioral model such as IP protection, simple structure, fast simulation time, and reasonable accuracy. As driver technology gets increasingly complicated and rise time of input signal gets increasingly smaller, important considerations such as simultaneous switching noise (SSN) becomes a major consideration when simulating multiple IO drivers in the integrated circuit. Unfortunately, IBIS falls short of becoming a complete IO behavioral model when simulating for SSN. This paper addresses the problem by assessing what is missing in IBIS. A method is presented for compensating for the missing information by complimenting the IBIS model with a black box that is simulator independent, without compromising with the speed that IBIS enjoys over the transistor models.**

***Index Terms*—Behavioral modeling, gate modulation effect, input output buffer information specification (IBIS), input/output (IO) buffer modeling, simultaneous switching noise (SSN).**

I. Introduction

With shorter rise times and fast and advanced drivers, simultaneous switching noise (SSN) simulations have become imperative in a system level test with behavioral models for input/output (IO) driver. Input output buffer information specification (IBIS) models are known to have an issue with their inability to simulate SSN in a network [1]. IBIS models are incapable of accounting for two distinct phenomena when compared with transistor models. Transistor models of IO buffers include information such as predriver current and crossbar current [2], [3] that IBIS models lack. The other area where IBIS models fall short of the transistor models is when the local power and ground signals are bouncing, thereby affecting the gate voltage of the pull-up and pull-down devices [4]. This paper addresses both these deficiencies of IBIS by introducing a black-box that can be used in conjunction with IBIS. The black-box consists of SPICE primitive constructs and can be used with any simulator of choice. This allows the model maker to introduce SSN modeling capability for their models without changing anything in the IBIS model and without waiting for any fix in the simulator as a result of a change in the IBIS specification. This enhancement of behavioral modeling using IBIS gives the user a physical circuit based model that they can understand and modify if need be unlike other purely mathematical behavioral models [5]–[7] that are abstract, hence hard to fix should a bug be found.

This paper has been organized as follows. Section II discusses the theory behind the correction factors that are included in the black-box. Section III discusses the process of creating the black-box. Section IV discusses an improvement over the methodology discussed in Section III. Section V discusses the metrics that are used in this paper to quantify the improvement in accuracy with the proposed methodology. Section VI includes three test cases using two drivers that assess the accuracy of the resulting model when compared with plain IBIS models and transistor level models of the IO drivers. Section VII presents an analysis of the results achieved after the tests. Section VIII concludes the paper. All simulations in this paper are performed in HSPICE on a SUN SPARC Sun Blade 100.

II. IBIS Deficiencies

Behavioral models of IO drivers such as IBIS are a high level description of the drivers with the intention of accurately representing the important and useful aspects of the driver. This results in faster and cost effective simulations. It is, however, easy to oversimplify the behavior model rendering it inaccurate and incomplete. This section looks at some of the issues in the IBIS model that are overlooked during model construction when comparing it with the transistor level model of an IO driver.

A. Predriver, Crossbar, and Termination Currents

Transistor models of IO drivers consist of more than just the pull-up and pull-down devices. Power distribution network circuits, predriver circuits and control circuits are primary blocks of circuit that are included in the IO drivers other than the pull-up and pull-down devices. On the other hand, IBIS models contain voltage-current (VI) and voltage-time (VT) tables to describe the pull-up, pull-down, and clamp devices along with some package information. As such, there is a lack of accurate current information in an IBIS model resulting in driver performance that is inconsistent when compared to the transistor netlist simulation. Fig. 1 shows the output current of a rising edge of an IO driver for both transistor level netlist and IBIS model. The zoomed part of the figure shows that the current profile in the transistor level model starts almost

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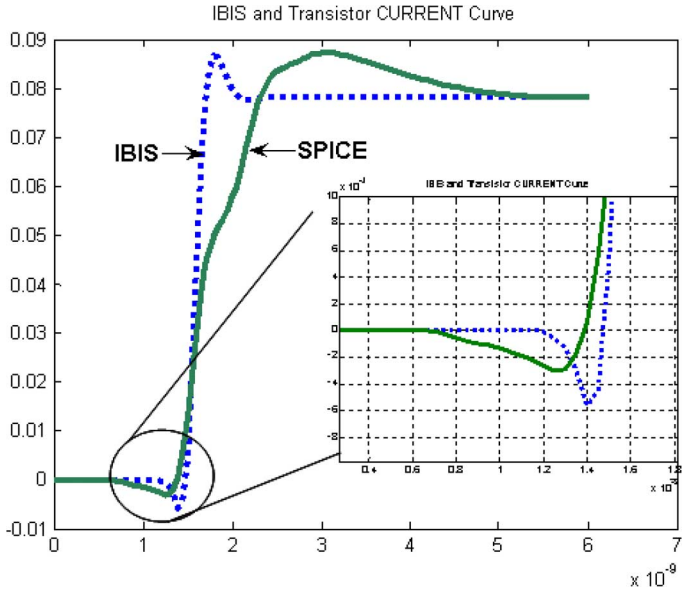

Fig. 1. Rising edge current at the output pin Vs Time of an IO driver demonstrating the lack of predriver current in IBIS models (broken line) when compared to the transistor model (solid line).

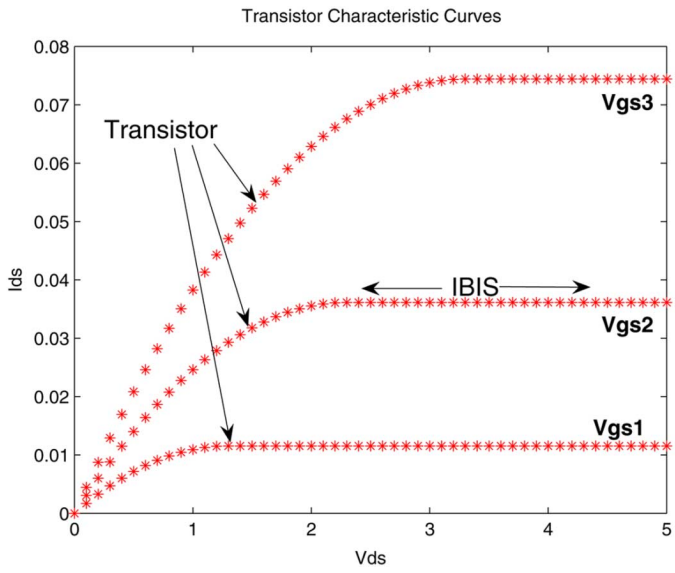

Fig. 2. Ids Vs Vds Characteristic curves for NMOS transistors. While transistor level models jump from one curve to the other with a change in Vgs, IBIS models confine to one curve (in this case, at Vgs2).

500 ps before the current in the IBIS model demonstrating the fact that there is some missing current in the IBIS model and that the missing current is related to the activity in the driver before the pull-up device (in this case) becomes active. Similarly, the leakage (crossbar) current through the pull-up and pull-down devices during switching and the termination current at the output of the driver are important questions that are not completely answered in an IBIS model.

B. Gate Modulation Effect

The power and ground bounce due to SSN affects the gate voltage of the pull-up and pull-down devices in an IO driver. This gate voltage fluctuation should result in a variation of current flowing through the pull-up and pull-down devices-thereby affecting the current flow in the overall driver. IBIS models do not reflect this.

To illustrate the difference between the behaviors of transistor and IBIS models, the characteristic (Ids Vs Vds) curves of an NMOS device is observed. Fig. 2 shows Ids curves for different Vgs values (figure shows three characteristic curves for Vgs1, Vgs2, and Vgs3 for demonstration purpose) as per (3) which is the spice level one MOS transistor model. This makes the transistor model current a function of both Vgs and Vds (2). When the power and ground sources bounces, Vgs values varies and the transistor models adapt by making the device stronger or weaker (by shifting vertically on the characteristic curves). On the other hand, each VI table in the IBIS models (pull-up, pull-down, power-clamp, and ground-clamp) represents only one of the characteristic curves shown in Fig. 2. As such a fluctuation in the power and ground source does not produce the same effect in an IBIS model (1). This effect is also known as the *gate modulation effect*

$$I_{ds(\mathrm{IBIS})} = f(V_{ds}) \tag{1}$$

$$I_{ds(\mathrm{trans})} = f(V_{gs}, V_{ds}) \tag{2}$$

$$I_{ds} = \mu_n C_{ox} \frac{W}{L}[(V_{gs} - V_{th})V_{ds} - \frac{1}{2}V_{ds}^2](1 + \lambda V_{ds}). \tag{3}$$

Fig. 3 shows the effect of gate modulation effect by increasing the number of drivers between transistor level drivers and IBIS model drivers, both switching from low to high. In the transistor level model [Fig. 3(a)], the output voltage deteriorates with the increasing drivers whereas the IBIS model circuit [Fig. 3(b)] shows relatively low degradation of the output signal thereby not allowing for a realistic simulation in the circuit with the IBIS model.

When these two problems in IBIS are combined, accurate simulations for simultaneous switching noise become a challenging prospect.

III. Black-Box Modeling of Error Function

The thesis behind this work is that without the necessity of changing IBIS models and the simulators that handle them, the model user can use the macro models for simultaneous switching noise simulations as well as any other complex system level simulations. This is done by complimenting the IBIS model with a black-box that contains the error function between the original IBIS and the transistor netlist model as shown in Fig. 4 (right). The black box is generated automatically using a MATLAB script for both the issues discussed in Section II. The error function contains spice primitives making it compatible with most simulators.

Previous solutions have tried to address the problem of insufficient representation of the extra current in IBIS model and have proposed methodologies that have extracted the signatures of the missing current at the VDD node-but have demonstrated the usefulness in a restricted environment [2]. These current signatures are obtained at a certain power/ground voltage. However, with varying voltage at the power and ground rails, current signature would change, thus rendering the correction in-

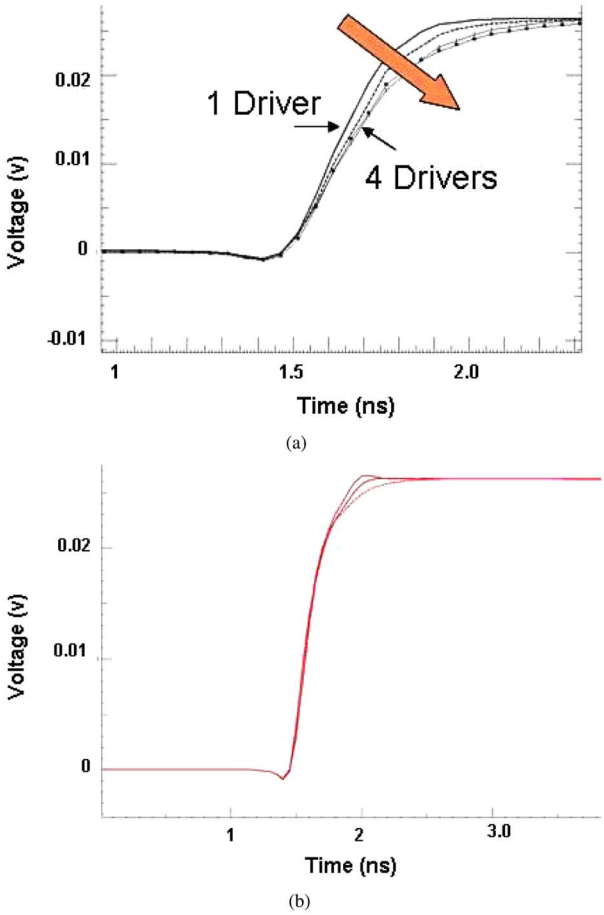

Fig. 3. Effect of modulation of the gate voltage as a result of the power and ground bounce. With the increase in number of drivers, SSN deteriorates, affecting the voltage response at the output pin in (a) transistor level models. Similar circuit does not elicit same response in circuits with IBIS level models (b).

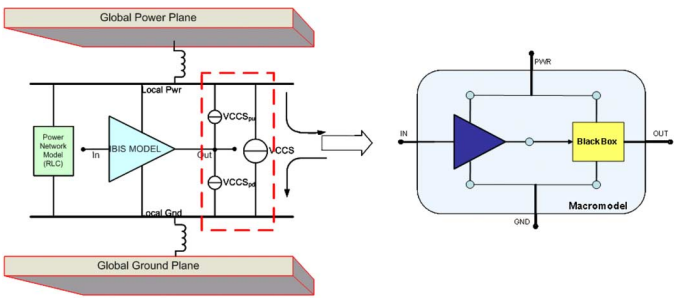

Fig. 4. Black-box modeling approach. Breakdown of various components of the proposed macro-model (within the box with dashed lines), (left) and high level overview of the macro model with the IBIS element and the blackbox (right).

accurate. The macro-modeling methodology, described in this paper, allows for a more robust solution where the correction is a function of the variation in the voltage levels at the power and ground pins—thus useful even when the supply rails are affected by SSN.

Fig. 4 (left) shows the various components of the macro model that is being proposed in this paper while Fig. 4 (right) is a high level overview of the macro model. The following sections describe the methodology of obtaining the parameters of the black-box for both the deficiencies discussed in Section II.

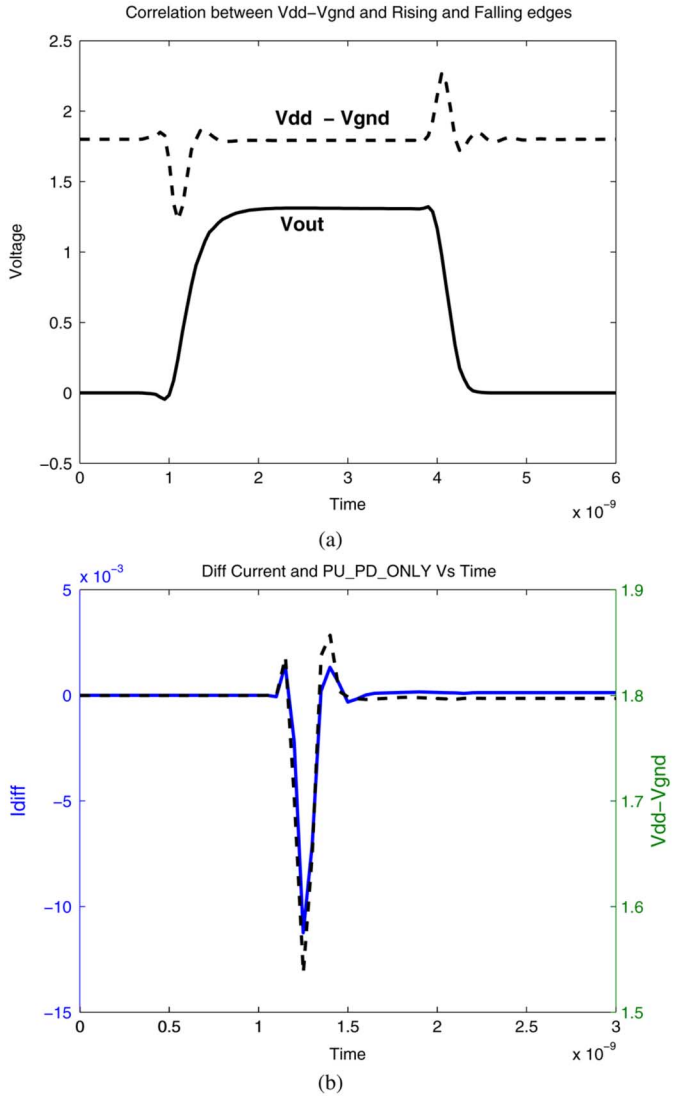

Fig. 5. Power droop and ground bounce correlate with the switching of the buffer (a). There is a high correlation between the difference in current (solid line) at the Vdd pin between the transistor level model and the behavioral (IBIS) model and V(Pwr-Gnd) (broken line) (b).

A. *Predriver Current Error Correction*

The crossbar current along with all the other currents that is absent from the IBIS model can be estimated by comparing two similar circuits-one with IBIS model and the other with its equivalent transistor model. The difference current is then compared to the difference in the voltage levels between the Vdd and Vgnd ($\mathrm{Vdiff} = \mathrm{Vdd} - \mathrm{Vgnd}$). It is observed that this difference in voltage level only occurs during a transition in the voltage level at the buffer output [Fig. 5(a)]. As the buffer switches, it draws (or sinks) current from or to the power supply. Fast changing current passing through the package parasitics generate a drop in the power signal and a bounce in the ground signal [8], [9].

When the difference current at the Vdd pin (I_{diff}) is compared against V_{diff}, a correlation is observed [Fig. 5(b)] between the difference in current values of the transistor level model and the behavioral (IBIS) model and the difference of voltage levels in the power and ground pins of the IBIS model as shown in

$$\begin{aligned} I_{\mathrm{diff,vdd}} &= I_{\mathrm{trans,vdd}} - I_{\mathrm{ibis,vdd}} \\ &= f(Vdd_{\mathrm{IBIS}} - Vgnd_{\mathrm{IBIS}}) \end{aligned} \tag{4}$$

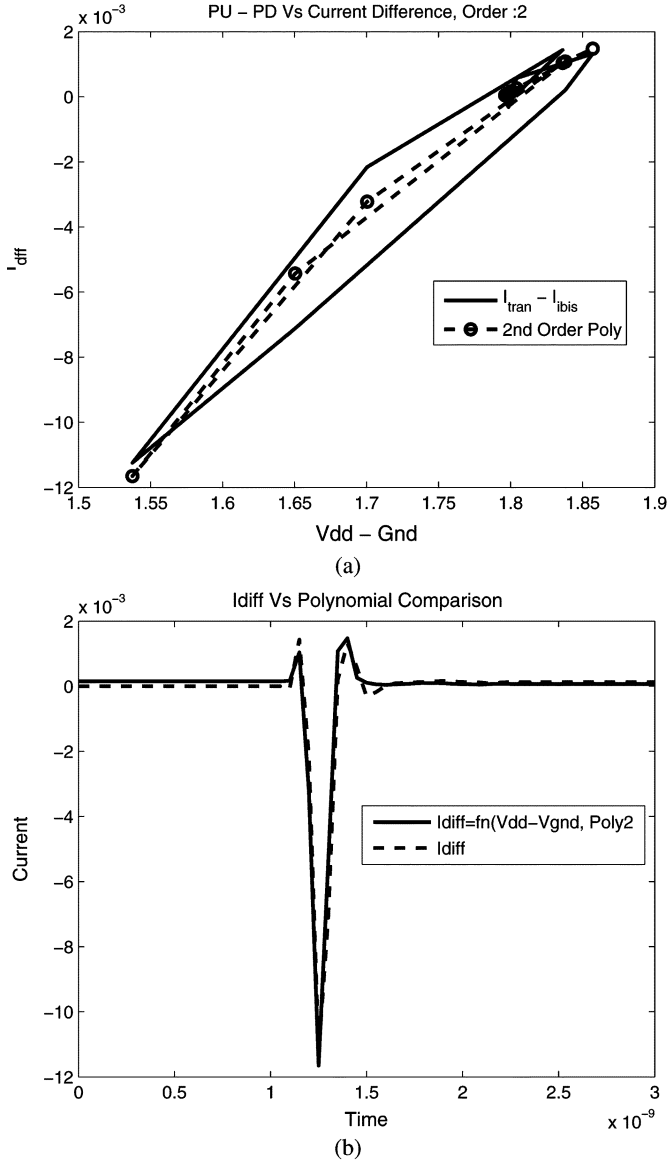

Fig. 6. The correlation in Fig. 5(b) is captured in a second-order polynomial that can be used to recreate the difference in current. Both the actual current difference and the current difference obtained using the polynomial are plotted (a) versus Vdd-Vgnd and (b) verses time.

where $\mathrm{Vdd_{IBIS}}$ and $\mathrm{Vgnd_{IBIS}}$ are voltage at the power and ground of the IBIS circuit.

The proposed error correction for predriver current can be done by carrying out the following steps.

Step 1): Setup circuit for rising and falling $\mathbf{I_{trans,vdd}}$ and $\mathbf{I_{ibis,vdd}}$: The correlation in (4) is captured in an *n*th-order polynomial [Fig. 6(a)] that can be used to recreate the difference in current. This is done by using a circuit with a single driver (using an IBIS model for the driver) and another circuit with the transistor model of the driver. Full package parasitics are used to obtain the current at the power pin in both the circuits. The output of the buffers are terminated in 50-Ω load to the ground. The circuit is subjected to both rising and falling input waveform to obtain polynomial coefficients for both the cases. The rise (and fall) time of the transition pulses should reflect the maximum speed of operation for the buffers. Rise time and fall time for polynomial generation for this work was 0.1 ns.

Step 2): Obtaining the polynomial coefficients for VCCS implementation: Once IBIS and transistor circuit SPICE output is obtained (.tr# files for HSPICE) for both rising and falling cases, it is read into MATLAB using the HSPICE toolbox [10]. MATLAB scripts are used to find the difference in the current at the power pin for both the circuits for the rising and falling cases as shown below

```
diff_current_Tran_IBIS_rise          =
Ivdd_Tran_rise-Ivdd_IBIS_rise;
diff_current_Tran_IBIS_fall          =
Ivdd_Tran_fall-Ivdd_IBIS_fall;
```

and using the difference current for rising and falling ("diff_current_Tran_IBIS_rise(fall)") to obtain the polynomials:

```
poly_coeff_rise                      =
polyfit(pu_pd_IBIS_rise,
diff_current_Tran_IBIS_rise, order);
poly_coeff_fall                      =
polyfit(pu_pd_IBIS_fall,
diff_current_Tran_IBIS_fall, order);
```

where "pu_pd_IBIS_rise(fall)" is the power-ground voltage of the IBIS model circuit and "order" is the desired order of the polynomial. The correlation is captured in an nth order polynomial [Fig. 6(a)] that can be used to recreate the difference in current.

Step 3): VCCS implementation: Once polynomials for the rising and falling curves are obtained, the extra current that needs to be injected in the IBIS model is done using voltage controlled current sources (VCCS). VCCSs are commonly available as spice primitives in most circuit simulators as shown below

```
GRisepoly risePoly 0 POLY(1) VDD
GND SCALE= 1 0.15682 − 0.37351 0.26511 −
0.0589
GFallpoly fallPoly 0 POLY(1) VDD
GND SCALE= 1 − 0.15860.22681 − 0.110490.0186
```

Fig. 6(b) compares the recreated difference current using the polynomial with the original. It can be observed that the current function generates very accurate difference current. The MATLAB script generates these polynomials for both the rising edge as well as the falling edge. Standalone tests of just the rising and falling edges show that the corrected IBIS waveforms are, in most cases almost 30% and in some cases more than 50% more accurate than standalone IBIS. It should be noted here that system level simulations are not possible with two different current sources supplying current for rising and falling edges separately. This is because there is no mechanism to detect the edges of the input stimulus to be able to apply the correct polynomial to the correct edge. To address this issue, an edge detecting mechanism is further discussed in Section IV. As a first step toward system level simulations, one single voltage controlled current source was obtained that captured the correlations for both rising and falling edges [Fig. 5(a)] in a single polynomial. Tests with only one polynomial show an improvement of nearly 20%–25% (Table I).

TABLE I
PERCENT IMPROVEMENT IN SIMULATION ACCURACY (AREA UNDER ERROR CURVE)

Test Setup	Driver	Pulse (one polynomial)	Pulse (two polynomial)	Pulse (2 Polynomial with Gate Modulation)
Parasitics only on power pin	driver 1	32.56%	42.14%	43.159%
	driver 2	35.31%	38.38%	46.39%
Parasitics on power pin and gnd Pin	driver 1	28.47%	42.41%	45.05%
	driver 2	20.08%	32.77%	34.54%

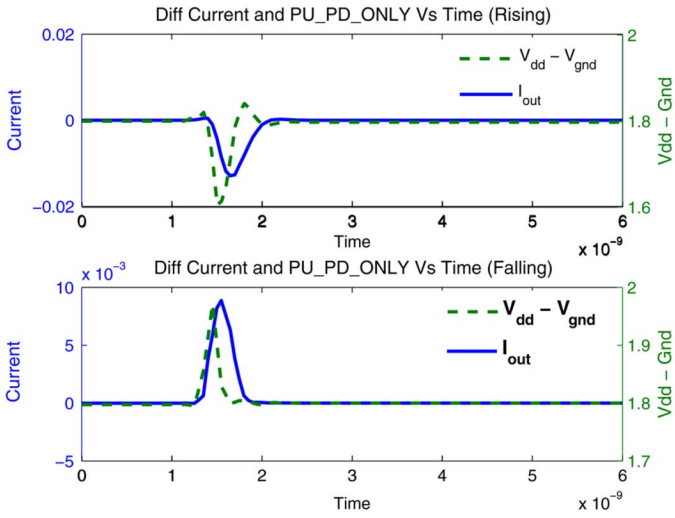

Fig. 7. Difference current at the output between IBIS model drivers and transistor model drivers have a high degree of correlation with the voltage difference at the power and ground pin in both the rising (top) and falling (bottom) transitions.

B. Gate Modulation Effect Error Correction

As discussed in Section II, gate modulation error correction is a function of the power and ground voltage. As in the case of the predriver error correction, where the current supply of the power pin was adjusted using the power and ground voltage (4), the gate modulation error correction requires the improvement of the total output current of the IO driver. The difference current at the output is a function of the power and ground voltage as shown in (5) and Fig. 7. $\mathrm{I}_{\mathrm{ibis,out}}$ in (5) is obtained using an IBIS model where the output current for the device is extracted from voltage-current tables. These tables are generated using a fixed power-ground voltage as discussed in Section II. To account for the power supply variations, a scaling coefficient K is introduced (6). K is a function of the instantaneous power supply voltage and the voltage at which the VI tables in the IBIS models were created (7). The effective output current thus scales corresponding to the actual voltage in the power and ground nodes. For example, if the instantaneous voltage at the power node jumps to 1.3 V during a simulation and IBIS models were created at 1.2 V, the effective current at the output node will be scaled by a factor of 1.08

$$I_{\mathrm{diff,out}} = I_{\mathrm{trans,out}} - I_{\mathrm{ibis,out}} = f(Vdd_{\mathrm{IBIS}} - Vgnd_{\mathrm{IBIS}}) \quad (5)$$

$$I_{\mathrm{eff}} = K \times I_{\mathrm{diff,out}} \quad (6)$$

where

$$K = N \times \frac{V\mathrm{inst}}{V_{\mathrm{nom}}} \quad (7)$$

$\mathrm{V}_{\mathrm{nom}}$ [in (7)] is the normal value at which the *I-V* tables in the IBIS models are created. $\mathrm{V}_{\mathrm{inst}}$ is the instantaneous (real time) voltage between the power and ground nodes of the I/O buffer. This voltage is not constant as the $\mathrm{V}_{\mathrm{nom}}$ but reflects the noise due to switching in the local power and ground nodes as shown in Fig. 5(a). N [in (7)] is a user dependent factor for adjusting the *K* factor and is usually the number of the drivers that are switching simultaneously in the system. SPICE implementation of the *K* factor is done in the following way:

```
Ek1 k1 0 vol= '(v(VDD1,GND1)-v(GND1))/
vcc'
Ek2 k2 0 vol = '4*(v(k1)-1)'
```

where "vcc" is the voltage at which the IBIS models were created "$\mathrm{V}_{\mathrm{nom}}$," "VDD1," and "GND1" are the local power and ground. The number of drivers used is four, hence $N = 4$.

As $I_{\mathrm{diff,out}}$ is the difference between the SPICE and IBIS model currents at the output, hence in effect, the error correction used for gate modulation effect not only corrects for the voltage fluctuations in the power and ground but also corrects for other effects such as the lack of termination currents in the IBIS models. Results with and without the gate modulation effect is discussed in Section VI.

IV. ACHIEVING IMPROVED ACCURACY FOR SYSTEM LEVEL SIMULATIONS

Even though a single polynomial (as discussed in the previous section) for both rising and falling edges gives a good result when compared to the plain IBIS models, much better results can be achieved when using two distinct polynomials—one for rising and the other for the falling edge for each error correction described in Section III. This is because each transition is dealt with individually rather than collectively by one single polynomial. Separate polynomials for rising and falling edges can be used by utilizing behavioral spice constructs to determine the edge of the input signal. A delayed input is used to detect the rising and falling edges, as shown in Fig. 8. The rising edge [Fig. 8(a)] is detected by inverting the delayed input and performing a *logical AND* operation with the original input. The falling edge [Fig. 8(b)] is detected by inverting the original input and performing a *logical AND* operation with the delayed input.

Once an edge is detected, the corresponding VCCS current is used to boost the current in the power supply loop (for the

TABLE II
PERCENT IMPROVEMENT IN SIMULATION ACCURACY (MEAN SQUARE ERROR)

Test Setup	Driver	Pulse (1 polynomial)	Pulse (2 polynomial)	Pulse (2 Polynomial with Gate Modulation)
Parasitics only on power pin	driver 1	19.58%	26.10%	26.38%
	driver 2	53.99%	61.15%	72.75%
Parasitics on power pin and gnd Pin	driver 1	16.72%	22.24%	23.07%
	driver 2	26.63%	56.05%	57.29%

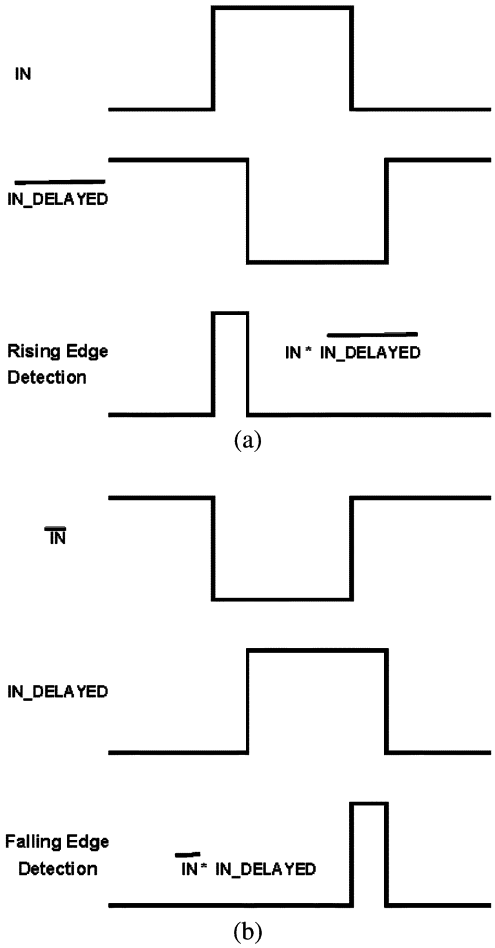

Fig. 8. Detecting (a) the rising edge and (b) the falling edge for system level simulations using the black-box.

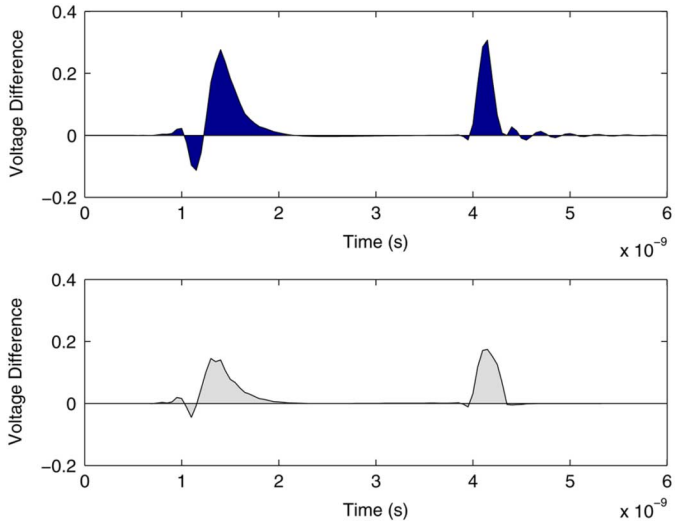

Fig. 9. Improvement in simulation Accuracy is judged using area under the difference curve of plain IBIS and transistor level models (top) and corrected IBIS and transistor level models (bottom).

predriver current) and the output pin loop (for the gate modulation effect).

V. METRICS

To quantify the improvement in simulation accuracy by using the black-box in conjunction with the IBIS model, various metrics were used. These include the following.

1) **Area under the difference curve**: The improvement in simulation accuracy is estimated by comparing the area under the difference curve between the output voltage of plain IBIS and transistor level model and corrected IBIS and the transistor level model as shown in Fig. 9. It can be observed in the figure that the bottom curve (with error correction) has less area when compared to the top curve (plain IBIS without error correction), thus signifying that the corrected IBIS curve overlaps with the transistor model curve to a greater degree when compared to the plain IBIS curve. This metric is used extensively throughout this work. Table I summarizes the improvement numbers for two drivers using the area under the difference curve.
2) **Mean square error**: For this method of assessing simulation accuracy, the error is estimated using the following formula:

$$\text{Mean Square Error} = \frac{1}{N}\sum_{i=1}^{N}(Y_{\text{IBIS},i} - Y_{\text{trans},i})^2 \qquad (8)$$

where $Y_{\text{IBIS},i}$ and $Y_{\text{trans},i}$ are individual output voltage values for the IBIS model circuit and transistor model circuit respectively. Table II gives the improvement numbers for two drivers using the mean square error between plain IBIS and corrected IBIS and transistor model.
3) **Maximum noise in the quiet line**: Maximum noise in the quiet line when multiple drivers are switching simultaneously can affect system performance and operation as a high voltage spike in the quiet line can reach the minimum voltage threshold and trigger a false signal. Fig. 15 displays the bar graph for two drivers used in the tests (next section).
4) **Delay**: Delay in the rising edge of the output signal at 90% of the signal strength is recorded for the transistor, plain

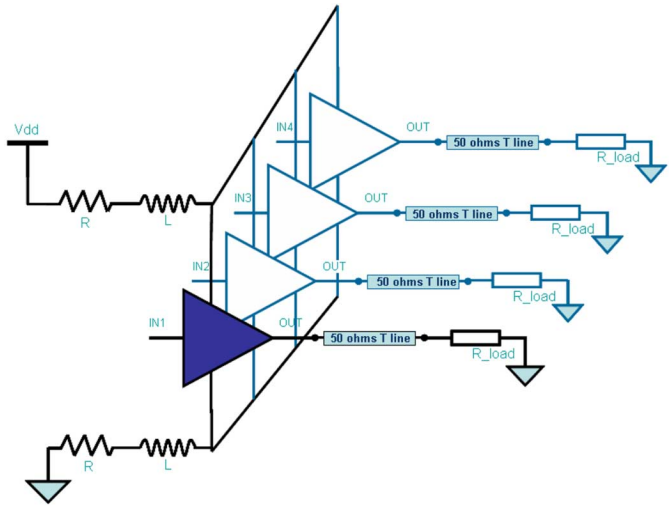

Fig. 10. Setup for testing the improved IBIS models. This setup shows lumped parasitic elements at both power and ground pins.

IBIS and corrected IBIS circuits. Fig. 16 shows the delay bar graph for the two drivers that are used in the experiment. The graph shows the relative percentage error of the IBIS models with respect to the transistor model. The delay for the corrected IBIS models are divided between the two correction factors that were used-namely predriver current error correction (phase one) (discussed in Section III-A) and gate modulation effect error correction (phase two) (discussed in Section III-B).

VI. Test Results

In this section, comparative test results are presented using transistor level models, plain IBIS models and improved IBIS models. The tests are performed on two drivers. The first (driver one) is a simple voltage mode CMOS cascading inverter driver (as described in [1]) and the other (driver two) is a real life 512 MB DDR2 voltage mode driver (part no. MT47H128M4BT-5E) from Micron Inc. [11]. Memory IO controllers use voltage mode drivers (HSTL, SSTL) and noise (SSN) is of concern in them, as such, tests are done on voltage mode drivers to prove the methodology described in this paper.

Test Setup: Tests were done with lumped elements modeling the power and ground parasitics in two different combinations. In the first case, the inductance (which is the primary cause of SSN [9] and is used here to model it) was placed only on the power pin (as described in [2]) while in the second instance, both the power and ground pins were connected to inductance (as described in [1]) (Fig. 10). In the second instance, only self inductance was used and mutual inductance was ignored with the assumption that the result in all the three cases (original (plain) IBIS, corrected IBIS, and SPICE), even without mutual inductance, should produce similar results. Results for both the setups are provided for each test described in this section. Tests were performed with three drivers switching simultaneously and one quiet driver. Decoupling capacitors are also used as a part of the solution to improve SSN response of the IBIS models. The power supply and rise time used for all the tests was 1.8 V and 100 ps, respectively. For the IBIS models, the C_comp was

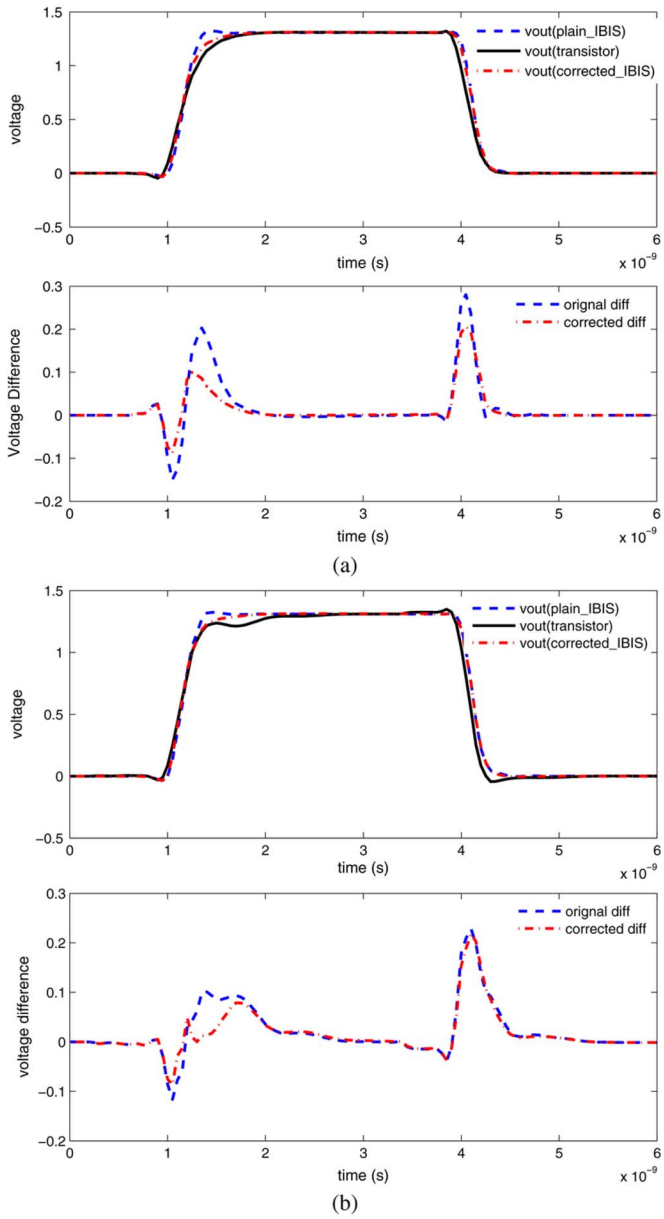

Fig. 11. Voltage (top) and voltage difference (bottom) between plain IBIS and transistor (dashed line) and corrected IBIS and transistor (dotted line) of a MICRON DDR2 driver, (a) with parasitics only on power pin and (b) parasitics on power and ground pin. The error correction is achieved with only one polynomial for both the edges.

split 25%, 75%, 0%, and 0% between pull up, pull down, power clamp, and ground clamp. R_load in Fig. 10 matches the characteristic impedance of the transmission lines (50 Ω). To validate the methodology described in this paper, tests were also performed with open ended terminations at the far end of the transmission line.

This section is divided in three further sections following the different stages of work performed to achieve the final result. The first section gives the results of the tests done with only one polynomial for both the edges for the predriver current error correction described in Section III-A; the second section includes the result when two polynomials, one for each edge, were used for the predriver current error correction. The third section has

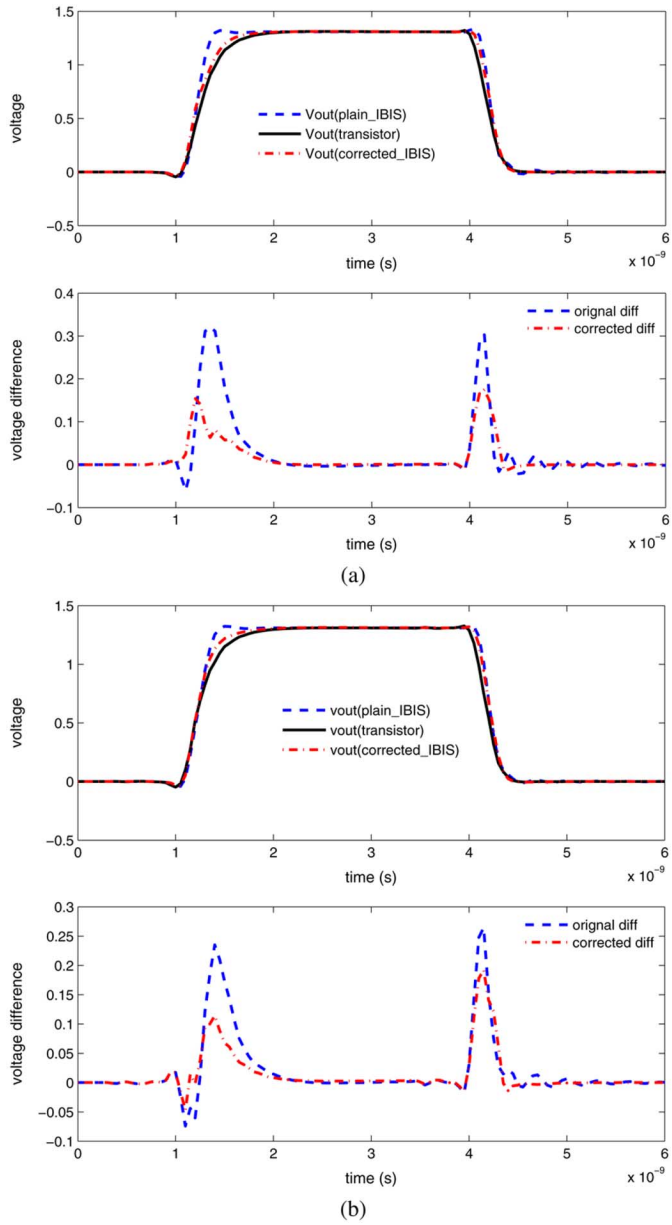

Fig. 12. Voltage (top) and voltage difference (bottom) of the MICRON driver, (a) with parasitics only on power pin and (b) parasitics on power and ground pin. The gate modulation error correction and predriver current error correction are achieved with separate polynomials for each edges

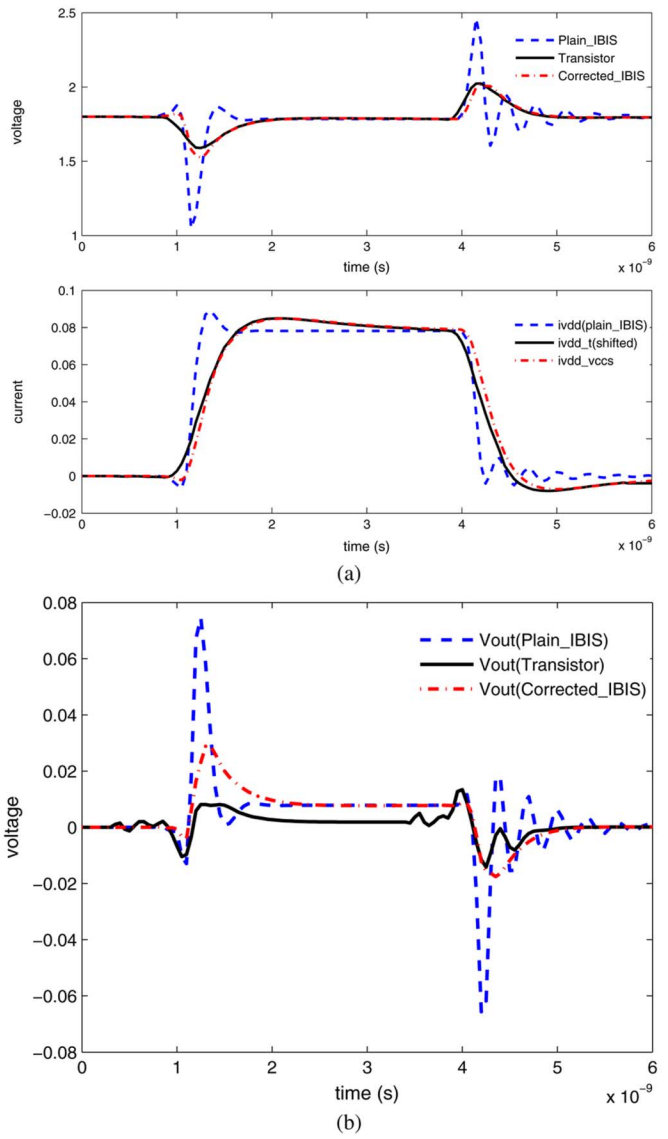

Fig. 13. (a) Vdd-Gnd voltage (top) and Vdd current (bottom) for test setup with parasitics on both power and ground pins of a MICRON DDR2 driver. (b) Quiet line voltage for the same setup. Plain IBIS is denoted using dashed line, corrected IBIS is shown as dots and transistor model waveforms are shown as solid lines. Both error corrections are included in this figure.

results with the gate modulation error correction with separate polynomials for each edge, as described in Section III-B. Results in this section also include effects of the predriver error correction along with the gate modulation error correction in the blackbox.

A. Same Equation for Rising and Falling Edges for Predriver Current Error Correction

In this section, results with only one polynomial in the black-box are presented. This polynomial was obtained by having a 010 pulse at the input of the driver while obtaining the polynomial (Step 1 of Section III-A). The MATLAB script generates the required polynomial which can be used in the VCCSs.

Tests were performed on both the drivers for this arrangement with and without ground parasitics. An overall improvement, measured by observing the area under the error curve (Section V-1) of, on average, 30% is observed in Table I. Similar observation can be made from Table II (mean square error).

Fig. 11 shows the output voltage and current of a MICRON DDR2 driver (driver two) for (a) no parasitics on the ground pin and (b) parasitics on power and ground pins.

B. Different Equations for Rising and Falling Edges for Predriver Current Error Correction

The tests performed in this section involve black-box with separate polynomials for rising and falling edges. An improvement in the area under the error curve of 10%–12% can be achieved over the method described in *A* with separate polynomials for the rising and falling edge. An overall improvement

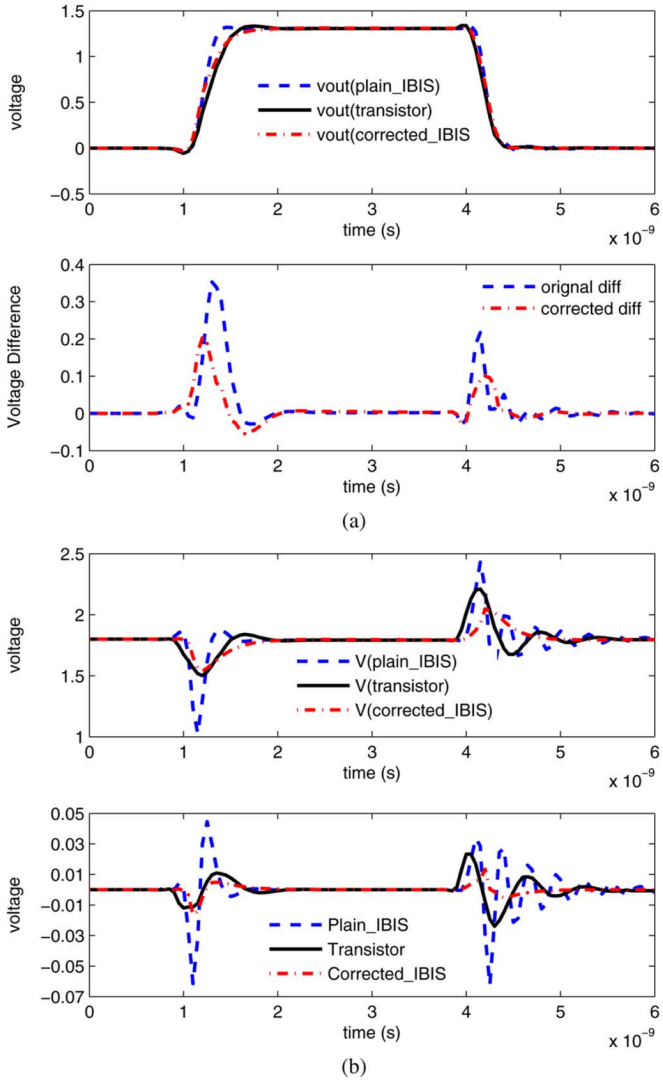

Fig. 14. (a) Voltage (top) and voltage difference (bottom) of the MICRON driver, with parasitics only on power pin and open ended termination at the far end, and (b) Vdd-Gnd voltage (top) and quiet line voltage for the same setup. Plain IBIS is denoted using dashed line, corrected IBIS is shown as dots and transistor model waveforms are shown as solid lines.

in simulation accuracy of 35%–40% can be achieved with this correction over plain IBIS.

C. Different Equations for Rising and Falling Edges for Gate Modulation Effect

Fig. 12 shows the improvement in voltage response in the MICRON DDR2 voltage mode driver with the gate modulation effect error correction along with the predriver current error correction. The error correction VCCSs are implemented using two separate polynomials, one for each edge. Fig. 12(a) shows the voltage response of the driver without package parasitics at the ground pin. Fig. 12(b) shows the voltage response of the driver with package parasitics at the ground pin.

Fig. 13(a) shows the Vdd-Gnd voltage (top) and the power pin current (bottom) for the MICRON driver. It can be observed that the corrected IBIS model follows the transistor model response closely when compared with the plain IBIS model.

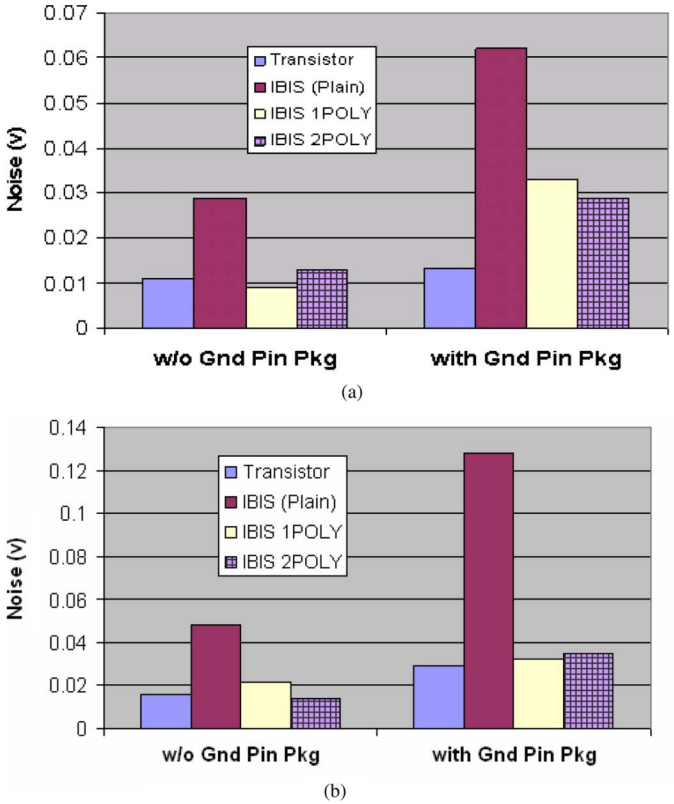

Fig. 15. Maximum noise in quiet line in (a) MICRON DDR2 and (b) Cascaded Inverter driver.

Fig. 13(b) shows the voltage induced in the quiet line as a result of SSN. Again, the corrected model shows a more realistic picture of the voltage levels in the quiet line.

Tests were also performed with open ended terminations at the far end of the transmission lines. Fig. 14(a) shows the improvement in voltage response in the MICRON DDR2 voltage mode driver with the predriver current error correction. The top figure shows the actual voltage at the output pad while the bottom figure shows the voltage difference between the corrected IBIS and the plain IBIS with respect to the transistor level models. The error correction VCCSs are implemented using two separate polynomials, one for each edge. An overall improvement of nearly 32% is observed with the predriver error correction in conjunction with the plain IBIS model. Fig. 14(b) shows the Vdd-Gnd voltage (top) and the voltage induced in the quiet line (bottom) for the MICRON driver.

It can be observed that the corrected IBIS model follows the transistor model response closely when compared with the plain IBIS model with an open ended termination at the far end of the transmission lines of the test setup described in Fig. 10.

VII. Results Analysis

Results presented and discussed in the previous section represent only a small number of the actual tests performed to test the blackbox. This section includes detailed results and performs analysis of the results achieved.

Table I shows the percent improvement in simulation accuracy for driver one (voltage mode cascading inverter) and driver

TABLE III
MAXIMUM NOISE (V) IN THE QUIET LINE

Test Setup	Driver	Transistor	Plain IBIS	Corrected IBIS 1 Polynomial	Corrected IBIS 2 Polynomial
Pkg on power pin	driver 1	0.016	0.0479	0.02148	0.0139
	driver 2	0.011	0.029	0.009	0.013
Pkg on power and gnd Pin	driver 1	0.029	0.128	0.0324	0.0348
	driver 2	0.0134	0.062	0.033	0.029

TABLE IV
ABSOLUTE DELAY (S) WITH RESPECT TO INPUT SIGNAL

Test Setup	Driver	Transistor	Plain IBIS	Corrected IBIS phase 1	Corrected IBIS phase 2
Pkg on power pin	driver 1	3.90E-10	2.56E-10	3.57E-10	3.68E-10
	driver 2	9.22E-10	6.41E-10	8.40E-10	8.94E-10
Pkg on power and gnd Pin	driver 1	3.88E-10	2.57E-10	3.38E-10	3.48E-10
	driver 2	9.10E-10	6.90E-10	8.57E-10	8.62E-10

two (DDR2 SDRAM driver). The improvement is assessed using the area under the error curve.

Table II summarizes the percent improvement in simulation accuracy using the mean square error method.

Table III gives the maximum noise in the quiet driver for the cascade inverter driver (driver one) and the MICRON DDR2 driver (driver two). Fig. 15 shows a summary of the maximum noise in the quiet line for the two drivers for both the cases of parasitic arrangement. It can be observed from the bar plot that the plain IBIS models has the largest noise when compared to the transistor models and the corrected models. After the correction, the noise in the quiet line is of comparable level to the noise in the transistor model.

Table IV presents the absolute delay of the rising edge of the plain IBIS, the corrected IBIS model (phase one and phase two) and the transistor model. Fig. 16 shows a summary of the relative percentage error in the delay of the rising edge of the plain IBIS and the corrected IBIS models with respect to the transistor model simulation. Delay is recorded at 90% of the signal level for the rising edge of the output and reference (input) signal. The corrected IBIS model delay is taken for both the phases of improvement described in Section III. It can be observed that the output after **phase two**[1] has the least delay error for both the drivers tested. In the plots, **phase one** represents the predriver current error correction.

Another observation that can be made from Table IV is the value of the delay itself. A delay of 0.9 ns for the transistor model MICRON driver includes the signal propagation delay of the driver. A delay of only 0.6 ns (in the case of plain IBIS) can result in a glitch in the system resulting in faulty signaling at the output.

[1]Implementation of gate modulation error correction and the predriver current error correction.

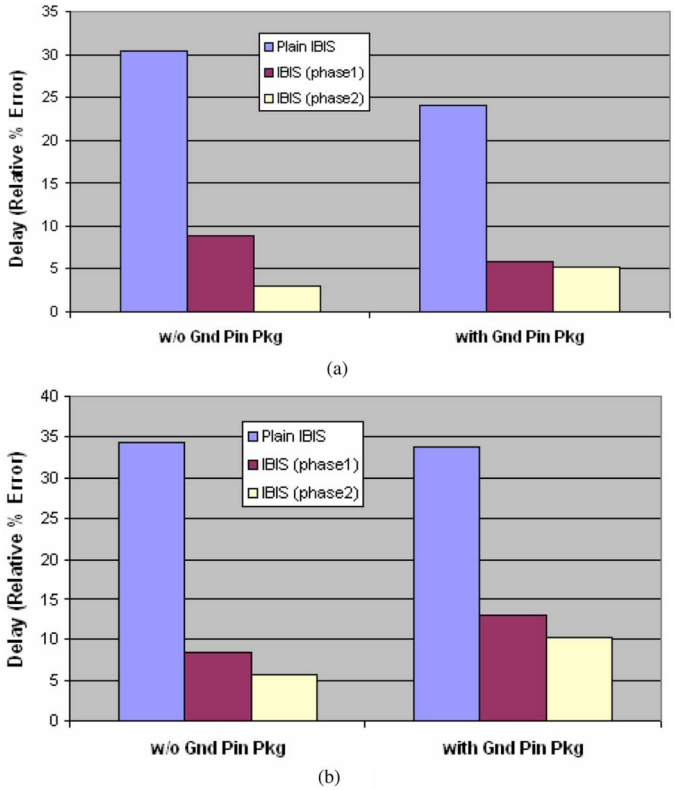

Fig. 16. Delay in the rising edge (relative % error) for (a) MICRON DDR2 and (b) Cascaded Inverter driver.

VIII. CONCLUSION

A black-box modeling approach has been proposed, implemented and tested in this paper. The methodology proposed keeps the IBIS model as the base modeling engine maintaining

the physical, circuit based structure of the IBIS models, thus allowing the model user to modify or debug the model.

The black-box consists of behavioral SPICE constructs to compensate for the missing currents in a traditional IBIS model. The parameters of the proposed black-box are obtained automatically using MATLAB scripts. Using the black-box with the IBIS model does not incur any simulation time overhead.

An improvement in simulation accuracy of more than 40% was achieved using a black-box approach. The parameters of the black-box are obtained using SPICE primitives, as such the usage of the black-box does not require special handling by the simulator and can be used in a simulator of choice. Also, as the black-box is separate from IBIS models, no changes have to be made to the IBIS model.

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