AC Coupled Backplane Communication Using Embedded Capacitor

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Abstract **Surface Mount Capacitors can be replaced with a buried capacitor in backplane interconnect applications requiring blocking capacitance, such as FiberChannel. This replacement improves cost, reliability and parasitic inductance. The smaller nominal capacitance value can be compensated for by using an equalizing receiver filter. Tradeoffs in capacitance choice are explained in detail. A nominal capacitance of around 1 pF provides a good choice for the analyzed scenarios.**

I. INTRODUCTION

Some interconnect standards, such as FiberChannel, require series capacitors for DC decoupling. These are usually built using surface mount technology (SMT). Embedded capacitor technology has proven better performance than surface mount technology (SMT) capacitors in power supply decoupling [1]-[7]. Embedded capacitor not only saves area for on-chip capacitor and the mount surface of SMT capacitor on PCB, but also has better reliability due to its embedded structure [5]. It also significantly reduces parasitic inductance. The question addressed in this paper is whether buried capacitors can be used to replace surface mount capacitors in interconnect circuits, and thus bring these advantages to that application. The key problem is that buried capacitors provide capacitance values smaller than those called for in the standards. With capacitance density of above tens of nF/cm2, if combined with the circuit design technique of AC coupled interconnect (ACCI) [9], the embedded capacitor actually is suitable for replacing the DC blocking capacitor in backplane chip-to-chip communication.

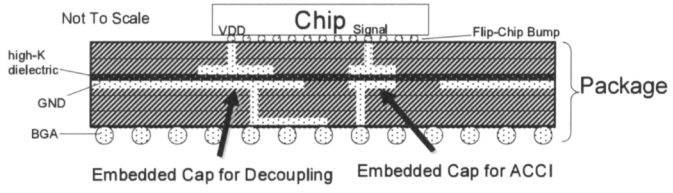

Fig. 1. Structure of Package Cross-section

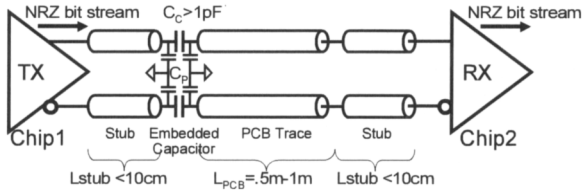

Fig. 2. Simplified Schematic of the ACCI channel with Embedded Capacitor

A typical cross-section of a packaging embedded capacitor for ACCI is shown in Fig. 1. The layer inside the laminate packaging for the embedded capacitors was created for power supply decoupling purposes, but eventually signals have to be routed from top to bottom and pass through the embedded capacitor layer. Therefore, it is straightforward to make use of the capacitor structure and insert a series capacitor in the signaling channel, where simplified schematic model for the proposed channel in Fig. 2. Notice that the embedded capacitor can also be manufactured in the PCB but the channel model in Fig. 2 remains valid. To represent the worst case scenario, the following analysis assumes that the channel consists of two segments of 10cm routing length (L_{stub}) on laminate package at both ends of the channel, a 100cm long 5mil-5mil microstrip on FR4 PCB (L_{PCB}), and a coupling capacitor (C_C) inserted between the first stub and the PCB trace. Though not shown in Fig. 2, appropriate parasitic inductance and resistance were included in the channel model. The detail of the modeling can be found in [7].

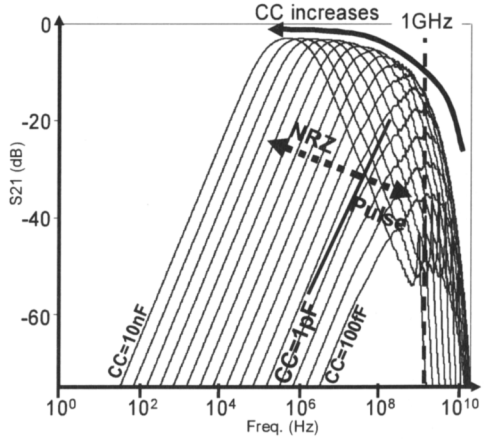

Fig. 3. Pulse signaling vs. NRZ signaling in Freq Domain

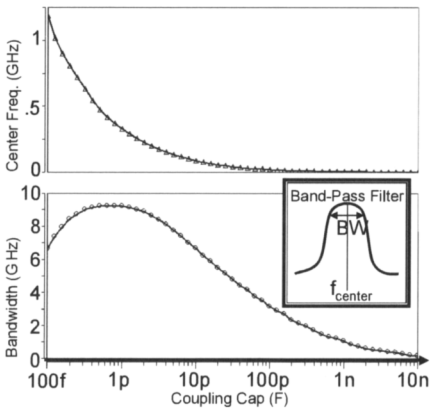

Fig. 4. Bandwidth and center freq. of the equivalent BPF

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II. Analysis of Proposed ACCI Channel

ACCI utilizes small series capacitors (150fF in [9]) in the channel to achieve passive equalization. There are two types of signaling method supported by ACCI – pulse signaling and NRZ signaling. Whether the channel is suitable for pulse or NRZ signaling depends on the size of the C_C. The simulation result in Fig. 3 shows the difference between pulse and NRZ signaling obtained by sweeping C_C over a large range (100fF to 10nF). It is clearly shown that an ACCI channel acts as an equivalent band-pass filter (BPF). The peak of the BPF shifts toward higher frequency when the value of C_C decreases and allows only high frequency components through the channel. The amount of high frequency components being passed through will determine whether pulse signaling or NRZ signaling is used. The magnitude of the BPF will be affected by both C_C and channel length, but once the value of C_C is determined the maximum channel length can be subsequently set by the circuit performance, such as minimum receiver sensitivity. The following section explains the relationship of signaling method and the BPF characteristics.

A. Pulse Signaling

When a smaller C_C is used (<1pF), the NRZ output of the transmitter will be differentiated across the capacitor and leaves only positive/negative pulses throughout the channel. The pulses consist of mostly high-frequency components; therefore the most suitable C_C value is the one that makes the channel BPF peak at highest frequency points. I.e., according to Fig. 4, the smaller the value of C_C the higher center frequency of the BPF, hence higher bit-rate supported. The unit step responses of ACCI channel with various C_C shown in Fig. 5 help explain this trend in the time-domain. It shows that smaller values of C_C results in narrower pulse widths. However, smaller values of C_C also reduce the pulse height. For C_C <1pF, the voltage pulse drops rapidly after the initial coupling. Thus ideally a very small C_C could make the pulse narrower than the target bit period and eliminate the need for additional equalization. However, the minimum reasonable value for C_C, which also corresponds to the lowest signal amplitude, is limited by the circuit performance and signal integrity; i.e., receiver sensitivity, crosstalk, and noises. For example, in standard 0.18um CMOS technology, in order to generate a 100mV swing plus 30mV margin for noise/crosstalk at receiver side, C_C value should be around 1pF.

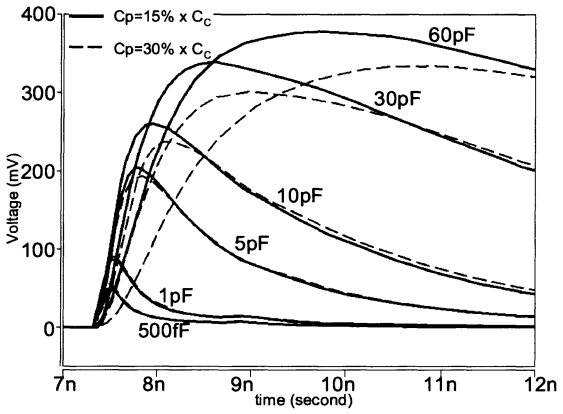

Fig. 5. Step Response of ACCI with Various C_C and C_P

Table I. Timing and Circuit Requirement for Various CC

C_C	Time for max run length	TX Requirement	RX Requirement
500f	1.8n	Voltage Mode	Pulse Receiver
1p	2.0n	Voltage Mode	Pulse Receiver
5p	3.8n	Voltage Mode	Pulse Receiver
10p	5.9n	Voltage Mode	NRZ Receiver (Or Pulse Receiver)
30p	14.3n	Voltage Mode	NRZ Receiver (Or Pulse Receiver)
60p	25.2n	Voltage Mode	NRZ Receiver (Or Pulse Receiver)

B. NRZ Signaling

If a larger value for C_C is used (>10pF), NRZ signal is supported by the ACCI channel. Unlike SMT DC-blocking capacitors with sizes of tens of nF or more, the embedded capacitor technology will only support capacitances up to the nF-range. The benefits of relatively smaller (compared with SMT) capacitance are relaxed constraints on the transmitter driving strength and less power consumption. But the downside comes from the pulse response produced in a channel with these smaller values of capacitance. In Fig. 5, larger C_C (>1pF) generate larger pulses, as well as much higher and longer tails. Those tails will decay depending on the size C_C but with proper constraints they can be used to support NRZ signaling. Table I lists the time for maximum run length in the bit stream when various C_C is used. For example, if 10pF is to be used, the maximum number of consecutive 1's or 0's for a 5Gb/s (200ps period) bit stream will be 5.9ns/200ps = 29. Notice that a capacitor value between 1pF and 10pF seems un-suitable for either pulse or NRZ signaling but in fact can still be used as long as the receiver has the latch block. In other words, the latch in the pulse receiver (comparator with hysteresis) is capable of recovering not only pulse but also NRZ signal, including a hybrid (pulse AND NRZ) due to a C_C in the mid-range.

C. Parasitics and Stub Length

One major difference between decoupling capacitors like [1] and signaling capacitors presented in this paper are the parasitics. In the case of power supply decoupling, all the fringe capacitance are beneficial, while the parasitic capacitor for ACCI signaling will degrade the signal edge rate and swing, as shown in Fig. 5. Especially when larger C_C (>10pF) is used, the rise time increases as much as 50% and amplitude decreases up to 10% due to the presence of parasitic capacitance.

The proposed scheme is assumed to share the same embedded capacitor structure with decoupling capacitors, which will be placed in the "die shadow" because its sensitivity to the relative location to the actual circuit (silicon die) [8]. Therefore,

for a next generation package of 10,000 pins with 0.65mm pitch BGA, the routing channel from the chip/package interface to the embedded capacitor could be as long as 5cm.. Fig. 6 compares the S21 of channels for different stub lengths. The stub is modeled as a 40ohm 30um-wide channel inside the laminate package. It is shown that when L_{stub} increases from 1cm to 10cm given that the total channel length is fixed at 120cm, the S21 does NOT vary by more than 1dB. In other words, the length of the stub does not affect the channel response unless the impedance is badly controlled.

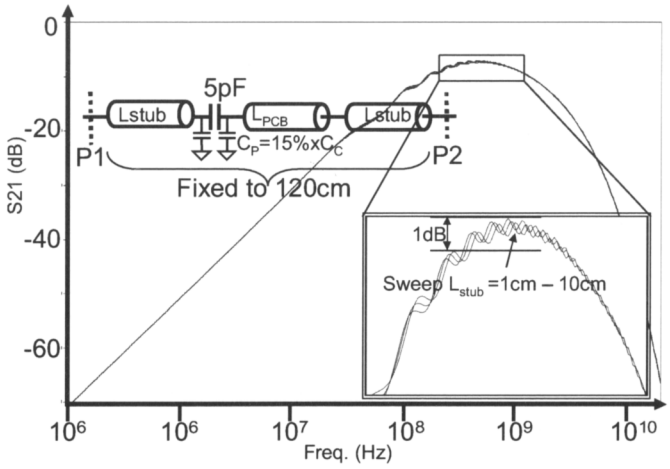

Fig. 6. Sweep L_{stub} while fixing total channel length

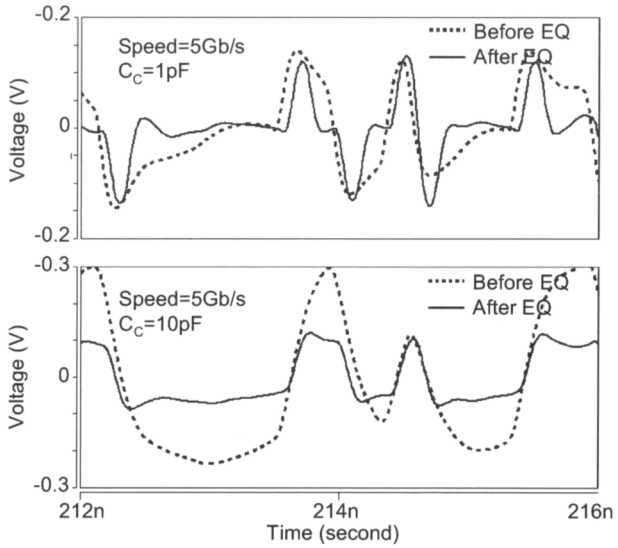

Fig. 7. Comparison of the waveform before and after fractional equalizer

III. Transceiver Design

ACCI utilizes the coupling capacitor for low-swing pulse signaling and a voltage mode transmitter is required. In this project, a simple pair of complementary progressively-sized inverters is used to transmit the NRZ bit stream.

It is possible to select the capacitor size and allowable channel length to be "matched" so that the passive equalization alone is enough to eliminate the inter-symbol-interference (ISI) at specific operating frequency [9]. The circuit, however, would have very limited flexibility. Thus, a non-clocked version of receiver-side fractionally-spaced equalizer (FSE) scheme [10] is introduced to accommodate a wider range of parameter variation, such as channel length from 10cm to 100cm and capacitor size from 1pF to 10pF. The fractional delay permits equalization within the bit period, thus giving the agility to equalize a number of pulse and NRZ scenarios. The comparison of time-domain waveforms in Fig. 7 shows that the FSE is able to cancel out the signal tails even when C_C varies a lot.

There are three major advantages gained by using this FSE receiver. First, the analog nature of the circuit makes the receiver work for both pulse signaling and NRZ signaling. Second, there is no clock involved in the transceiver thus saving the effort of designing the clock distribution network and saving power in the clock tree. And third, the power consumption is low, compared with digital filter at comparable speed with similar channel characteristic.

The simulated eyediagrams in Fig. 8. show that the fractional FIR is capable of recovering the received pulse signals as well as NRZ signals. The transceiver is implemented in standard 0.18 CMOS technology and can send a 5G/ps bit stream through a worst-case channel of [10cm]=[1pF]=[100cm]=[10cm]. The power consumption is 5mW for the transmitter and 15mW.

IV. Conclusion

Embedded capacitor combined with ACCI circuit shows the advantages of low power, high speed, high flexibility, and relaxed circuit constraint, in addition to the advantages that originally comes with embedded capacitor [7]. The trade-offs between capacitor size, parasitic of the capacitor, channel length, and constraint on circuit performances are used to determine the most appropriate value for the embedded series capacitor. However, the performance is not highly sensitive to the value chosen. A fractional FIR pulse receiver is introduced to enable the channel to operate correctly across multiple length and capacitance ranges. When using this receiver, a series capacitance of around 1 pF is a good choice, giving an area of 1000 um^2, based on a density of 100 nF/cm^2. This combination is a good candidate for replacing SMT series capacitors with buried capacitors in backplane applications.

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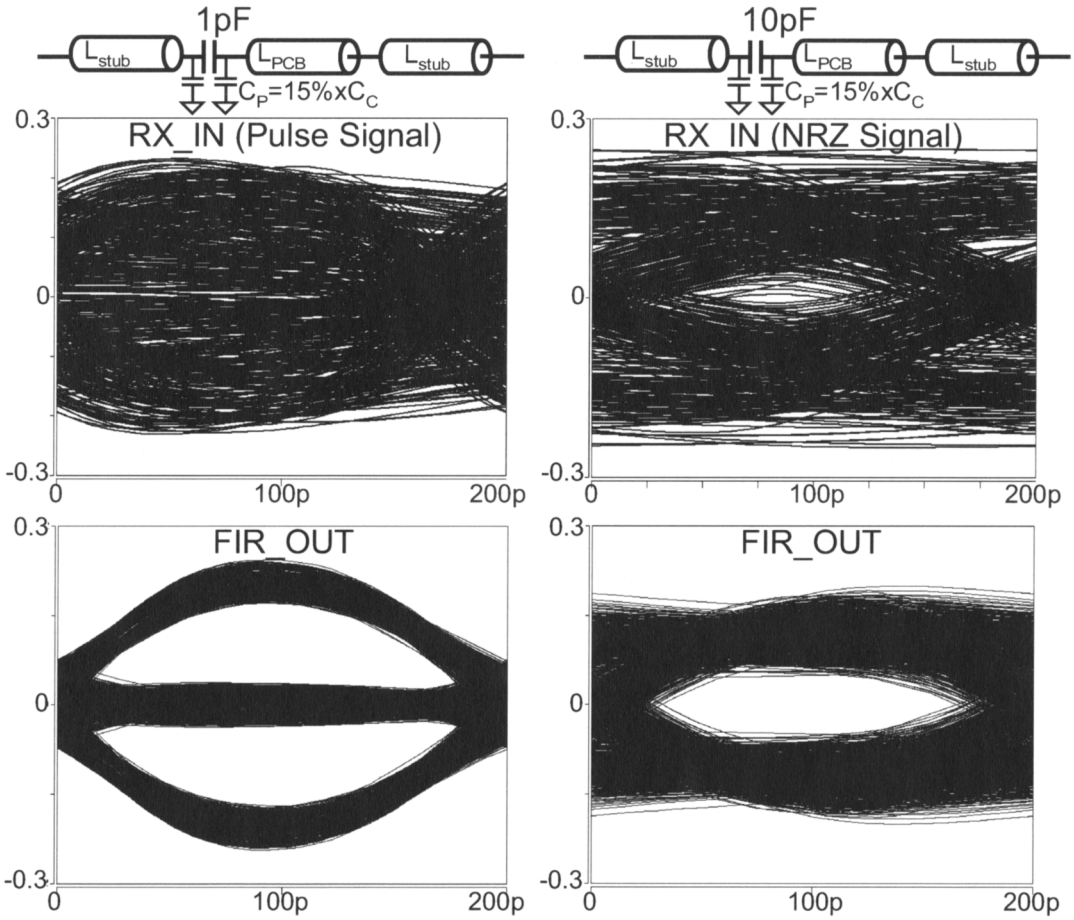

Fig. 8. Eye diagram of the receiver waveform before and after the fractional FIR