Keeping Hot Chips Cool: Are IC Thermal Problems Hot Air?

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PANEL SUMMARY

Thermal issues are becoming more important but is the hype getting the better of the facts? Does this deserve more attention than for some niche designs and technologies such as 3D ICs.? Does the broader design community need to worry about it at 32nm and beyond or it will only impact a small segment of designs? In short, does the severity of power issues coupled with packaging complexity translate into a thermal crisis in future? This is an educational panel with a little bit of controversy that will address the thermal issue in IC design. When will this issue be emerging as a crucial concern if at all? What are the solutions to resolve this potential crisis?

Categories and Subject Descriptors

B Hardware, B.7 Integrated Circuit, B.7.2 Design Aids

General Terms

Algorithms, Performance, Design, Measurement

Keywords

VLSI design, Thermal management, Power dissipation

PANELIST VIEWPOINTS

Darvin Edwards: Thermal issues are becoming a larger design concern across all manner of devices and systems. High performance microprocessors are pushing the limits of air cooling with growing die sizes, growing parasitic leakage powers, and higher powers in general, though several design, process and software tricks are being used to slow the growing power dissipation trend. On the low end, DC-to-DC converts and digital amplifiers are becoming ever smaller and more efficient, but are experiencing higher power densities per mm^2 which must be cooled. New classes of packages including stacked die packages and package-on-package (POP) have led to higher power densities on the PCB, creating PCB hot spots which must be managed. Other packaging technologies on the horizon such as embedded die and 3D through-silicon via technology (TSV) promise to make this situation worse. System on a chip (SOC) solutions often integrate logic, memory, and driver type devices which can result in high thermal gradients on the die, as can high current transistors on analog devices. These on die hot spots can no longer be ignored, but must be managed in the design phase. Existing tools to co-design thermal performance and die layouts are sub-optimal for the task. Future process roadmaps show reduced maximum junction temperatures for some logic devices which will only make thermal management more difficult.

Several other trends are driving thermal management complexity.
Incremental battery capacity improvements allow higher portable power dissipation for functions such as games and video, while the drive towards more compact circuit subsystems results in higher power densities and potentially more thermal problems. A series of recent product thermal issues reported in trade journals highlight the failure of many design engineers to appropriately account for these challenges. As well, the limits of available power generation infrastructure to supply and cool the plethora of new electronic products are causing a growing level of legislative initiatives to dictate power dissipation performance per function.

This confluence of factors is driving the need for more thermal engineers to perform better system level analysis, better thermal modeling tools which are more flexible, faster and detailed, and a higher level of accuracy in IC package abstraction (compact models) to ensure robust thermal design. An overarching goal must be to reduce power consumption per function through smart process design, die design and software optimization.

Paul Franzon: The "niche" in which detailed thermal design matters grows with technology scaling. A key decision is

DAC 2008, June 8–13, 2008, Anaheim, California, USA

ensuring that thermal design is being conducted with sufficient fidelity before a product fails due to a thermally induced failure. One approach to answering this question is to develop a simple metric that predicts thermal design needs based on simple design and technology parameters.

Stephen Kosonocky: At 65nm many companies are able to integrate four or more CPU cores per die. Looking forward to 32nm, major performance gains are likely to continue to be made chiefly by adding cores, threads and special purpose accelerators. Improving single thread performance will also put pressure on chip designers to push die temperatures even higher. Although thermal monitoring and throttling is standard for most high performance designs today, these techniques are designed to prevent catastrophic failures and cannot be counted on during normal operational modes. Presently, thermal modeling is mainly used for floorplanning and package/system planning. As we push die temperatures higher, reliability and performance modeling may need to account for local thermal conditions.

Alan J Weger: It is not mere accident or hyperbole that has led thermal issues to the forefront, especially in high-performance systems -- what's more, these issues are not limited to any particular class of electronic devices. Five broad trends have converged: the inexorable demand for lower cost, greater performance, and system integration (including 3D); the end of classical scaling and the associated parasitic leakage and process variability; the non-scalable nature of cooling systems; continued reliability challenges; and the rising cost of energy and related environmental impact. Silicon chips, in their operating environment, can reside in one or more of three regimes: power-limited, temperature-limited, and hotspot-limited; these regimes, and their interaction with design and layout, must be understood. Two counter-trends offer an "exit strategy": increased parallelism, and improved power and thermal modeling, design and management. The balance between these trends will determine the regimes in which a particular implementation resides, and the extent to which a thermal crisis can be averted.

Andrew Yang: Thermal integrity for chip-package-system is becoming more critical as system-in-package (SiP) designs increase its adoption, especially for stacked-chip with through-silicon-via (TSV) technologies. Addressing this challenge requires more accurate chip power estimation and distribution with consideration of process-dependent leakage current and activity-based dynamic power. Integrated die/package thermal analysis enables optimization of system-level cooling design and mitigation of stress-induced package failures. Advanced package structures further increase analysis complexity due to its 3-D nature.