Inductively Coupled Connectors and Sockets for Multi-Gb/s Pulse Signaling

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***Abstract*—Multi-Gb/s pulse signaling is demonstrated with inductively coupled interconnects across packaging interfaces. This has application in realizing submillimeter pitch, true zero insertion force (ZIF) surface mount connectors, and sockets. The signaling data rate achieved in this system is from 1 to 8.5 Gbps, which depends on the 3-dB coupling frequency of the composite channel consisting of the inductive interconnections and the transmission lines. This paper presents the results of a set of experiments demonstrating this capability and describes the principles behind the design of inductively coupled sockets and connectors.**

***Index Terms*—3-dB coupling frequency, alternating current (ac) coupled interconnect, backplane connectors, fine pitch, impedance matching, inductive coupling, pulse signaling, sockets, zero insertion force.**

I. Introduction

THIS paper addresses the feasibility of using inductively coupled interfaces for high-speed signal connections in connectors and sockets, i.e., level 2 and 3 interconnections. So far, inductively coupled interconnects have mainly shown potential for multi-Gb/s signaling in level 1 interconnections, i.e., direct chip to chip communication and 3-D integrated circuit (ICs) [1]–[6].

The basic concept is shown in Fig. 1 [7], [11]. Inductors are fabricated on two opposing surfaces, e.g., the faces of a connector or socket. When mated, they form a transformer, which is used to carry signals through the mated interface. The main advantage of building a separable connection this way, is that it is possible to achieve a high density with a simple mechanical structure. This in turn, offers potential for cost reduction and support for true 3-D packaging. Being a true zero-insertion force interface, very high pin counts could be easily supported. It is difficult to use capacitive coupling for this application, because the structure is placed in the transmission line, not at one end. Thus, both the driving impedance and load being driven is 50 Ω. The high, frequency-dependent impedance of a series capacitor $(1/\omega C)$ would lead to reflection noise (i.e., return loss). Unless large capacitors, or lossy codes guaranteeing only high frequency content, are used the transmitted swing would be too small (i.e., excessive insertion loss). In contrast, inductively coupled connectors can achieve a broadband matching impedance and give acceptable values to return and insertion losses. The main contributions of this paper are a presentation of the design principles behind this technology and a description of the results of a set of experiments, showing the potential for high-frequency operation. Section II discusses signaling choice for inductive connectors. Section III discusses performance needs for connectors. Section IV discusses transformer modeling and optimization to achieve good signal integrity. Section V discusses experimental work. Section VI discusses future potential and system level application.

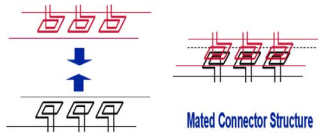

Fig. 1. Inductively coupled connector interface.

II. Signaling Options for an Inductive Connector System

Transformers can be used, in theory, either for nonreturn to zero (NRZ) or pulse signaling. Step response is illustrated for the two cases in Fig. 2. The input signal in our system is broadband conventional digital NRZ data; output waveform from the transformer can be faithfully reproduced NRZ or pulses depending on the value of inductance. An ideal transformer is a high pass filter and the value of inductance sets the 3-dB high pass coupling frequency for the filter. NRZ signaling with a transformer in a 50-Ω system needs fairly large values of inductances to be able to couple data across a wide band of frequencies from close to direct current (dc) to the knee frequency corresponding to the digital edge. As shown in Fig. 3, when inductance values approach 500 nH there is minimal low frequency attenuation in the forward power transfer (S21) and this would lead to faithful reproduction of the input NRZ waveform. However it is impractical to realize 500-nH inductance values in available board level processes in submillimeter pitch footprints. For example, the maximum inductance realizable in a process with 25-μm trace width/space and 75-μm microvias in a 775-μm outer diameter is 22 nH.

The most realistic option for submillimeter pitch inductive connector system is pulse signaling. All the information in a

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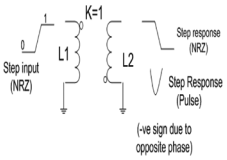


Fig. 2. NRZ and pulse signaling across a transformer.

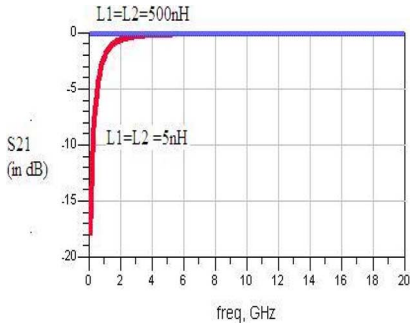


Fig. 3. Frequency response for ideal transformer in Fig. 2.

digital signal is in the high-frequency content of the edge. When passed through a low-inductance transformer, the edge becomes a pulse. This information can be used to detect a 1–0 and 0–1 transition. A transformer realized with small inductance values ranging from 1–5 nH can be used to read high frequency information in the edge while attenuating low-frequency components. This can be used to convert input step to pulses as shown in Fig. 2. These pulse waveforms can then be recovered back to NRZ through circuit techniques [12]. Transformers with outer diameters ranging from 260 to 460 μm can be used to achieve 1–5 nH inductances in a printed circuit board (PCB)/package process with 25-μm minimum trace width and 50-μm microvias. In addition to PCB/package process constraints the choice of transformer outer diameter also depends on the gap spacing.

III. Electrical Performance Requirements for a Connector/Socket

In simplistic terms the goal of a good connector is to achieve maximum forward signal transfer with minimal reflections from discontinuities. For example, the goal of the transformer used as a connector is to achieve useful values of insertion loss (S21) and return loss (S11), as described in Sections IV–VI. Exact numerical values desired are specific to the channel and dictated by the attenuation budget, signal-to-noise ratio requirements, bandwidth, and signaling data rate. Fig. 4 shows a block diagram of a typical backplane connector channel with two inductive connectors in the transmission path. Single ended signaling is assumed in this work.

Reference [8] suggests a method for establishing acceptable *S*-parameter specifications for connectors by correlating time domain and frequency domain performance metrics. For X Gbps NRZ signaling, S21 values better than -4 dB are recommended until X GHz for the value segment products. S11 values better than -10 dB are recommended until $0.7*\mathrm{X}$ GHz and values better than -6 dB between $0.7*\mathrm{X}$ to X GHz. These

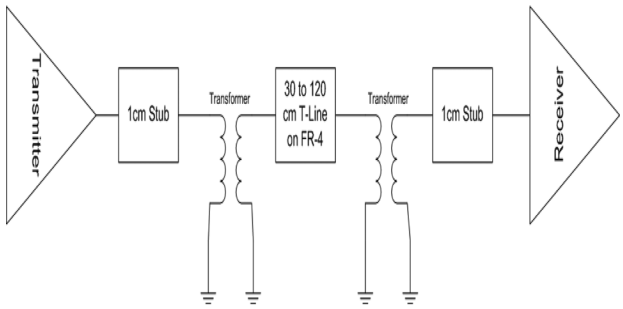


Fig. 4. Inductive connector system block diagram.

metrics are for X Gbps NRZ signaling and have to be adapted for X Gbps Pulse signaling. With the low inductances, suited for pulse signaling, there will be addition attenuation as well, as can be seen in Fig. 3. With pulse signaling, the objective is to have sufficiently low losses so that the signal to noise ratio at the receiver is acceptable. Custom pulse receiver circuits as discussed in [12] are assumed in this work. A typical requirement for a pulse receiver circuit is 200-mV peak-to-peak input signal with SNR ratio better than 20 dB for recovery to NRZ.

IV. Transformer Modeling and Optimization

A. Transformer Model

High-fidelity transformer models are necessary in order to obtain useful performance predictions. The elements in the model depend on the geometry of the inductor coils, the substrate they are realized on and return paths. Fig. 6 shows the baseline circuit model adopted in this work which correlates with representative transformer physical geometry shown in Fig. 5. The return paths can be dc or capacitively coupled. Here, L represents the inductance of the primary and secondary coils assuming they are equal, K represents the magnetic coupling coefficient between the coils, Cc is the crossover capacitance arising due to the overlap area of the two coils, Cp is the parasitic capacitance to ground for the coils, and R is the winding resistance for the coils. The model can be expanded to distributed structures by cascading multiple sections of the lumped model. Electromagnetic (EM) tools like Sonnet [15] or HFSS [14] can be used for modeling distributed structures. The choice of whether to use a lumped model or a distributed model must be made based on the electrical length of the structure. For example the edge rate in most high-speed digital applications is ~ 70 ps. This sets the knee frequency at 7 GHz. If the electrical length of a structure is less than or equal to 1/10 of operating wavelength at 7 GHz then a lumped model would suffice, else distributed or EM modeling is needed. The model in Fig. 6 ignores skin effect. Skin effect should be modeled for thicker metallization while it can be ignored for thinner metallization. A ladder network could be used to include skin effect. In this paper the structures were small enough that only lumped models were needed.

B. Transformer Optimization

1) Choice of Inductance Value: The choice for the nominal inductance value is driven by a tradeoff between signal ampli-

Fig. 5. Transformer geometry.

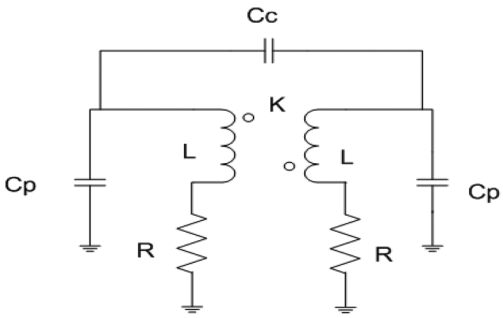


Fig. 6. Equivalent circuit model.

TABLE I
TRADEOFF BETWEEN DATA RATE AND SIGNAL AMPLITUDE

L1 = L2 = L(nH)	Settling time to 10% of peak voltage (nsec)	Peak Voltage (mV)
1nH	0.190 nsec	183.5mV
5nH	0.561 nsec	393.5mV
15nH	1.5 nsec	460mV
25nH	2.45 nsec	475mV

TABLE II
SAMPLE GEOMETRIES FOR REALIZING 1 AND 5 nH INDUCTANCES IN A PCB PROCESS WITH 25-μm MINIMUM TRACE WIDTH AND 50-μm MICROVIAS

1nH Inductance	**5nH Inductance**
Outer Diameter = 260μm	Outer Diameter = 460μm
Trace Width, Spacing = 25μm, 25μm	Trace width, Spacing = 25μm, 25μm
No. of Turns = 2	No. of Turns = 4

tude and signaling data rate. Table I summarizes peak voltage and settling time obtained from step response of an ideal transformer in response to 1-V peak input with 100-ps edge rate. For example a transformer realized with 5-nH inductors takes 0.561 ns to decay down to 10% of its peak voltage. If we can tolerate 10% of intersymbol interference (ISI) between adjacently transmitted data bits, this implies a 1.78-Gb/s peak signaling data rate. Faster decay times are achieved with 1-nH inductors with the tradeoff being reduced signal swing. The attenuation budget of the end system the connector is deployed in will determine the engineering tradeoff in choosing appropriate values of inductance. The ISI could also be reduced through active equalization, but that approach is not addressed in this paper. Table II summarizes sample geometries for realizing a 1- and a 5-nH inductance.

2) Optimizing Frequency Response and Step Response: High magnetic coupling coefficient values (k) are desirable in inductively coupled connectors for improving insertion loss and return loss, and increasing bandwidth. A real world transformer

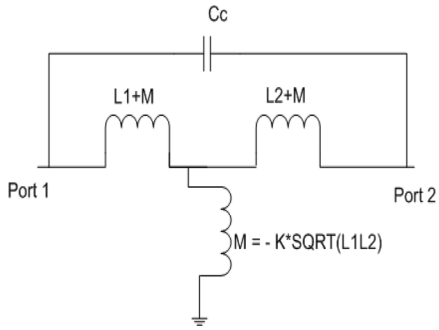


Fig. 7. Transformer circuit model (assuming opposite winding phase).

does not have a perfect coupling coefficient, due to the minimum required gap spacing between the inductors, and the resulting leakage inductance causes high-frequency roll-off in the forward transfer function (S21) and degrades the return loss (S11) as well. Test-structures designed in this work had outer diameters ranging from 100 to 500 μm to achieve a K ranging from 0.6 to 0.9 across a 5-μm gap spacing. A series capacitor is a high-pass filter and this can be used to compensate for the high-frequency roll off in the forward transfer function and also to tune the return loss. Series crossover capacitance (Cc) inherent in the transformer physical implementation, due to the parallel plate overlap area can be used to tune the frequency response. Iterative simulations with simple lumped transformer models can be used to determine values of crossover capacitance which achieve best case values of S21 and S11.

The impact of Cc on performance can be analyzed independently of the winding resistance and shunt parasitic capacitance. Fig. 7 shows a simplified transformer model without winding resistance and shunt parasitic capacitance. This simplification is to help in deriving manageable closed form expressions for *S*-parameters and transfer functions. The transformer model in Fig. 7 can be viewed as a parallel combination of the transformer T-circuit model and crossover capacitance assuming both these elements share a common ground return path. Equivalent ABCD network can be determined for this network and then converted to *S*-parameters, as in [19].

S-parameter equations derived from first principles using ABCD chain parameter computations for transformer models are unwieldy. This makes it hard for the designer to gain an intuitive understanding of channel optimization. In this respect the voltage transfer function is more useful. Nevertheless, *S*-parameters are a valuable source of guidance early on in the design process to help the designer identify potential sources of discontinuity and problem spots in the frequency domain. Once this is accomplished it is more informative to look at transfer functions and step response. Fig. 8 shows the input impedance plot obtained using Agilent design system (ADS) as a function of Cc with fixed values of L1, L2, and K in the circuit model in Fig. 7. When the value of Cc is 10 fF impedance profile is rising (inductive) and this would lead to S11 degradation. When the value of Cc is 400 fF impedance ranges from 40 to 56 Ω over a narrower bandwidth of 2.2–4.2 GHz. When the value of Cc is 200 fF impedance ranges from 40 to 60 Ω between 3–9 GHz

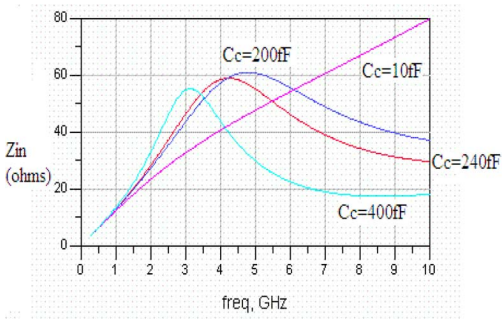


Fig. 8. Input impedance versus frequency for model in Fig. 7 ($L1 = L2 = 2$ nH; $k = 0.7$; Cc varies from 10 to 400 fF).

and S21/S11 can be optimized in this bandwidth. For this transformer, a nominal value for Cc of 200 fF is a good choice.

When the value of Cc changes to 240 fF, i.e., a 20% variation over a nominal value of 200 fF the input impedance shows variation of 1–9 Ω between 4.5–10 GHz. Process variations is another issue to be mindful of when designing inductive connectors for real world applications and impedance variations should be within $\pm 10\%$. Equation (1), at the bottom of the page, shows the voltage transfer function H21(s) for a simplified transformer model without shunt parasitic capacitance and winding resistance shown in Fig. 7. The term $(L1L2 - M^2)$ is proportional to leakage in the transformer system and the product of this term with Cc in the numerator of (1) impacts the zeros of the transfer function $\left(s = \sqrt{(M)/(L1L2 - M^2)Cc}\right)$. When the leakage inductance is very small, Cc has no impact upon the system zero but it still impacts the system poles. This implies that Cc has almost no effect on controlling reflection noise in the system. As the leakage inductance grows Cc has more control over reflection noise in the system.

$$\frac{((L1L2-M^2)Ccs^2-M)R_Ls}{ACcs^3+(L1L2-M^2+BCc)s^2+(R_sL2+R_LL1)s+R_sR_L} \quad (1)$$

where $A = (L1L2 - M^2)(R_s + R_L)$ and $B = (L1 + L2 + 2M)R_sR_L$.

From *S*-parameter or Input impedance plots a range of useful values of Cc can be identified to tune the system response. However, a point to note is that excess crossover capacitance can negatively impact transformer step response due to overshoots and oscillations. Hence the value of crossover capacitance used to tune the frequency response should be as small as possible without introducing overshoots or oscillations in the step response. Pole zero plots derived from the transfer function in (1) can also be used to determine values of Cc which make system response underdamped or unstable which introduces overshoots or oscillations in the system transient response. The transfer function in (1) is a third-order system and hence the system response can be more complex than a second-order system depending on dominant poles and their relative proximity to each other as well. An overdamped system has no overshoots in its transient response. From this analysis an upper bound can be established on values of Cc that can be used to tune the system.

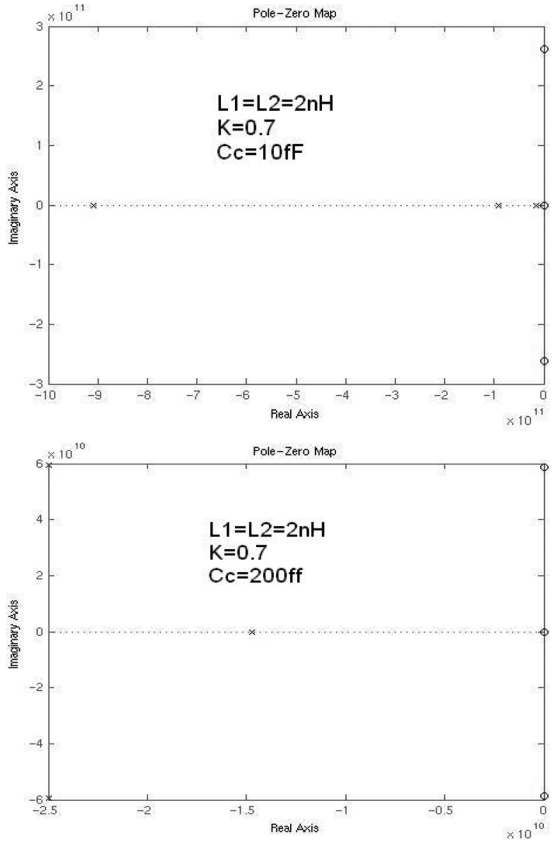


Fig. 9. Pole zero plots obtained from (1) ($L1 = L2 = 2$ nH; $K = 0.7$; Cc varies from 10 to 200 fF; 50-Ω system).

The poles of the transfer function convey information about the nature of the response. When $\mathrm{Cc} = 10$ fF the system poles are real and distinct as shown in Fig. 9 and the system is overdamped. When $\mathrm{Cc} = 200$ fF the system has real and complex conjugate poles. In this case, system response depends on the dominant poles. The dominant poles are the ones located closer to the origin. Since the real pole is located closer to the origin in this case it is expected that this system will have an overdamped response. When $\mathrm{Cc} = 400$ fF the system has real and complex conjugate poles but in this case the complex poles are located closer to the origin. This is shown in Fig. 10. Hence it is expected that this system will have an underdamped response with one or two overshoots before settling to steady state value. This in turn reduces the SNR of the system and introduces sources of error in the interconnect channel. From these pole zero plots the designer can ensure that the choice of values of Cc used to tune input impedance or frequency response do not cause the system response to be underdamped. A more rigorous discussion of pole zero plots for different values of termination can be found online[2] for the interested reader. Fig. 11 shows step response derived from (1) in a 50-Ω system with Cc varying from 100 to 400 fF.

In Fig. 11 the magnitude of the overshoot approaches $1/10$ of the signal swing when the crossover capacitance is 400 fF. This is the region where the system response is underdamped

[1]http://www.lib.ncsu.edu/theses/available/etd-03292004-140152/unrestricted/etd.pdf

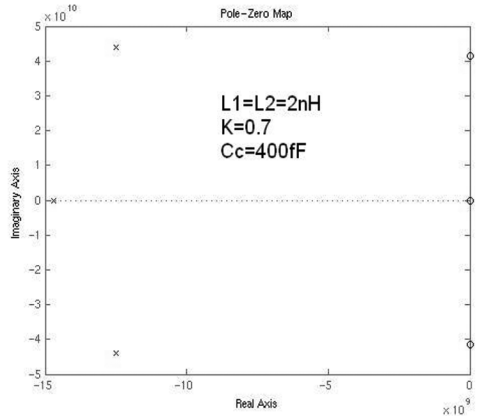


Fig. 10. Pole zero plots obtained from (1) ($L1 = L2 = 2$ nH; $k = 0.7$; Cc $= 400$ fF; 50-Ω system).

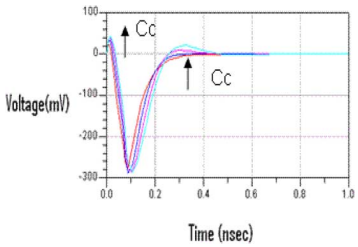


Fig. 11. Step response derived from (1) for a 70-ps edge: $L1 = L2 = 2$ nH; $K = 0.7$; Cc varies from 100 to 400 fF.

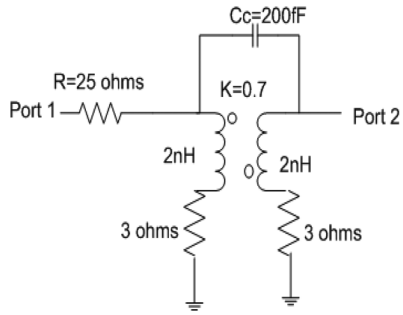


Fig. 12. Transformer model (with series termination and Cc).

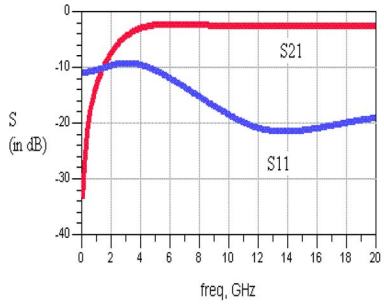


Fig. 13. Frequency response showing broadband impedance matching for the structure shown in Fig. 12.

as observed in the pole zero plots. Optimizing crossover capacitance helps in high-frequency impedance matching. Controlling the low frequency return loss needs lossy elements like a series resistance since electrically a transformer is a short-circuit at dc.

Fig. 13 shows that broadband $S11 >= -10$ dB for a baseline transformer circuit model shown in Fig. 12 can be achieved through a combination of 25 Ω series termination and 200 fF series crossover capacitance. Operating at multi-Gb/s speeds needs fast settling times for the inductors and based on Table I the inductance value should be intermediate between 1–5 nH. Inductance values of 2 nH and magnetic coupling coefficient values of $k = 0.7$ are reasonable assumptions for an inductive connector system built in packaging interfaces to operate at multi-Gb/s speeds. The threshold on the acceptable value of K varies on a case by case basis and is specific to the attenuation budget of the system (i.e., single connector system or two connector system, etc.) and the reflection noise tolerance of the system (i.e., the extent of degradation introduced by series leakage inductance). An approximate rule of thumb is to keep leakage inductance term in the transformer T-circuit model <1 nH, the faster the edge rate this requirement becomes more stringent. Cc value of 200 fF is nominal for impedance matching in the 3–9 GHz band and also the transient response is overdamped with this choice of Cc.

Too low a value of series termination provides no benefits for impedance matching while too high a value attenuates the signal transmitted to unacceptable levels. Hence, an intermediate value of 25 Ω is used in this simulation. The transformer model parameters shown in Fig. 12 can be realized in small electrical winding lengths and can thus be represented with a lumped model. The nominal transformer geometry that corresponds to $L1 = L2 = 2$ nH, $k = 0.7$, and Cc $= 200$ fF is shown in Table III. The transformer geometry shown in Table III can be realized in an aggressive laminate technology with 25-μm minimum trace width and 50-μm microvias[3]. Here, the gap spacing is assumed to be 25 μm and dielectric constant of the material in the gap is assumed to be 4.0. A gap spacing of 25 μm is a realistic estimate for spacing between two printed circuit boards with a surface roughness ranging from 1 μm to 5 μm with a thin coat of polyimide acting as a spacer. Based on empirical trends observed in ASITIC simulations, a transformer outer diameter alteast 10 times the gap spacing is needed to achieve a K of 0.5 across this gap spacing. Polynomial curve fits obtained from ASITIC plots of K versus gap spacing can be used to be understand relationship between these parameters for different transformer geometries. These relationships can be used by the designer as rules of thumb [7], [18]. Magnetic coupling is a complex function of several geometrical parameters and 3-D EM simulations should be used for higher accuracy. A generic choice of transformer geometry with 370 μm outer diameter with 25 μm trace width/spacing fails to achieve a K of 0.7 and also falls short of achieving a 200 fF crossover capacitance. This geometry is documented in Table III for purpose of comparison with the nominal geometry. In order to boost the crossover capacitance, the trace width was increased to 47 μm. Increasing the trace width means a reduction in Inductance and hence a higher loop area is required to realize a 2 nH inductance with wider traces. The additional loop area is also needed to increase K from 0.6 to 0.7. Several references in the literature capture closed form expressions for transformer circuit model elements

[2]see http://www.endicottinterconnect.com/hyperBGA.php and http://www.sanmina-sci.com/

TABLE III
TRANSFORMER GEOMETRY TO ACHIEVE $L1 = L2 = 2$ nH; Cc $= 200$ fF; $K = 0.7$ ACROSS A 25-μm DIELECTRIC SPACING WITH A DIELECTRIC CONSTANT OF 4.0; 25 μm MINIMUM TRACE WIDTH; 50-μm MICROVIAS

Outer Diameter (D in µm)	W/S (in µm)	Number of Turns	K	Cc (fF)
370	25/25	2	0.60	88.85
460	**47/25**	**2**	**0.70**	**200.3**

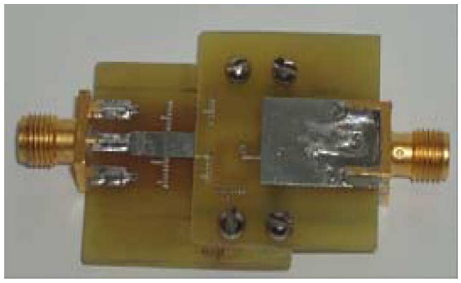


Fig. 14. Inductive connector channel prototype.

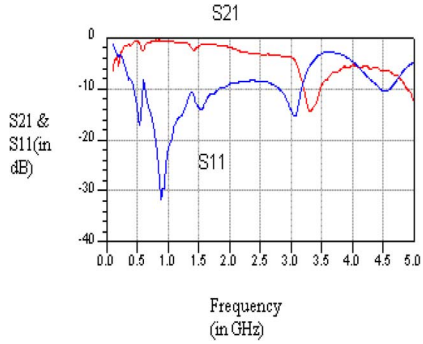


Fig. 15. Measured *S*–parameter data from 200 MHz to 5 GHz.

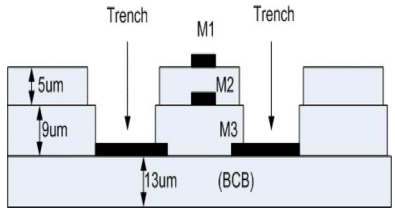


Fig. 16. Three-layer substrate process with buried bumps (2-μm–thick copper metallization and BCB dielectric with Er $= 2.65$).

and these equations can be used to obtain quick first pass estimates while designing transformer geometries [17]–[19].

Integrating a series resistance of 25 Ω is hard through geometrical optimizations for a spiral inductor on PCB due to minimum trace widths of the order of 25 μm. Options include using an embedded resistor or building inductor coils with thin metallization to increase series resistance on organic substrates. These results show that broadband impedance matching can be achieved for an inductive connector through Cc and series termination optimization and Table III also documents geometrical details of a nominal structure to build this in a 1-mm laminate technology. Since an inductive channel is frequency dependent, numerical optimization of model parameters requires extensive simulation on a case by case basis specific to the edge rate and signaling data rate of the system. The transfer function in (1) can be plugged in a TDR simulation setup to determine precise numerical values of Cc and series termination to minimize reflection noise. SNR values can be tabulated and analyzed for different cases.

V. EXPERIMENTAL WORK—INDUCTIVE CONNECTOR PROTOTYPES

Proof of Concept

Coarse pitch inductive test structures built on low-cost PCBs were used to establish feasibility for inductive connectors through radio frequency and digital measurement. The complete details were reported in [7] and are summarized briefly in this section. Fig. 14 shows test setup for a 10-mm outerdiameter inductive connector prototype used to establish proof of concept. Fig. 15 shows measured *S*–parameters for the experimental prototype shown in Fig. 14 from 200 MHz to 5 GHz. Return loss is better than or equal to -10 dB from 500 MHz to 3 GHz, and insertion loss is better than or equal to -3.7 dB from 220 MHz to 3 GHz. These performance metrics offer potential for deployment as backplane connectors [8].

Inductive elements have to scale down to submillimeter pitches and higher data rates to have potential for supporting higher data rates. Building submillimeter pitch inductive test structures needs printed circuit board processes with 1–2 mm feature size traces and 50-μm microvias. Lacking ready access to fine line laminates at the time this project was performed; thin film structures were fabricated to provide structures of the same dimensions. The remainder of this section is used to describe these experiments.

A. Fine Pitch Inductive Connectors

Inductive test-structures were fabricated in a three metal layer substrate process with similar physical structure, assembly, and layout to the one reported in [13] and shown in Fig. 16. The buried solder bumps are used to provide signal/ground connections, self-align the inductive coils, and also control the air gap spacing between the substrates. They are only present to facilitate the experiment; they would not be used in a final structure. Benzocyclobutene was used as the dielectric material because of its low permittivity and excellent planarizing properties. The top metal layer was used for the inductive I/O structures while routing was through 50-Ω striplines on the inner metal layer.

One of the substrates was flipped onto its corresponding mating sample with buried bumps to create the test interface for characterizing inductive coupling. Fig. 17(a) shows a cross-sectional view of the test setup and Fig. 17(b) shows a sample photo of an inductor on the bottom substrate.

Transformers of various outer diameters with geometrical variations on trace width/space were built on the substrate. Inductance values were optimized to achieve Gb/s 2 + signaling speeds with sufficient signal swing. Capacitive tuning was achieved by varying transfomer outer diameter and trace width. Transformer geometrical variations were designed based on exhaustive EM, lumped model simulations to achieve

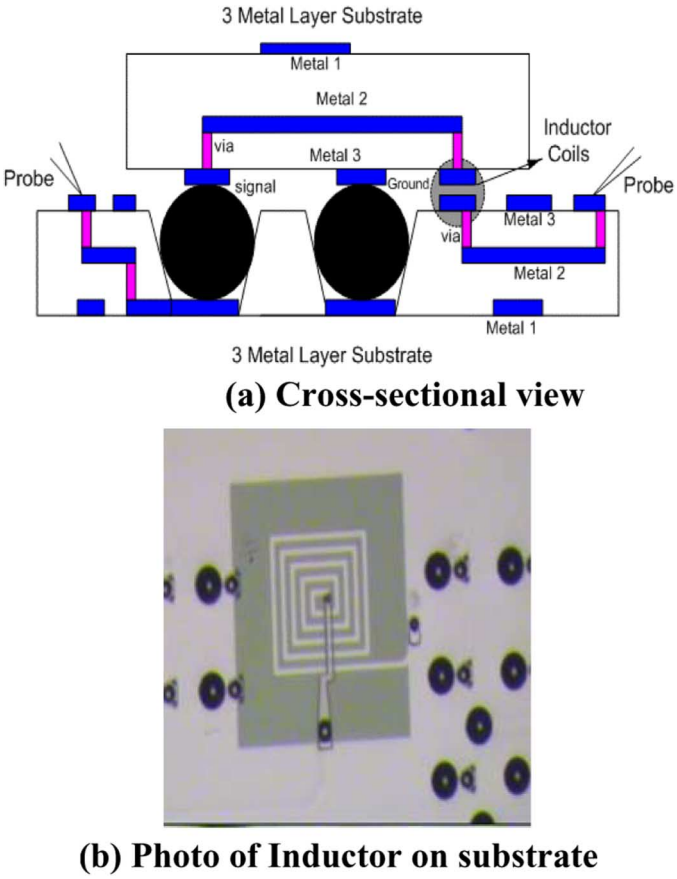


Fig. 17. Test frame for characterizing inductive coupling using fine line geometries. This is not intended to represent what an inductively coupled connector might look like.

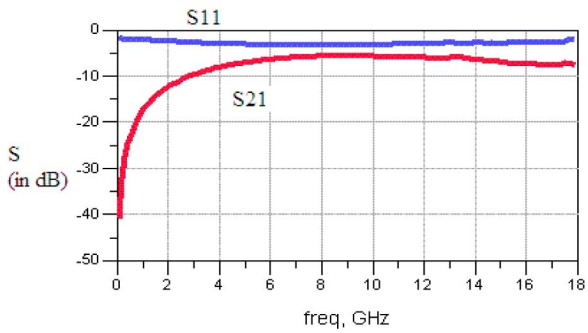


Fig. 18. Measured data for a 100-μm-diameter transformer (SB1_11a) (with 1.22-nH inductors realized with 5-μm trace width/space) across a gap spacing of 5–7 μm.

$K >= 0.6$ across 5–7 μm air gaps with minimal parasitics. This is comparable to the spacing expected in an inductively coupled laminate assembled, as shown in Fig. 14. The shunt capacitive parasitics (Cp) for the transformer structures were minimized by keeping ground return structures away at a distance of 1/4 the outer diameter of the inductor coils. Fig. 18 shows S21 and S11 measurements for a 100-μm–diameter transformer (named experiment "SB1_11a").

The 3-dB bandwidth of this structure is as high as 15.2 GHz since the capacitive parasitics and leakage inductance are minimal. Figs. 19 and 20 show the measured eye diagram for transformer SB1_11a for $2^7 - 1$ PBRS data at 4.25 Gb/sec and 8.5 Gb/s with 25-ps edge rates. These clearly show the pulse nature of the signals. Time domain measurements were made with an Agilent N4901b serial BERT and a Tek11801A oscilloscope. As expected with small inductance values, the decay rate is fast and this enables high speed operation. Eye closure is more severe at 8.5 Gb/s compared to 4.25 Gb/s due to more ISI.

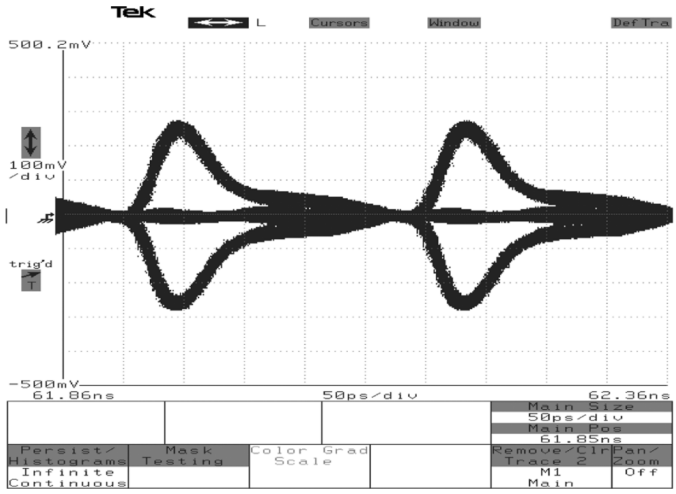


Fig. 19. Measured data for a 100-μm-diameter transformer (SB1_11a) (with 1.22 nH inductors realized with 5-μm trace width/space) across a gap spacing of 5–7 μm: Eye diagram at 4.25 Gb/s.

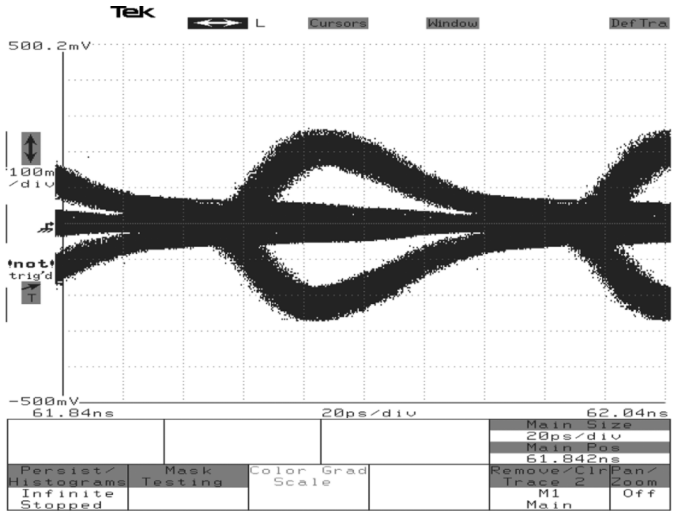
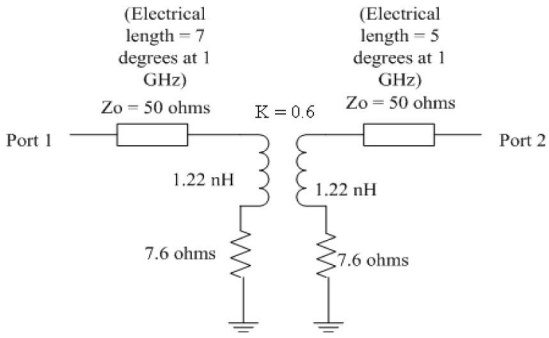


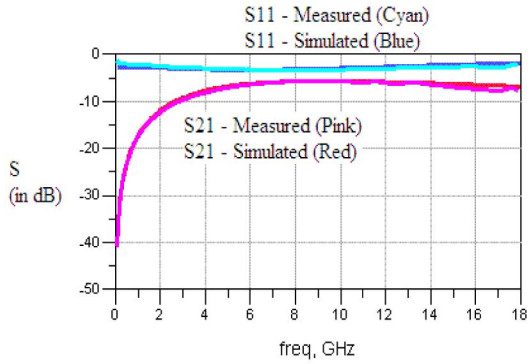
Fig. 20. Measured data for a 100-μm-diameter transformer (SB1_11a) (with 1.22-nH inductors realized with 5-μm trace width/space) across a gap spacing of 5–7 μm: Eye diagram at 8.5 Gb/s.

Fig. 21(a) shows the electrical model for the transformer SB1_11a. Values of magnetic coupling coefficient (K) and inductance in the model were extracted using ASITIC.[1] Shunt capacitive parasitics are very small and make minimal impact on the model since the inductor is on a low loss substrate as opposed to conductive silicon. Also the ground plane is removed in the area immediately surrounding the inductor to reduce shunt capacitive parasitics and to prevent eddy currents. The dc resistance at port 1 was measured to be 7.5 Ω which correlates

[3]http://rfic.eecs.berkeley.edu/~niknejad/asitic.html



(a) Lumped circuit model



(b) Measured vs Simulated S21, S11 (Mag)

Fig. 21. Measured versus simulated results for 100-μm-diameter transformer (SB1_11a).

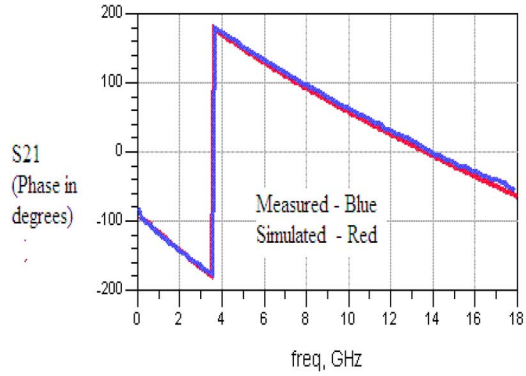


Fig. 22. Measured versus simulated S21 for SB1_11a (phase).

TABLE IV
SUMMARY OF TRANSFORMER MEASUREMENTS ON SB1_11A

Transformer Sample # (100µm Outer Diameter)	Inductance (from ASITIC)	3dB high pass coupling frequency	3dB bandwidth	AC Coupled eye opening
SB1_11a	1.22nH	3.6GHz	15.2GHz	400mV pp @ 4.25 Gb/sec 200mV pp @ 8.5 Gb/sec

closely with 7.6 Ω predicted in the model. Fig. 21(b) shows the measured versus simulated S21 and S11. Fig. 22 shows the measured versus simulated phase. The results for S21 more than meet acceptable requirements for connectors. However, the results for S11 do not—the reasons are discussed below at the end of this section. Lossless transmission line models from ADS [16] were used to include the effect of the 50-Ω feedlines from the probe pad to the inductor. The lengths of the feedlines are asymmetric since there are multiple columns of inductor experiments which need to be routed to corresponding probe pads. Note that a simple circuit model provides a broadband match from 50 MHz to 18 GHz for both phase and magnitude information due to the lumped nature of the transformer. The electrical length of this structure is 1.1 mm and approaches 1/10 of the operating wavelength at only 17 GHz and hence lumped models are valid over two decades of bandwidth. This saves a lot of simulation time compared with full wave EM simulations needed in commercial connector design.Table IV summarizes measurements on experiment SB1_11a. We are able to achieve 8.5 Gb/s signaling with a 100-μm–diameter transformer which is built with 1.2-nH inductances. The 3-dB bandwidth is fairly high for this structure and this could help in scaling to higher data rates in the future, for example by using some equalization to reduce the pulse ISI

The return loss characteristics for structure SB1_11a is poor because the crossover capacitance between the two inductor coils in this measurement was too small. For example, the crossover capacitance is estimated to be 7–15 fF for structure SB1_11a from simple parallel plate formulas, and a value of 150–200 fF is needed to create an acceptable value of S11. Unfortunately, the yield was low and transformers of larger diameters with varying trace widths could not be characterized in this process. Since the intercoil gap spacing is fixed by the self aligned solder bumps, there is no degree-of-freedom in varying gap spacing and material dielectric constant. Varying the intercoil gap spacing to a different value needs a new fabrication run with a different value of solder ball diameter or trench depth. Improving the high-frequency return loss for this structure requires a boost in the crossover capacitance. This could be done by increasing trace width, increasing outer diameter, reducing gap spacing or increasing dielectric constant. Low–frequency return loss can be improved through a 20–50-Ω integrated series terminator. This resistor was not available in the thin film process we had access to.

VI. FUTURE POTENTIAL

The experimental work reported in Section V showed that a prototype of a fine pitch inductive connector could support signaling speeds up to 8.5 Gb/s. The 5-μm trace width/feaures available in the substrate process were used to realize 100-μm -diameter transformers with 1.2-nH inductance. In a laminate process with 25-μm trace width/space and 50-μm microvias a 1.2-nH inductance can be realized in a 275-μm diameter structure. This geometrical structure however only serves the purpose of achieving desired value of inductance. Transfer function analysis as discussed earlier in this paper is needed to determine optimum values of Cc and series termination for impedance

TABLE V
IMPLEMENTATION OF $\sim$ 1.2 nH INDUCTANCE WITH DIFFERENT FEATURE SIZES. LEFT COLUMN: THIN FILM PROCESS REPORTED IN THIS PAPER. RIGHT COLUMN: IN A COMMERCIAL HIGH DENSITY LAMINATE PROCESS

Prototype Case (SB1_11a) (Gap Spacing = 5~7µm)	**PCB/Package Process (Gap Spacing = 25µm)**
5µm/5µm Trace width/Space	67µm/25µm Trace width/space
Via size : 10 µm	Via size : 50 µm
100 µm Outer diameter	550 µm diameter
1.2 nH inductance (# of turns = 4)	1.15 nH inductance (# of turns = 1)

matching. Assuming that a nominal value of Cc of 200 fF and a K of 0.7 is desired across a gap spacing of 25 μm the transformer outer diameter and trace width have to be readjusted to achieve these values. Table V shows outer diameter required for realizing a 1.2-nH Inductance, Cc of 200 fF, and $K = 0.7$ in a package/PCB process. The dielectric material in the 25-μm gap spacing between the coils is assumed to have a dielectric constant of 4.0

VII. CONCLUSION

Multi-Gb/s pulse signaling is demonstrated with submillimeter pitch inductive connector prototypes. Series resistance tuning, capacitive tuning and inductance value optimization can lead to good signal integrity in inductive systems. ZIF submillimeter pitch surface mount inductive connector technology can address some of the problems inherent in press fit style connectors and be a viable option in the near future. Inductive connectors are well suited in custom applications where the air gap spacing, process feature sizes, and operating frequency range are well known.

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