Fig. 8, a reference design achieves 6.3% EVM for an output power of -3 dBm for sub-gigahertz ISM-band. Table I summarizes the UHF RF transceiver's characteristics. The specifications of two RF transceivers [9] and [10] for UHF applications are also shown for comparison in this table. The RX current is not the lowest, however, the power dissipation in RX mode is the smallest because of the 1.8-V supply voltage. Although the TX output power and RX IIP3 are a little worse due to the antenna switch and the matching network, this work have great advantages.

V. Conclusion

A low power fully CMOS integrated RF transceiver chip for WSNs in sub-gigahertz ISM-band applications is implemented and measured. The IC is fabricated in 0.18-μm mixed-signal CMOS process and packaged in LPCC package. The fully monolithic transceiver consists of a receiver, a transmitter, and an RF synthesizer with on-chip VCO. The overall receiver cascaded noise figure, sensitivity, and cascade IIP3 are 9.5 dB, -98 dBm, and -10 dBm, respectively. The overall transmitter achieves less than 6.3% error vector magnitude (EVM) for 40-kb/s mode. The chip uses 1.8-V power supply and the current consumption is 25 mW for reception mode ad 29 mW for transmission mode. This chip fully supports the IEEE 802.15.4 WPAN standard in sub-gigahertz mode.

References

[1] Y. K. Park, H. M. Seo, Y. K. Moon, K. H. Won, and S. D. Kim, "Low power radio receiver specifications of ubiquitous system for coexistence with various wireless devices in 2.4 GHz ISM-band," in *Proc. 20th Int. Techn. Conf. Circuits/Syst., Comput. Commun.*, 2005, pp. 150–151.

[2] S. Sarkar, P. Sen, A. Raghavan, S. Chakarborty, and J. Laskar, "Development of 2.4 GHz RF transceiver front-end chipset in 0.25 μm CMOS," in *Proc. 16th Int. Conf. VLSI Design*, 2003, pp. 42–47.

[3] P. S. Choi, H. C. Park, S. Y. Kim, S. C. Park, I. K. Nam, T. W. Kim, S. J. Park, S. H. Shin, M. S. Kim, K. C. Kang, Y. W. Ku, H. J. Choi, S. M. Park, and K. R. Lee, "An experimental coin-sized radio for extremely low-power WPAN application at 2.4 GHz," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2258–2268, Dec. 2003.

[4] C. Cojocaru, T. Pamir, F. Balteanu, A. Namdar, D. Payer, I. Gheorghe, T. Lipan, K. Sheikh, J. Pingot, H. Paananen, M. Littow, M. Cloutier, and E. MacRobbie, "A 43 mW bluetooth transceiver with -91 dBm sensitivity," in *ISSCC Dig. Tech. Papers*, 2003, pp. 90–91.

[5] M. Valla, G. Montagna, R. Castello, R. Tonietto, and I. Bietti, "A 72-mW CMOS 802.11a direct conversion front-end with 3.5-dB NF and 200-kHz 1/f noise corner," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 970–977, Apr. 2005.

[6] I. Nam, Y. J. Kim, and K. Lee, "Low 1/f noise and DC offset RF mixer for direct conversion receiver using parasitic vertical NPN bipolar transistor in deep N-well CMOS technology," in *IEEE Symp. VLSI Circuits Digest Techn. Papers*, 2003, pp. 223–226.

[7] Y. J. Jung, H. S. Jeong, E. S. Song, J. H. Lee, S. W. Lee, D. Y. Seo, I. H. Song, S. H. Jung, J. B. Park, D. K. Jeong, S. I. Chae, and W. Kim, "A 2.4-GHz 0.25 μm CMOS dual-mode direct-conversion transceiver for bluetooth and 802.11b," *IEEE J. Solid-State Circuits*, vol. 39, no. 7, pp. 1185–1190, Jul. 2004.

[8] P. Zhang, T. Nguyenbetta, and B. Razavi, "A 5-GHz direct-conversion CMOS transceiver," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2232–2238, Dec. 2003.

[9] W. Schuchter, G. Krasser, and G. Hofer, "A single chip FSK/ASK 900 MHz transceiver in a standard 0.25 μm CMOS technology," in *Proc. IEEE RFIC Symp.*, 2001, pp. 183–186.

[10] H. Komurasaki, T. Sano, T. Heima, K. Yamamoto, H. Wakada, I. Yasui, M. Ono, T. Miki, and N. Kato, "A 1.8-V operation RF CMOS transceiver for 2.4-GHz-Band GFSK applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 5, pp. 817–825, May 2003.

Voltage-Mode Driver Preemphasis Technique For On-Chip Global Buses

Liang Zhang, John M. Wilson, Rizwan Bashirullah, Lei Luo, Jian Xu, and Paul D. Franzon

***Abstract*—This paper demonstrates that driver preemphasis technique can be used for on-chip global buses to increase signal channel bandwidth. Compared to conventional repeater insertion techniques, driver preemphasis saves repeater layout complexity and reduces power consumption by 12%-39% for data activity factors above 0.1. A driver circuit architecture using voltage-mode preemphasis technique was tested in 0.18-μm CMOS technology for 10-mm long interconnects at 2 Gb/s.**

***Index Terms*—Global buses, low-power, on-chip, preemphasis, repeater insertion.**

I. Introduction

In high performance VLSI system designs, repeater insertion can be required for up to 80% of on-chip global interconnects [1]. As technologies continue to scale and operating frequencies continue to increase, the number of repeaters required increases exponentially to improve the signal bandwidth of interconnect channel and meet the delay goal of cross-chip communication [2]. Even with a suboptimal delay approach, repeaters still consume a significant amount of power and area and cause layout complexities [3]. Besides, delay latency from repeaters themselves undermines total signal delay improvement.

A hybrid current/voltage mode (CM/VM) on-chip signaling scheme with adaptive bandwidth capability was reported to minimize the number of repeaters [4], but it required pipeline latency to accommodate its computational data paths, and its power saving was not significant for low data activity interconnects. A similar current sensing technique was used in [5] for differential interconnects, but it consumed even more power than [4] did and its power dissipation performance was worse than that of the traditionalTYhis VM single-ended interconnects for data activity factors below 0.5. Therefore, these CM signaling schemes enhanced the interconnect bandwidth, but the static current path of CM signaling caused more total power dissipation at low data activity [6]. A VM low-swing differential interconnect architecture with distributed line equalization was reported in [7], but it increased the load of clock wires and had the same layout complexity problem as repeaters did.

Equalization techniques have been widely used for applications in chip-to-chip communication [8]. They compensate the frequency-dependent attenuation in lossy transmission lines to achieve higher data

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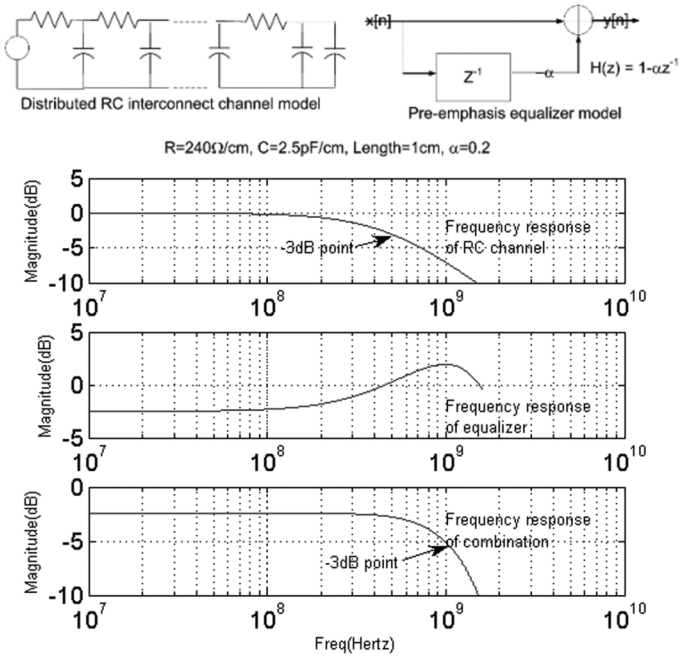

Fig. 1. Frequency responses of a distributed *RC* interconnect channel, preemphasis equalizer, and their combination.

rates. In this paper, a VM driver preemphasis technique is used to "deemphasize" the low frequency signal components on interconnects. It reduces inter-symbol interference (ISI) and signal swing. As a result, both the bandwidth and the power consumption of the interconnects are improved.

II. Theory Verification

ISI can be explained as a symbol on a channel corrupted by another symbol traveling on the same channel at an earlier time. For both a lossy transmission line channel and an *RC* interconnect channel, ISI happens when the energy stored from an earlier symbol sums with an unrelated symbol. From a frequency perspective, it happens when the attenuated high-frequency signal components in the channel are overwhelmed by the unattenuated low-frequency components. Hence, ISI can be countered by either emphasizing the high-frequency components or attenuating the low-frequency components, i.e., equalizing the channels.

A 1-cm long *RC* interconnect channel is modeled as a distributed *RC* line in Fig. 1 with designated parameters of resistance $R_0 = 240\,\Omega/\text{cm}$ and parasitic capacitance C_0 =2.5 pF/cm. Matlab simulation with *RC* delay formula [9] indicates it is a low-pass channel with -3 dB frequency at 0.5 GHz. The transfer function of the one-tap discrete feedforward equalization (FFE) model in Fig. 1 is $H(z) = 1 - \alpha Z^{-1}$. α is the equalization coefficient and determines the amount of attenuation. The frequency response of this equalizer shows low-frequency attenuation and high-frequency compensation at 1 GHz. By combining this equalizer with the *RC* channel, the system -3 dB frequency is improved from 0.5 to 1 GHz and the combined channel can be used for transferring 2 Gb/s nonreturn zero (NRZ) data.

To further verify the bandwidth improvement of this equalization technique, a channel with an equalized driver (driver preemphasis), and a channel with repeater insertion are compared in time domain in Fig. 2. (k-1) uniformly spaced buffers are inserted along the line as repeater insertion.

In Matlab simulation, delay t_ν is defined as the time from $(t = 0)$ to the time when the normalized voltage reaches threshold ν at the receiving end of the line. $t_{0.5}$ is used for repeater insertion by assuming transistors switch at $\nu = 0.5$ and $(t_{0.5} - t_{0.2})$ is used for driver preemphasis because equalized signals are attenuated and switch between $\nu = 0.2$ and $\nu = 0.8$. For a wide range of interconnect lengths and equally sized drivers and repeaters, the driver preemphasis technique results in lower delay latencies than repeater insertion. It achieves 411-ps interconnect delay at 10 mm, a 26% and 19% improvement over lines with one repeater $(k = 2)$ and four repeaters $(k = 5)$, respectively. Hence, driver preemphasis technique can be used instead of repeater insertion technique to achieve 2-Gb/s data rate at the given channel.

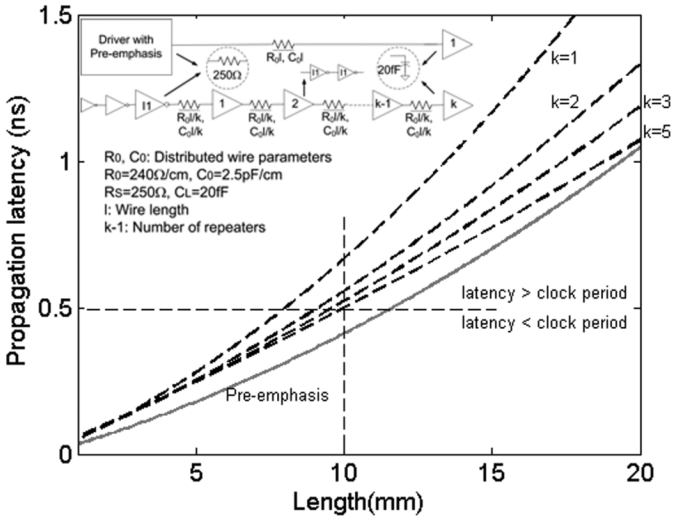

Fig. 2. Propagation latency comparison of driver preemphasis and repeater insertion.

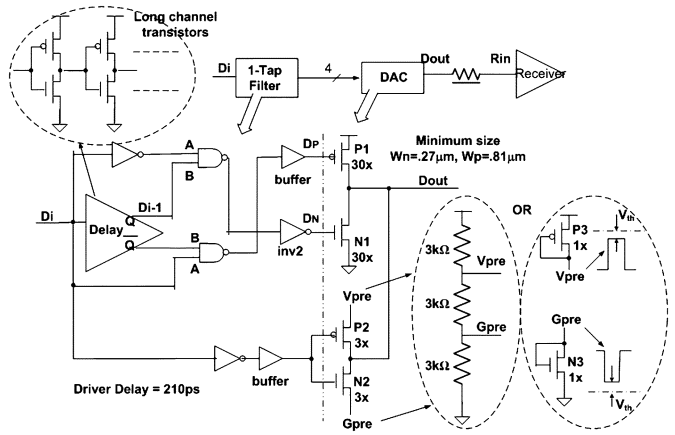

Fig. 3. Driver circuit with preemphasis.

III. Implementation

A. Preemphasis Driver

The driver circuit with preemphasis is shown in Fig. 3. Unlike a transmitter for chip-to-chip communication, an on-chip bus driver cannot afford a complicated equalizer design with significant power overhead. Our approach consists of a one-tap finite impulse response (FIR) filter and a simple digital analog converter (DAC).

The FIR filter checks whether the current symbol is different from the previous sent one and it determines whether the unattenuated driver

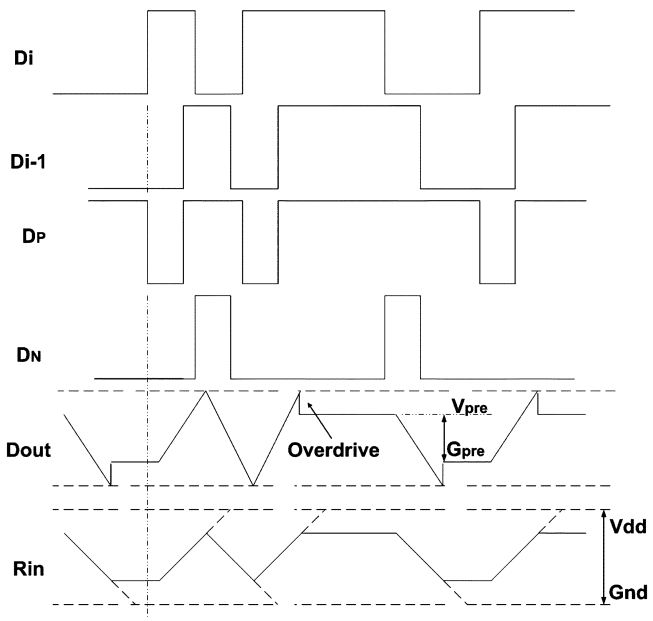

Fig. 4. Conceptual timing diagram.

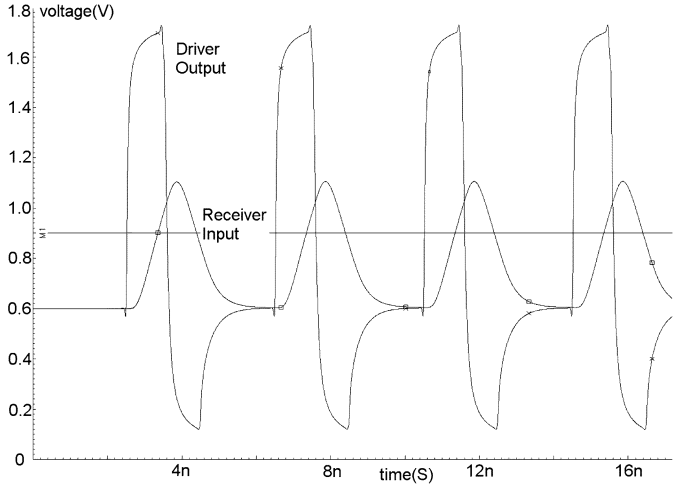

Fig. 5. Driver output and receiver input waveforms of preemphasis bus.

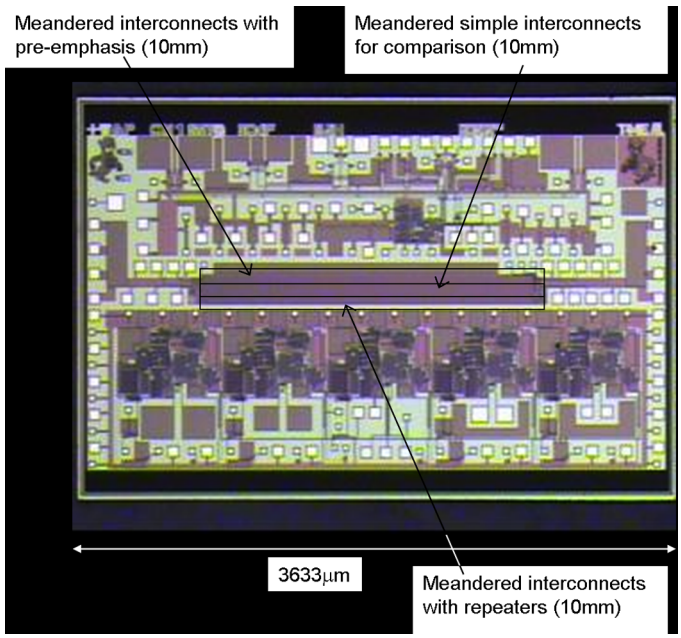

Fig. 6. Die photograph.

in DAC should be turned on. The DAC has one unattenuated driver and one attenuated driver. The unattenuated driver, tri-state gate P1/N1, is only turned on when there is a "0" to "1" or "1" to "0" transition and provides full signal swing at $D_{\rm out}$. To drive a 1-cm-long interconnect with $R_0 = 240\ \Omega/\text{cm}$ and $C_0 = 2.5$ pF/cm at 2 Gb/s and produce a swing from $V_{\rm pre}$ to $G_{\rm pre}$ at the receiver input, $R_{\rm in}$, P1/N1 is sized to 30x of the minimum transistor width ($W_{\rm min}$). The attenuated driver, P2/N2, is a normal output driver gate, but its output swing is from $V_{\rm pre}$ to $G_{\rm pre}$. P2/N2 only needs to keep this voltage level and they are sized to $3xW_{\rm min}$.

$V_{\rm pre}$ and $G_{\rm pre}$ can be provided by either a serial-resistor structure or diode-connected transistors. If the static power consumed on the serial resistors is shared by a 16-bit bus, it is only 0.01 pJ/bit at 2 Gb/s-data rate and is ignorable. Diode-connected transistors do not require any extra static power consumption, but they give up noise margin due to $V_{\rm th}$ variation. The dc points at both the driver output and the receiver input are dependent on $V_{\rm th}$. If $V_{\rm th}$ variation between the driver and receiver tracks each other, the dc points also track and cause no noise margin penalty, but slow N and fast P at one side and fast N and slow P at the other side will degrade noise margin.

Long channel transistors are used in the delay cell to detect a "0" to "1" or "1" to "0" transition. At slow process corners, the delay is larger and the signal pulses at nodes D_P and D_N are wider. It ends up with more preemphasis on driver output signal to compensate the process variation. While at fast corners, the output signal needs less preemphasis and the D_P/D_N pulses are narrower. The extra power overhead of the preemphasis driver is mainly from the delay cell in the FIR filter. It is less than 0.2 pJ/bit and is likely to further scale with technology.

Fig. 4 shows the conceptual timing diagram. Every previous sent bit determines the preemphasis. Data sequence does not need to be pipelined or delayed as in [4] before appearing at the bus input. Therefore, it does not introduce any extra clock period of latency into the timing. The overdrive shown in the Fig. 4 is the by-product of preemphasis. It increases signaling speed by providing a larger signal than required at the receiver input [7]. Fig. 5 shows the simulated waveforms of the driver output and receiver input. An equalized low-swing signal is achieved at the receiver end.

B. Demonstration

To match the designated parameters in the theoretical verification, $R_0 = 240\ \Omega/\text{cm}$ and $C_0 = 2.5$ pF/cm, meandered metal-4 lines in TSMC 0.18-μm CMOS technology with a length of 10 mm and width of 4.5 μm are used.[1]

The wires are shielded by metal-4 ground lines with 1-μm spacing and have inductance $L_0 = 3$ to 5 nH/cm. The greatness of the inductive effects is calculated based on the damping factor $\xi = R_0 l/2\sqrt{C_0/L_0} = 2.7 > 1$. It indicates the effect of the inductance on the circuit is small [15] unless even wider lines as used in [16] are considered. Design rules in [14] show the same result and the final silicon measurement does not observe inductive behavior.

Fig. 6 shows the test chip demonstrating a single channel 2-Gb/s preemphasis bus. Repeater bus and simple no-repeater bus with the same routing area are also included in the test chip as benchmarks.

[1][Online]. Available: http://www.oea.com/document/metal.pdf

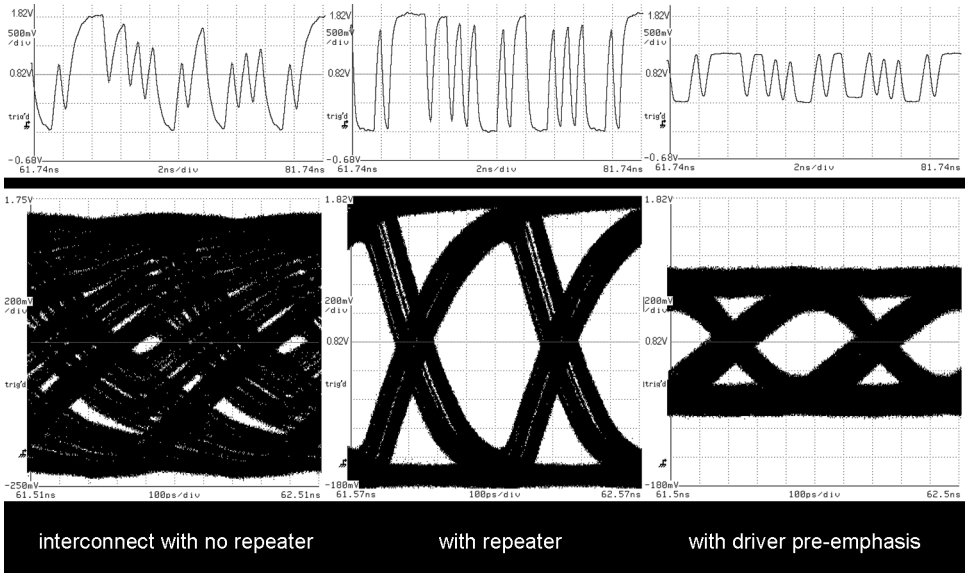

Fig. 7. Measurement results at the receiver input with a data pattern input and a 127-bit PRBS input (2 Gb/s).

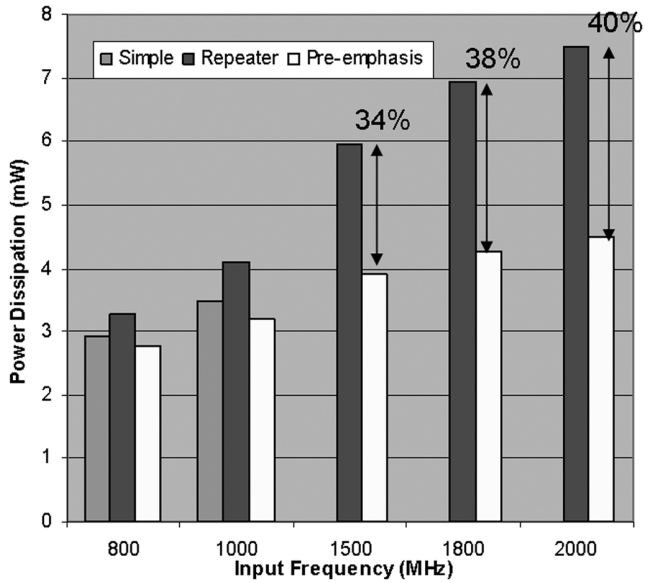

Fig. 8. Power dissipation measurement at different frequencies with PRBS input, data activity factor $= 0.5$ (the simple interconnect does not work above 1 Gb/s).

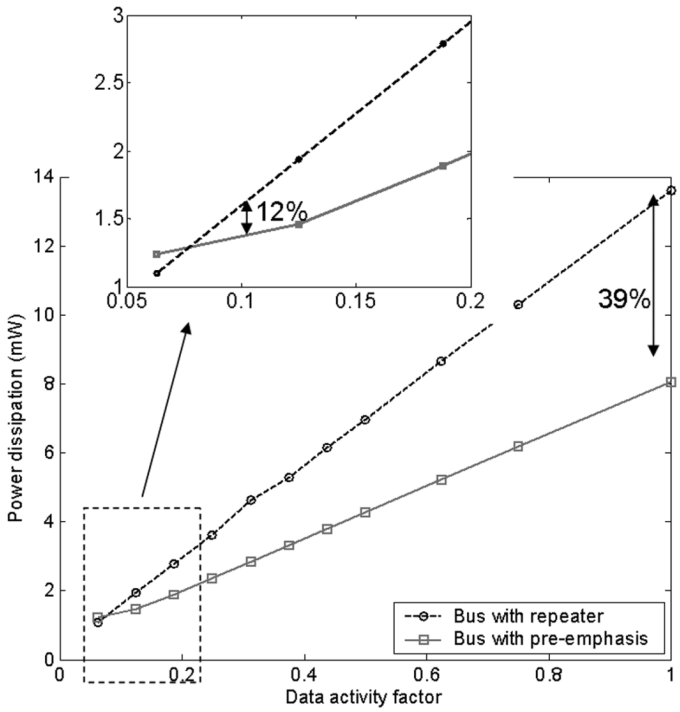

Fig. 9. Measured power dissipation at different data activity factors with 2-Gb/s data pattern input.

Data pattern profiles with different signal activity factors and a 127-bit pseudo-random binary sequence (PRBS) input are probed in from an Agilent 81134A source. The measurement results at the receiver input are shown in Fig. 7, simple bus with no repeater (left), repeater bus (middle), and preemphasis bus (right).

A data pattern is used for the waveform measurement to show ISI and the PRBS input is used for eye diagram measurement. At 2 Gb/s, the simple bus has severe ISI, resulting in eye closure. The repeater bus alleviates ISI by boosting the whole signal, while the preemphasis bus does this by attenuating the low-frequency signal components. Both approaches increase bandwidth, but driver preemphasis saves power. An interconnect delay latency of 420 pS is measured and matches the 411 pS Matlab simulation results.

Fig. 8 shows the power dissipation measurement for PRBS data (activity factor $= 0.5$) at different frequencies. The simple bus does not work above 1 Gb/s. The preemphasis bus decreases power consumption by up to 40% when compared to using repeaters. Fig. 9 shows the power dissipation measurement for 2-Gb/s data patterns with different data activity factors. For activity factors above 0.1, the use of driver preemphasis reduces power by 12% to 39%.

IV. Performance Evaluation

A. Bus Structures

In an on-chip signaling design, delay latency, data throughput, power, area, and noise are all important performance metrics. This section gives a further comparison between driver preemphasis and repeater insertion techniques based on the simulation results when the design metrics of power, area, and noise are included.

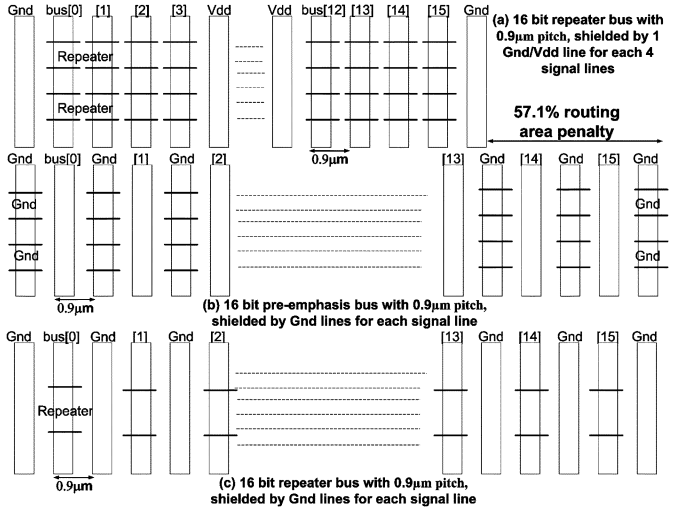

Fig. 10. 16-bit repeater and preemphasis bus structures, meanders and dummy underlying metal layers not shown.

A repeater bus structure with 0.9-μm pitch is shown in Fig. 10(a). It has shielding lines for every 4-bit signal lines to provide current return paths. Same wire width and spacing are assumed. The distributed *RC* model of 10-mm long and 0.45-μm wide metal-4 lines can be extracted as $R_0 = 1.73$ kΩ/cm, area and fringe capacitances to bottom layers, $C_{\rm bottom} = 0.388$ pF/cm, and the coupling capacitance between two neighboring lines, $C_{\rm coup} = 0.774$ pF/cm.[1] $C_0 = C_{\rm bottom} +$ CCMx$C_{\rm coup} = 3.48$ pF/cm is the total parasitic capacitance. CCM is the coupling capacitance multiplier factor. It can be 0, 1, 2, 3, or 4 depending on the transition direction of the two neighboring lines.

The worst CCM is 4 while both neighbors switch to the opposite direction. To look for the most power-optimal repeater insertion at a designated timing target, Lagrange's method, as used in [10] and [11], is performed. At 1nS wire delay, the optimal segment number $n = 5$ and the optimal repeater size $W = 36\times$Wmin are found.

Driver preemphasis results in low-swing signal. Unlike the low-swing schemes in [12], which generally sacrifice noise margin and bandwidth for power dissipation, our preemphasis technique improves bandwidth while trading off noise margin due to reduction in voltage swing. To quantify the worst case area penalty for preemphasis bus to achieve the same or better noise performance as full-swing bus, each signal line in Fig. 10(b) is fully shielded by ground lines with four distributed connections to top power metals. Therefore, preemphasis bus could take about 57.1% worst case area penalty comparing to repeater insertion bus in Fig. 10(a). The preemphasis bus has the same $R_0 = 1.73$ kΩ/cm, $C_{\rm bottom} = 0.388$ pF/cm, and $C_{\rm coup} = 0.774$ pF/cm, but with the worst CCM $= 2$ for fully shielded bus, $C_0 = 1.94$ pF/cm. A fully shielded bus structure is also proposed in Fig. 10(c) to compare the drive preemphasis technique with the repeater insertion technique at the same bus routing area. It has the same *RC* parameters as the preemphasis bus. The optimal repeater insertion segment number and the optimal repeater size are found at $n = 3$ and $W = 34\times$Wmin.

B. Performance Comparison

The performance of the three bus structures is compared in Table I based on HSPICE simulation. For structures (a) and (b), the preemphasis bus has a 57.1% area penalty, but it could save power consumption as much as 34.1% at a data activity factor of 0.15 [13] and removes all of the layout blockage and active area of repeaters. The repeater bus has 26%–49% of the worst case $(-+-)$ and best case $(+++)$ data-dependant delay variation comparing to the delay on a signal line with two quiet neighbors $(0+0)$. The preemphasis bus has negligible data-dependent delay and its intra-bus crosstalk noise is only one-tenth of the repeater bus crosstalk noise. The crosstalk numbers were obtained when one signal line is quiet and all the other lines switch in the same direction at the same time.

TABLE I
PERFORMANCE COMPARISON

	Repeater Bus with 0.9μm Pitch		Repeater Bus with full shielding		Pre-emphasis Bus with 0.9μm Pitch	
Driver+Wire+Receiver Delay (ns)		Δ		Δ		Δ
-+- (worst)	1.25	+26%	.856	+0.2%	.829	+0.4%
0+0	0.99	-	.854	-	.826	-
+++ (best)	0.50	-49%	.852	-0.2%	.823	-0.4%
Crosstalk (mV)	550		40		43	
Power (mW) (act=0.15)	1.02		0.74		0.67	
Width of routing area (μm)	18.9		29.7		29.7	
Driver delay (ns)	0.16		0.15		0.21	
Driver power (mW) (act=0.15)	0.05		0.05		0.22	
R(kΩ/cm)	1.73		1.73		1.73	
Cbottom(pF/cm)	.388		.388		.388	
Ccoup(pF/cm)	.774		.774		.774	
C0(pF/cm)	3.48		1.94		1.94	

For structures (b) and (c) with the same bus routing area, similar performance on delay variation and crosstalk is observed, but the preemphasis bus still saves 9.5% power at a activity factor of 0.15. The power saving decreases as the data rate decrease from 2 to 1 Gb/s.

Crosstalk on the preemphasis bus from full-swing signals is analyzed as a 16-bit full-swing bus crossing orthogonally beneath the preemphasis bus and switching in the same direction at the same time. This intra-layer noise is ignorable because the coupling capacitance is only 1 fF between the two layers.

C. Technology Scaling

As long as there is still signal noise margin to be traded off for power and bandwidth as $V_{\rm dd}$ and $V_{\rm th}$ scales, the voltage-mode driver preemphasis circuit scales. Multiple-$V_{\rm dd}$ and multiple-$V_{\rm th}$ algorithms have been investigated extensively to reduce power without drastically degrading circuit performance or increasing leakage current. This design trend can be naturally adapted to driver preemphasis technique, which requires an emphasis supply voltage for high-frequency signal components or an attenuation supply voltage for low-frequency components.

V. CONCLUSION

A driver preemphasis architecture for on-chip global buses was used to minimize the number of repeaters required to meet the goal of signal latency and throughput. For 10-mm Metal-4 interconnects at 2 Gb/s in TSMC 0.18-μm technology, it has no extra clock latency and obtains 12% to 39% power saving.

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REFERENCES

[1] R. Rusu and G. Singer, "The first IA-64 microprocessor," *IEEE J. Solid-State Circuits*, vol. 35, no. 11, pp. 1539–1544, Nov. 2000.
[2] J. Cong, "An interconnect-centric design flow for nanometer technologies," *Proc. IEEE*, vol. 89, no. 4, pp. 505–528, Apr. 2001.

[3] R. Ho, K. W. Mai, and M. A. Horowitz, "The future of wires," *Proc. IEEE*, vol. 89, no. 4, pp. 490–504, Apr. 2001.
[4] R. Bashirullah, W. Liu, R. Cavin, and D. Edwards, "A hybrid current/voltage mode on-chip signaling scheme with adaptive bandwidth capability," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 12, no. 8, pp. 876–879, Aug. 2004.
[5] D. Schinkel *et al.*, "A 3 Gb/s/ch transceiver for *RC*-limited on-chip interconnects," in *Proc. ISSCC*, Feb. 2005, pp. 386–387.
[6] E. Seevinck, P. v. Beers, and H. Ontrop, "Current-mode techniques for high-speed VLSI circuits with application to current sense amplifier for CMOS SRAM's," *IEEE J. Solid-State Circuits*, vol. 26, no. 4, pp. 525–536, Apr. 1991.
[7] R. Ho, K. Mai, and M. Horowitz, "Efficient on-chip global interconnects," in *Proc. Symp. VLSI Circuits*, 2003, pp. 271–274.
[8] W. Dally and J. Poulton, *Digital Systems Engineering*. Cambridge, U.K.: Cambridge Univ. Press, 1997.
[9] T. Sakurai, "Closed-form expressions for interconnection delay, coupling, and crosstalk in VLSI's," *IEEE Trans. Electron Devices*, vol. 40, no. 1, pp. 118–124, Jan. 1993.
[10] X. Liu, Y. Peng, and M. C. Papaefthymiou, "Practical repeater insertion for low power: What repeater library do we need?," in *Proc. DAC*, 2004, pp. 30–35.
[11] K. Banerjee and A. Mehrotra, "A power-optimal repeater insertion methodology for global interconnects in nanometer designs," *IEEE Trans. Electron Devices*, vol. 49, no. 11, pp. 2001–2007, Nov. 2002.
[12] H. Zhang, V. George, and M. Rabaey, "Low-swing on-chip signaling techniques: Effectiveness and robustness," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 8, no. 3, pp. 264–272, Jun. 2000.
[13] A. P. Chandrakasan and R. W. Brodersen, *Low Power Digital CMOS Design*. Norwell, MA: Kluwer, 1995.
[14] A. Deutsch *et al.*, "On-chip wiring design challenges for gigahertz operation," *Proc. IEEE*, vol. 89, no. 4, pp. 529–555, Apr. 2001.
[15] Y. Ismail, E. Friedman, and J. Neves, "Figures of merit to characterize the importance of on-chip inductance," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 7, no. 12, pp. 442–449, Dec. 1999.
[16] R. Chang, N. Talwalkar, C. Yue, and S. Wong, "Near speed-of-ling signaling over on-chip electrical interconnects," *IEEE J. Solid-State Circuits*, vol. 38, no. 5, pp. 834–838, May 2003.
[17] D. Burger and T. M. Austin, "The simplescalar tool set, version 2.0," Univ. Wisconsin, Madison, Tech. Rep. CS-TR-97–1342, 1997.

Joint AGC-Equalization Algorithm and VLSI Architecture for Wirelined Transceiver Designs

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***Abstract*—Traditional approaches of *automatic gain control* (AGC) involve estimating the average power or the peak amplitude over an extended time period, which results in high hardware complexity and a long processing time. Moreover, the accuracy of traditional approaches is seriously degraded by noise and *intersymbol interference*. In this paper, we propose a *joint AGC and equalization* (Joint AGC-EQ) scheme, in which the AGC circuitry comprises only one-tenth of the area of a traditional AGC. In addition, the total convergence time of the proposed Joint AGC-EQ is only half that of traditional *blind equalization*. The scheme is already silicon proven for the application of a *Fast Ethernet* transceiver using *Faraday/UMC* 0.18-μm cell libraries.**

***Index Terms*—Automatic gain control (AGC), blind equalization, equalizer.**

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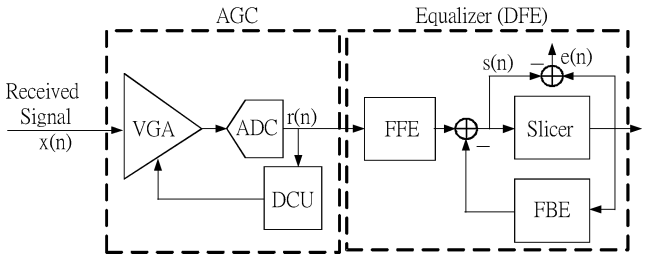

Fig. 1. Block diagram of a traditional equalizer and AGC.

I. Introduction

Automatic gain control (AGC) and *equalizer* circuitry are the key building blocks of modern communication and data storage systems. The generalized AGC and widely used *decision feedback equalizer* (DFE) are shown in Fig. 1. The AGC circuitry can increase the power of the input signal as well as avoid saturation of the *analog-to-digital converter* (ADC). In contrast to pure analog gain control, modern AGC circuits [1]–[4] are separated into two parts: 1) the *variable-gain amplifier* (VGA) in the analog front end and 2) the *digital control unit* (DCU) in the digital circuitry. Traditional DCUs collect data over an extended period, estimate the average power or the peak amplitude, and adjust the gain of the VGA, which results in high hardware complexity and a long processing time.

On the other hand, the equalizer in Fig. 1 comprises the *feedforward equalizer* (FFE), the *feedback equalizer* (FBE), and the *slicer*. The FFE and FBE can eliminate the *pre-* and *postcursor intersymbol interference* (ISI), respectively. The slicer is the decision device. In addition, for *blind equalization* [5]–[8], the equalizer requires an extra period to normalize the initial weights before the normal equalization procedure, in case of ill-convergence [5] of the tap weights. This extra period will extend the total convergence time and increases the hardware complexity. Unfortunately, the convergence periods take a very long time when no *procedure parallelism* is exploited, which is not desirable in modern low-cost high-speed receiver IC designs.

To overcome the previous disadvantages, we propose a *joint AGC and equalization* (Joint AGC-EQ) algorithm in this paper. The key idea of our scheme is to use the equalizer as the power meter of the AGC and connect both components together to implement the *convergence procedure* and *hardware circuits*. Therefore, the Joint AGC-EQ scheme is not only a low-cost AGC scheme, but is also a blind equalization scheme. By doing so, we can skip the procedure of the equalizer weight normalization. That is, the proposed Joint AGC-EQ scheme provides the following advantages.

1) **Cost efficiency:** The digital gate count of the AGC circuitry is less than one-tenth that of the traditional approach, and there is no extra loading in the equalizer.
2) **Fast convergence:** The blind equalization and AGC evaluation periods can be overlapped, so that the overall Joint AGC-EQ convergence period being only half that of the traditional approach.

The Joint AGC-EQ algorithm has been implemented in silicon and embedded in commercial intellectual property for the application of a *fast ethernet transceiver* based on *Faraday/UMC* 0.18-μm process libraries. The intellectual property also passes the University of New Hampshire InterOperability Laboratory worst case cable testing and the stringent *killer pattern* testing. The rest of this paper is organized as follows. In Section II, we review the problems of conventional AGC. In Section III, we derive the proposed Joint AGC-EQ algorithm. A convergence analysis is explained in Section IV. The hardware implementation and experimental results are presented in Section V. Finally, we conclude our work in Section VI.