Fully Integrated AC Coupled Interconnect Using Buried Bumps

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***Abstract*—Presented is the complete demonstration of an assembled system using AC coupled interconnect (ACCI) and buried solder bumps. In this system, noncontacting input/output (I/O) are created by using half-capacitor plates on both a chip and a substrate, while buried solder bumps are used to provide power/ground distribution and physical alignment of the coupling plates. ACCI using buried bumps is a technology that provides a manufacturable solution for noncontacting I/O signaling by integrating high-density, low inductance power/ground distribution with high-density, high-speed I/O. The demonstration system shows two channels operating simultaneously at 2.5 Gb/s/channel with a bit error rate less than 10^{-12}, across 5.6 cm of transmission line on a multichip module (MCM). Simple transceiver circuits were designed and fabricated in a 0.35-μm complementary metal–oxide–semiconductor (CMOS) technology, and for PRBS-127 data at 2.5 Gb/s transmit and receive circuits consumed 10.3 mW and 15.0 mW, respectively. This work illustrates the increasing importance of chip and package co-design for high-performance systems.**

***Index Terms*—AC coupled interconnect (ACCI), buried bumps, capacitive coupling, MCM, pulse signaling, noncontacting I/O, chip and package co-design.**

I. Introducton

NUMEROUS types of noncontacting, interchip signaling methods have been presented, such as ACCI [1], [2], proximity communication [3], and wireless superconnect (WSC) [4]. ACCI using buried solder bumps is a technology that provides a *complete solution* by integrating high-density, low inductance power/ground distribution with high-density, high-speed input/output (I/O). The mixture of buried solder bump technology and AC coupled I/O has the potential to improve yield during packaging and assembly since I/O channels are no longer dependent on the yield of a solder bump. For the same reason, this technology has the potential to increase the long-term reliability of chip/carrier components of electronic systems used in harsh environments. The buried solder bump technology can also be combined with a high-k dielectric underfill to reduce the required area for coupling capacitors and/or relax the requirement on interplate separation, while also providing stress relief between the chip and substrate [5]. The key concept with ACCI is that DC connections are not needed to convey the information contained in high-speed digital signals. Instead the information in these signals can be coupled via "AC connections," such as a series capacitor.

When using buried solder bumps with ACCI, the buried solder bumps have two purposes. First, the buried bumps provide DC connections (e.g., for power and ground) across the interface. Second, the buried bumps provide a means to self-align the chip and package surfaces while maintaining a close and controlled proximity between corresponding capacitor plates. This creates AC and DC paths simultaneously across the same interface between chip and package. An important advantage of AC connections is that circuit design considerations can be made the limiting factor to achieving high I/O density rather than physical limitations such as the manufacturability of dense arrays of sub-100-μm solder bumps. Since process and circuit design techniques develop more quickly than package and interconnect technologies, due to physical and economic constraints, it is important to consider chip and package co-design solutions that can reduce the overall cost for a particular level of performance. A primary goal of this research is to reduce the limits on performance imposed by the physical constraints of packaging technologies and push the silicon and circuit designers into the critical path. In doing this, advances in packaging and off-chip I/O will be able to increase more rapidly with silicon and circuit performance.

The work presented in this paper on ACCI distinguishes itself from the recent work in this area that focuses on three-dimensional integrated circuits (3-D-ICs) [3], [4], [6] by demonstrating communication over significantly longer and more lossy interconnects at higher data rates than reported for noncontacting 3D-IC efforts. The remaining sections of this paper will examine the major challenges associated with using ACCI to communicate data across long interconnects. Section II provides a brief background on the ACCI system. In Section III, an overview of the substrate stack-up is given and an assembled substrate and chip using buried bump technology is presented. Section IV provides a discussion of pulse signaling and the passive equalization provided by ACCI, and addresses the tradeoffs with capacitor variation and transmission line length. The transceiver circuits used in this demonstration and the measured results are presented in Section V, and Section VI

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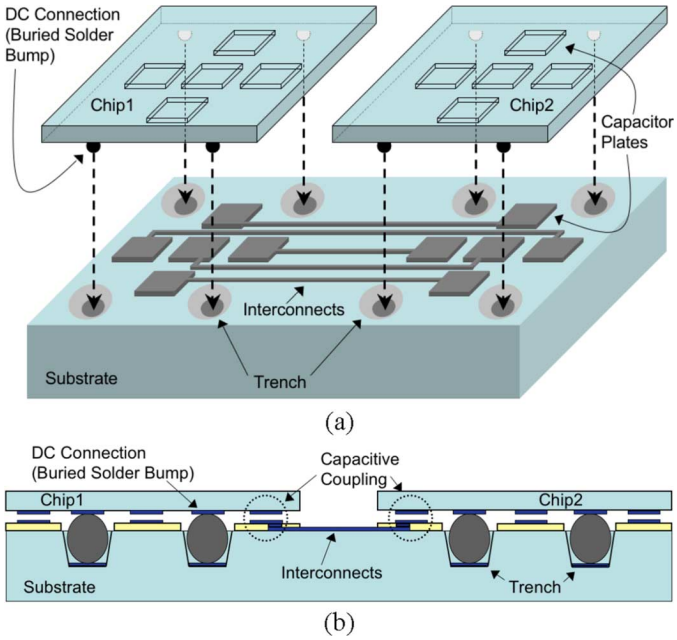

Fig. 1. ACCI Physical Structure: (a) "3-D" view; (b) cross-sectional view.

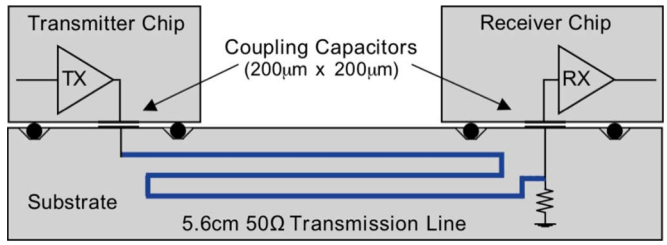

Fig. 2. ACCI demonstration system.

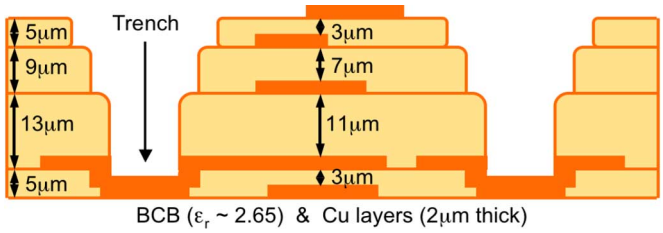

Fig. 3. Five metal layer substrate stack-up with trenches for buried bumps.

discusses issues relating to transmission line design in ACCI systems. Sections VII and VIII are a discussion highlighting the advantages of ACCI and the conclusions of this work.

II. ACCI Physical System

The major challenges when communicating across long interconnects in ACCI come from the inherently lower signal-swing due to the low impedance of a terminated transmission line, the frequency dependent losses of a transmission line, and signaling through two small series capacitors. It has been demonstrated that ACCI can work at 3 Gb/s across long interconnects by using circuit design techniques and the intrinsic passive filtering of the series capacitors to compensate for the frequency dependent losses of a microstrip line on a FR4 PCB [2], while saving power when compared to systems using active equalization.

An illustration of the physical ACCI system with two chips mounted on a common substrate using buried solder bumps is shown in Fig. 1. The buried solder bumps provide power and ground to the mounted chips, and are also used to self-align the AC coupling elements and control the resulting gap between the chip and substrate. The substrate uses five copper metal layers for power, ground, signal routing, and coupling element formation. Benzocyclobutene (BCB) was chosen for the dielectric layers because of its low permittivity ($\varepsilon_{\rm r} \sim 2.65$), low-loss tangent ($\tan\delta \sim 0.002$ from 1 to 10 GHz), and excellent planarizing properties [7].

Fig. 2 shows the ACCI equivalent circuit for the demonstration system. It includes the transmitter and receiver chip, and the substrate with a 5.6-cm-long 50-Ω microstrip line. The capacitive coupling element is formed between the top metal layer on the substrate and the top metal layer on the complementary metal–oxide–semiconductor (CMOS) chip. The conformal, 1.7-μm-thick glass from fabrication is left as-is covering the portion of the capacitive element on the CMOS chip. The corresponding portion of the capacitive element on the substrate is not covered by a dielectric. In this work, the capacitor plate size is 200 $\times$ 200 μm (i.e., a 270 fF coupling capacitance for a 1-μm air gap between capacitor plates), and this element could be used for I/O pitches just above 200 μm, because of the comparatively low lateral coupling. Simulations show that scaling to a 0.18-μm circuit technology allows the coupling capacitor to be reduced to less than 80 m $\times$ 80 μm, with signaling rates in excess of 5 Gb/s/channel.

III. Substrate With Buried Bumps

To demonstrate ACCI with buried bumps, a multimetal layer substrate was design and fabricated at RTI International (formerly MCNC-RDI). The substrate was manufactured using a silicon wafer with five copper interconnect layers, each 2 μm thick, and four BCB dielectric layers, of varying thickness. An illustration, of the substrate stack-up showing the thickness of each dielectric layer is shown in Fig. 3. The lower two metal layers (M1 and M2) were used for power and ground distribution, as references planes, and to form the contacting layers for the buried bumps. The large overlapping areas of M1 and M2, separated by a relatively thin BCB layer (3–5 μm), also provide integrated decoupling that helps to decrease the impedance of the power supply. (If the intermetal dielectric was created using a very thin silicon nitride layer, 100 nm and $\varepsilon_r \sim 7$, then the integrated decoupling capacitance could be increased by approximately 100$\times$.) The two metal layers, M3 and M4, embedded in dielectric were used for the routing of transmission lines and the top metal layer, M5, was mainly used to form the AC I/O structures. In some situations, the top metal layer was also used to create low-loss microstrip lines for long runs across the substrate, and also as a reference plane to form striplines using M3. That is, when chips are flipped onto the surface of the substrate, thereby realizing a complete ACCI system, the close proximity between chip and substrate changes the impedance of embedded microstrip lines passing beneath. If large chips are attached to the substrate where long transmission lines are routed,

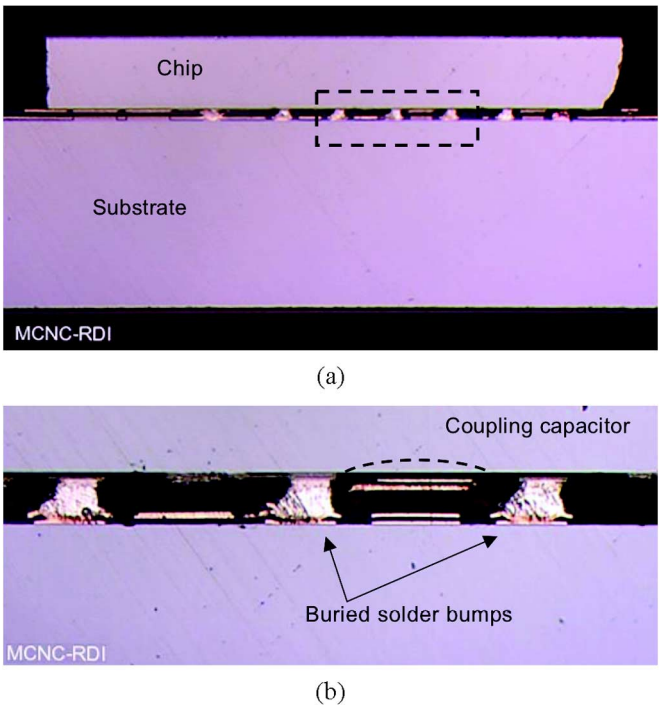

Fig. 4. Cross-sectional views: (a) substrate and chip; (b) buried bumps and coupling capacitor.

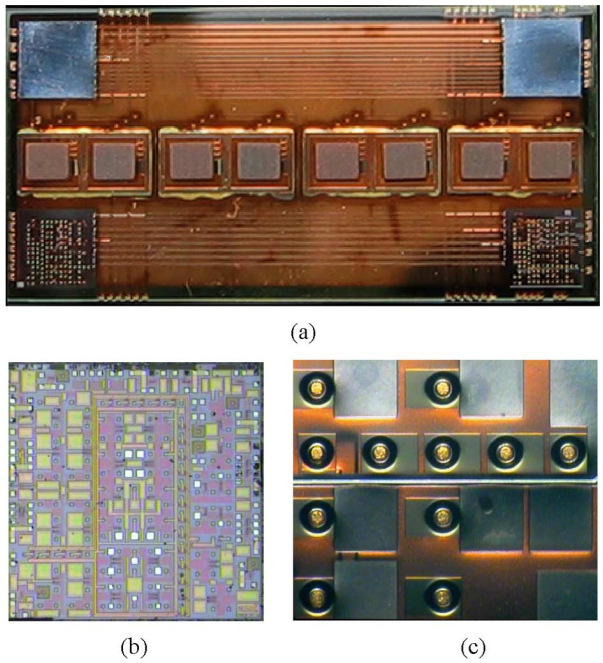

Fig. 5. ACCI system: (a) assembled MCM; (b) chip; (c) trenches and AC I/O.

it is necessary to form striplines beneath the chip to maintain predictable and controlled impedance. This will be discussed further in Section VI.

Fig. 4 shows the cross section of an assembled substrate and CMOS chip. Coupling capacitors formed by the substrate and chip interface can be seen between the buried bumps. In the images of Fig. 4, it can be seen that there is slight misalignment in the coupling elements ($\sim 5\mu$m). Misalignment in this case is due to the fact that the chips and substrates were deliberately brought into contact, and friction at the interface prevented the solder bumps from self-aligning. This intimate contact resulted in a separation between the chip and substrate capacitor plates of less than 1 μm and was chosen so that the performance at minimum separation could be established. By controlling the solder ball volume and re-flow parameters, any specific gap distance can be achieved. The capacitor shown in Fig. 4 is smaller than that used in this demonstration.

The ACCI system can be scaled to interconnect multiple ICs. Shown in Fig. 5 is a photograph of an assembled substrate populated with two CMOS ICs and eight decoupling capacitors. The substrate has two chips mounted, but can accommodate up to four chips and includes eight sites for BGA decoupling capacitors. Fig. 5 also shows a chip photo of the TSMC 0.35-μm CMOS chip used in this demonstration and a zoomed in view of a mounting site for the IC on the substrate. The zoomed in view shows solder bump trenches that are approximately 30-μm deep, and the plates corresponding to the capacitive AC coupling elements on the surface of the substrate. The substrate is 25 $\times$ 12.5 mm and each CMOS chip is 3.2 $\times$ 3.2 mm.

IV. Channel Response, Pulse Signaling And Equalization

In ACCI channels, the combination of series coupling capacitors, shunting parasitic capacitors, and transmission line create a channel with a bandpass response. The transmission line and parasitic capacitors define the low-pass response, while the coupling capacitors define the high-pass response. To reduce reflections, one or both sides of the transmission line should be terminated. Terminating at one side of the transmission line, instead of both sides, produces an increase in the received signal at the expense of reflections on the line.

The main difference in signaling through an ACCI channel verses a traditional channel is the use of bipolar pulse mode signaling. The first coupling capacitor in the ACCI channel converts the edges of a binary non-return to zero (NRZ) signal into a bipolar pulse signal, which is very similar to a ternary NRZ signal. This conversion comes from the differentiation that occurs due to the high-pass characteristic of the series capacitive coupling. When using ternary NRZ signaling, the intermediate state denotes a continuation of the previous full swing logic state [8]. The key distinction between the true definition of ternary NRZ signaling and the form of bipolar pulse mode signaling used in ACCI, is in the fact that the pulse duration does not have to equal the entire bit period, but can be less than or equal to the bit period. When the pulse duration is greater than the bit period the result is intersymbol-interference (ISI). (Intersymbol-interference occurs when the signal energy in neighboring bits overlaps, thereby, making the accurate distinction of data more difficult.) A comparison of NRZ, ternary NRZ, and bipolar pulse mode signaling (ACCI) waveforms are shown in Fig. 6. In this example, the duration of the bipolar pulse signal is less than the bit period.

In more detail, first consider that the full swing transmitter produces a step input to the ACCI channel. The first series cou-

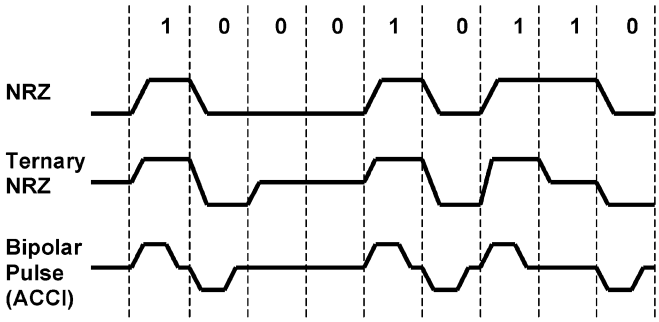

Fig. 6. Comparison of NRZ, Ternary NRZ, and bipolar pulse mode signaling (ACCI) [Note: bipolar pulse duration is less than bit period in this example].

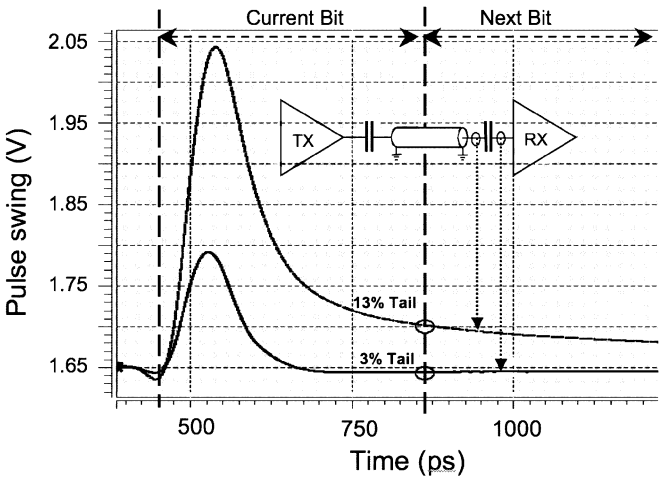

Fig. 7. Coupling capacitors provide passive high-frequency compensation—helping to reduce ISI.

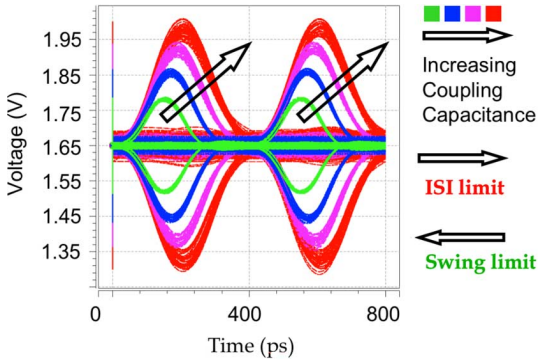

Fig. 8. Pulse eye diagram for increasing coupling capacitance.

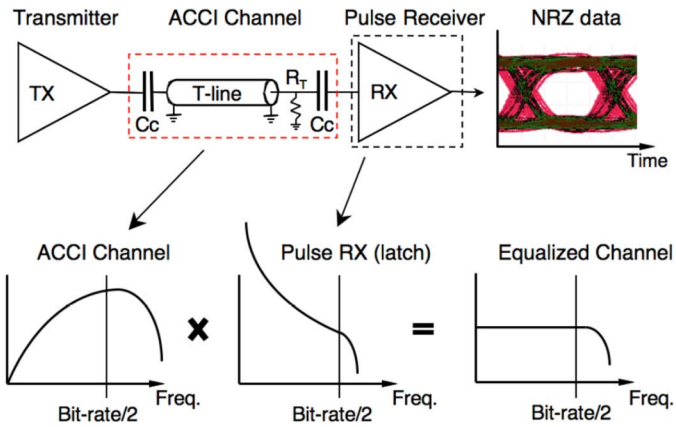

Fig. 9. Frequency domain equalization scheme for pulse signaling in ACCI.

pling capacitor differentiates this edge and produces a pulse that propagates on the transmission line. The transmission line has a low-pass response due to the skin effect and dielectric loss, causing dispersion, which "smears" the signal into neighboring bit periods. Without compensation this dispersion will cause ISI, reducing the voltage and timing margin at the receiver. The second coupling capacitor de-emphasizes the low frequency components by filtering the long pulse tail, thereby, reducing energy that interferes with adjacent pulses. This allows ACCI to save chip area and reduce power dissipation typically associated with active high frequency equalization. An illustration of how this passive filtering is used to compensate for ISI is shown in Fig. 7.

The pulse amplitude and width at the receiver are determined by the coupling capacitors, transmission line characteristics, and the edge rate and amplitude of the transmitted step. For a given data rate and pulse receiver input sensitivity, there is a range of coupling capacitor sizes and transmission line lengths, within which a pulse receiver is able to recover the data. These limits along with the required interconnect length and AC I/O density, determine the design space for a given chip and interconnect technology. Fig. 8 shows the differential pulse eye diagram after the second coupling capacitor (i.e., at the receiver input). The arrows show the trend resulting from increasing the coupling capacitor size. Larger coupling capacitors will increase the amplitude and duration of the pulse. The increased amplitude relaxes the constraint on the receiver input sensitivity, but increasing the pulse width too much will eventually introduce ISI and limit the maximum signaling rate. However, a smaller coupling capacitor is more efficient at filtering the pulse signal tail and mitigating ISI, but the corresponding reduction in signal amplitude increases the input sensitivity requirement for the receiver. Therefore, the maximum coupling capacitance is constrained by the ISI limit, or the data period limit, while the minimum coupling capacitance is constrained by the swing limit, or receiver input sensitivity and noise levels in the intended system. In summary, a small series capacitor to create pulse mode signaling can be used to compensate for the frequency dependent losses of a channel and is equivalent to "over-equalization" [9].

As discussed, the overall band-pass characteristic of ACCI channels uses a different equalization scheme than traditional transmission line channels. High-frequency compensation used in traditional transmission line channels is not required in ACCI. However, low-frequency compensation is necessary. The critical components of the system and their corresponding frequency responses are shown in Fig. 9. The receiver is essentially a latch or edge detector and is used to compensate for all low-frequency attenuation. It effectively flattens the frequency response of the channel. The latch detects and captures pulses, and remains stable until detecting the next opposite polarity pulse in the NRZ data stream; thereby, implementing an adaptive low frequency compensator. As long as the pulse data rate is less than the latch bandwidth, the low-frequency

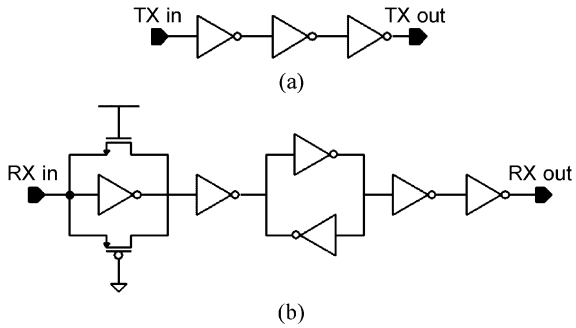

Fig. 10. Circuits for ACCI system demonstration: (a) transmitter and (b) receiver.

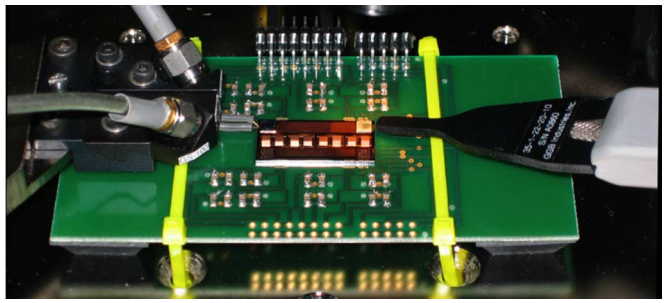

Fig. 11. ACCI MCM-D System under test.

compensation dynamically adapts to changes in pulse width caused by the transmission line and coupling capacitor variations. Furthermore, as long as the NRZ signal edge rate has enough energy in the passband of the ACCI channel, any digital signal can pass the ACCI channel and be recovered by the pulse receiver. Theoretically, this corresponds to a digital signal with a data rate approaching DC. This explains how the latch-based pulse receiver can recover long consecutive "1" or "0s". The transmission line also affects the channel response and pulse shape. Longer transmission lines result in more attenuation, especially high-frequency attenuation. This not only extends pulse width (increasing ISI) but also limits pulse amplitude. Thus, the maximum transmission line length is constrained by both the ISI limit and receiver signal amplitude requirements. (From the simulation results shown in Fig. 8, it can be seen that the limiting factor in this demonstration was the 0.35-μm CMOS technology. Simulations show a 0.18-μm CMOS technology will enable signaling rates in excess of 5 Gb/s for the same channel.)

V. Transceiver Circuits And Measured Results

Elaborate circuits are not needed to demonstrate ACCI technology. Instead, as shown in Fig. 10, an inverter chain can be used for data transmission, and a self-biased inverter with an asynchronous latching circuit can be used as a receiver. The transmitter and receiver circuits used in this work do not require any clocking to transmit or receive the incoming data stream. Very similar receiver circuits have been demonstrated for single-ended capacitive coupled signaling [6], and a variety of receivers have been demonstrated for differential signaling [2], [10], [12].

By using an inverter chain to create the transmitter, the DC power consumption associated with biased transmitter circuits is eliminated. In addition, the small series coupling capacitor presents a high-impedance to the output stage helping to isolate it from the low impedance transmission line; thereby, decreasing the transmit power even further. The transmitter only needs to be sized appropriately for the target range of coupling capacitor sizes and transmission line lengths. Increasing the strength of the transmitter beyond the "worst case" combination for the channel will only result in increased power consumption and power supply noise. Currently, research is being conducted on differential ACCI channels that use complementary output stages to maintain this advantage, while reducing simultaneous switching noise. Though differential ACCI systems have already been demonstrated, scaling them to have a large number of I/O will require careful evaluation of techniques to reduce simultaneous switching noise. The technique presented in [11] skews the transition time for each transmitter into one of eight timing slots, per period, to effectively average the aggregate switching current.

The self-biased receiver circuit was adapted from a previous design [6]. The only modification to this receiver was in the biasing of the input stage. The earlier design used diode-connected transistors, but the receiver used in this work implemented resistive feedback by using a transmission gate. A buffer that helps to amplify the received pulse follows the self-biased input stage. This buffer also provides the needed isolation between the input stage and the latching structure that follows. This asynchronous latch has a data dependent bias point at the input and output (either high or low), and must be isolated from the bias point of the input stage to function properly. Since the receiver uses an asynchronous latch, its delay is not dependent on the clock used to sample incoming data. The delay from the input of the receiver to the output of the latch is 365 ps (less than one bit period at 2.5 Gb/s) from the receiver input to the output of the latch, for typical process, voltage, and temperature. The output of the latch uses two buffering stages to drive the pad and high-impedance probes used for measurement.

For testing, two CMOS chips were bumped and flip-chip attached to a substrate and then mounted to a PCB, as shown in Fig. 11. Although both CMOS ICs are identical, only the transmitter circuits were used on one IC to drive data across the channel, and only the receiver circuits on the other IC were used to recover data from the channel. Input data was provided via an Agilent 81134 PRBS source and output data was measured using a Tektronix 11801B Digital Sampling Oscilloscope with a GGB Model 35 high-impedance active probe. Two transmitters on the transmit chip were driven by separate channels from the PRBS source at 2.5 Gb/s/channel for a total throughput of 5 Gb/s across two 5.6-cm 50-Ω micro-strip lines on the substrate (meandered). For a single channel operating at 2.5 Gb/s, the transmitter consumed 10.3 mW and the receiver consumed 15.0 mW, for a total power of 25.3 mW. Table I summarizes system specifications and performance.

Fig. 12 shows the measured output of the receive chip for both a 32-bit arbitrary data pattern and PRBS-127 data $(2^7 - 1)$ on channel-1, while channel-2 transmits and receives PRBS-127 data. Each channel operates without error in the presence of

TABLE I
PERFORMANCE SUMMARY

Supply Voltage	3.3V
Technology	0.35μm CMOS & MCM-D
Data Rate	2.5Gb/s/channel
Interconnect Length	5.6cm
Power Dissipation (TX)	10.3mW
Power Dissipation (RX)	15.0mW
Bit Error Rate (BER)	Better than 10^{-12}

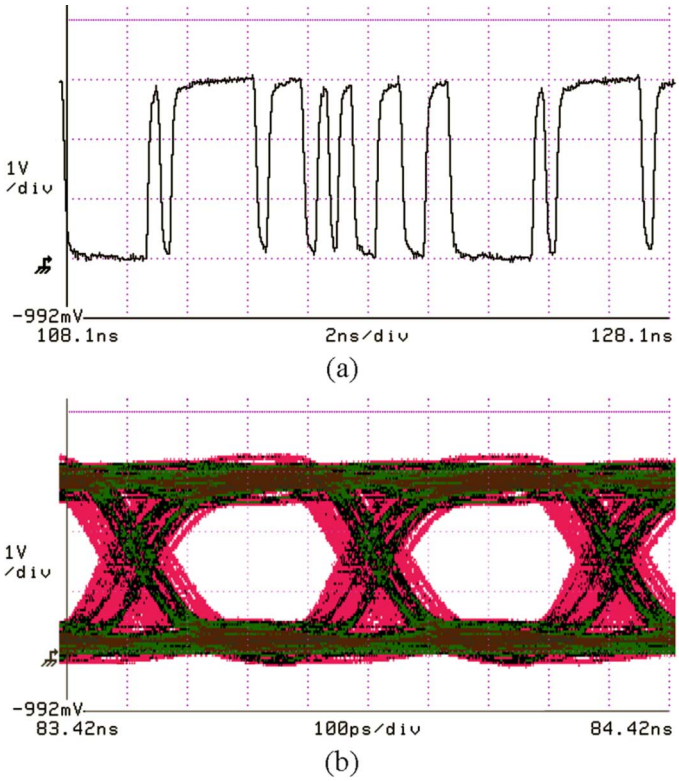

Fig. 12. Measured output for two channels operating at 2.5 Gb/s/channel: (a) 32 bit arbitrary pattern; (b) PRBS-127 eye diagram.

power supply noise from the adjacent channel. Bit error rate (BER) measurements of the system performed using an Agilent 86130A BERT, at 2.5 Gb/s/channel, were better than 10^{-12} for PRBS-127 data, and were only stopped due to time constraints. Also, the peak-to-peak jitter on the PRBS-127 data of channel-1 is less than 120 ps, most of which is due to the use of the asynchronous receiver circuit.

VI. Transmission Line Design Issues With ACCI Using Buried Bumps

In a typical flip-chip assembled system, the distance between the substrate and the flip-chip is generally large when compared to the dimensions of the dielectrics and the signal lines routed on the substrate. This large separation means that the chip mounted above the substrate does not significantly affect the characteristic impedance of the lines on the substrate. However, as the chip comes into close proximity with the surface of

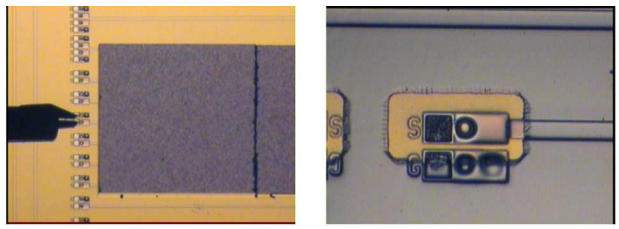

Fig. 13. (a) Chip placed on substrate. (b) Added reference plane.

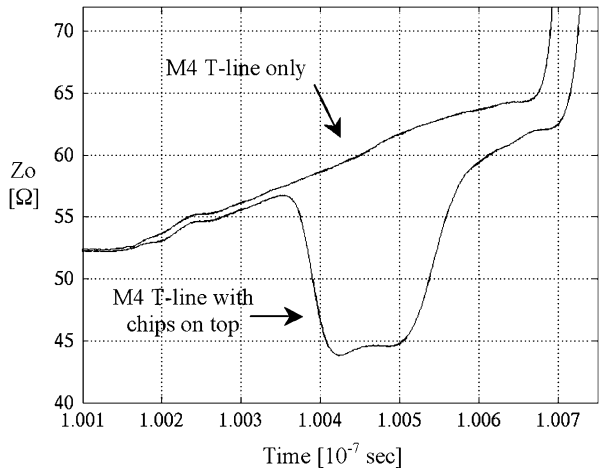

Fig. 14. TDR measurement of T-line: with and without chips.

the substrate, the presence of conductive materials and high permittivity dielectrics, begin to influence the electrical behavior of transmission lines routed on the substrate beneath the chip. This influence needs to be considered and a method for controlling the characteristic impedance of lines routed beneath a chip on the substrate needs to be established. During the evaluation of the initial process run, it was determined that the top metal layer would be needed to be used as a reference plane to form striplines using M3 for transmission lines routed beneath a large chip.

To evaluate the impact of a chip in such close proximity to the substrate, multiple samples were placed face down on the substrate and the characteristic impedance of transmission lines in M4 were measured using a Tektronix 11801B Digital Sampling Oscilloscope in TDR mode. These samples and the substrate were cleaned and examined before assembly to insure that no debris was present at the interface. Shown in Fig. 13(a) are multiple chips placed face down above a transmission line under test. The influence of the chips was measured and shown to be significant, and indicates that striplines should be used when lines pass beneath a large chip and given the dimensions of the layer stack-up (see Fig. 3) forces the use M3 lines on the substrate. M4 lines cannot be used because of the very thin dielectric layer between M4 and M5. To evaluate the conversion of embedded micro-strip lines to striplines, lines on silicon wafer were measured and then re-measured after the deposition of a reference plane (0.8 μm Ti/Cu). Fig. 13(b) shows a GS probe

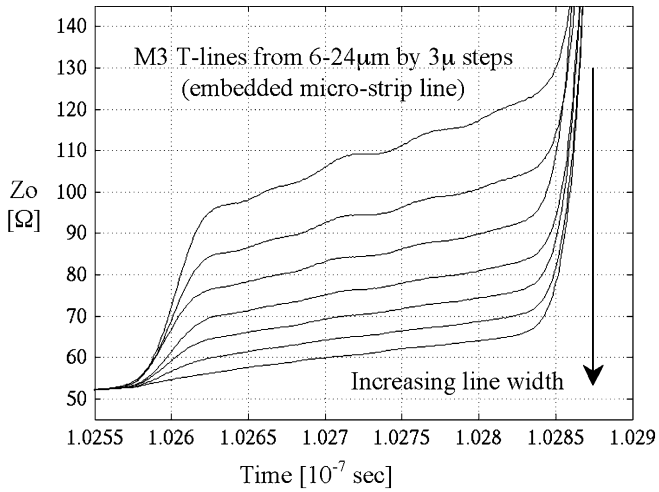

Fig. 15. TDR measurement of embedded micro-strip lines.

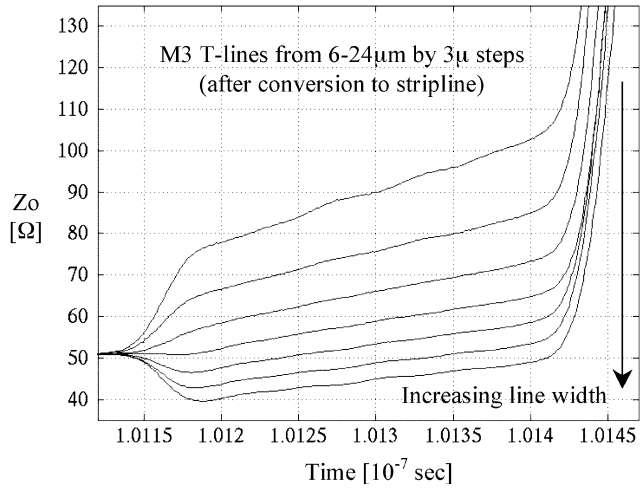

Fig. 16. TDR measurement of striplines *(addition of Ti/Cu)*.

pad with the added metal that was opened for the signal probe tip, after the addition of the reference plane.

Shown in Fig. 14 is a comparison of TDR measurements for a 46-μm-wide and 50-mm-long line in M4, with and without chips placed on top of the substrate. Five chips (each 2×2 mm) were placed near the center of the line to emulate the presence of a large bump attached chip in close proximity to the substrate. The change in the characteristic impedance shows that the chips have a significant impact on the impedance of the underlying transmission lines.

The addition of the reference plane on the top surface of the wafer enables the routing of transmission lines beneath a chip, and adds the benefit of reducing the required line width to achieve the desired system impedance of 50 Ω. A comparison of the line impedance for 25-mm-long M3 lines (varied from 6 to 24 μm in 3-μm steps) is shown in Figs. 15 and 16. The waveforms in Fig. 15 show that the impedance of the embedded microstrip lines varies from 50 to 95 Ω. After the conversion to stripline the range of impedance values vary from 40 to 75 Ω, as shown in Fig. 16. The conversion to stripline reduces the required line width by 50%, from 24 to 12 μm, and enables denser routing without the need for additional layers in the substrate. If transmission lines were routed in M4 or M5, then simultaneous routing over M3 would not have been possible due to the extremely high coupling that would have occurred without a reference plane above the top routing layer. This shows that the best topology for transmission line routing in MCMs using ACCI is a stripline structure when the transmission line is routed beneath die. For the example reported in this work, the required line width was reduced by 50%, saving significant routing area. Once routed lines escape the edges of the die, these lines can be converted to microstrip to reduce losses, as the available periphery permits.

For a multichip module-deposited (MCM-D) process, lines widths of 12 μm can be manufactured with high yield; however, if the substrate was manufactured using a lamination process (MCM-L) then line widths would be limited to approximately 25 μm, for currently available packages. Using a MCM-L, as an interposer between an ACCI chip and PCB, would enable this technology to interface and communicate across cards or in backplane applications. The capacitive interface would be created between the chip and the MCM-L, and a different arrangement for the solder bumps is preferred given the coefficient of thermal expansion (CTE) mismatch between the chip and MCM-L [13].

VII. Discussion

Numerous advantages are the result of combing ACCI with a chip and package co-design approach. By reducing the limitations imposed by packaging and interconnect, ACCI allows overall improvements to increase more rapidly by providing a technology that places silicon and circuit issues in the critical path. In addition, the use of ACCI enables reductions in power consumption by implementing simple circuits and passive equalization. Both of these advantages are inherent, positive outcomes of using a small series capacitor to create an AC coupled interface. (The same power savings can be achieved by integrating the series coupling capacitor and termination resistor on-chip, assuming that power reduction is the primary goal. This eliminates the need for surface mounted discrete components, such as DC blocking capacitors, and eliminates the signal integrity issues associated with signaling through a relatively large surface mount component at high frequencies.) ACCI using buried bumps also has the potential to improve yield during packaging and assembly since I/O channels are no longer dependent on the yield of a single solder bump. Also, the close proximity of the chip and substrate requires the use a stripline structure when routing beneath the chip. This constraint has the advantage of creating controlled impedance lines in a high breakout situation.

Recent results have demonstrated a differential ACCI link, fabricated in the TSMC 0.18-μm CMOS, capable of signaling at 36 Gb/s (6 channels simultaneously at 6 Gb/s/channel) across FR-4 micro-strip PCB traces with lengths of up to 30 cm, for series coupling capacitor variations from 95 fF to 165 fF [12]. This demonstration used wire bonds, to connect from on-chip metal–oxide–metal (MOM) capacitors to traces on a PCB, which degrade the performance when compared to using ACCI with buried solder bumps to create off-chip interconnect. The use of wire bonded I/O allowed for simple assembly and testing

of experiments to verify circuit functionality and to quantify issues such as coupling capacitor variation, without requiring flip-chip assembly.

VIII. Conclusion

Though similar "capacitive coupled interconnect" schemes have been presented, they lack a solution for providing high-density, robust power and ground distribution that is also compatible with current manufacturing methods. ACCI is a technology that has demonstrated a *complete solution* by combining buried solder bumps to provide high-density, low inductance power and ground distribution with high-speed AC I/O using capacitive coupling. In addition, ACCI using buried solder bumps can use existing methods of manufacturing without significant changes being needed. Measurements and simulation results show that the limiting factor for this demonstration was the 0.35-μm CMOS technology, not the AC coupled interconnect.

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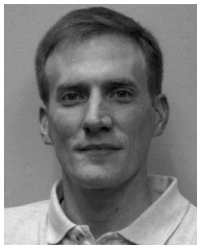

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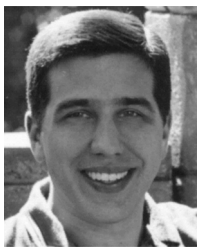

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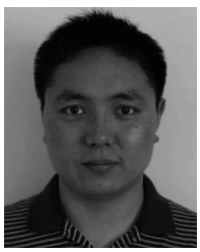

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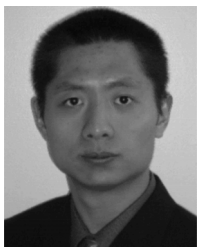

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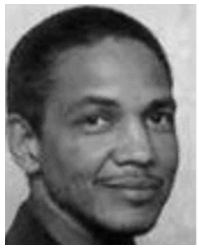

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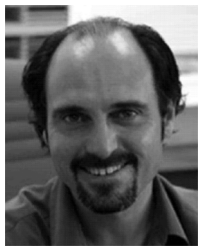

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