System level Validation of Improved IO Buffer Behavioral Modeling Methodology Based on IBIS

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Abstract:

System level simulation and validation of a new macromodeling methodology based on IBIS (Input/Output Buffer Information Specification) models is presented. Enhancements of the black-box techniques discussed in [1] are discussed. The proposed macromodel is circuit based and can be customized by model makers or users. The new macromodel produces models that can be simulated accurately for Simultaneous Switching Noise (SSN). To demonstrate the solution, a CMOS voltage-mode driver circuit and a MICRON DDR2 driver are simulated using real life package models and compared with equivalent circuits created with IBIS models of the same drivers.

1. Introduction

A new macromodeling methodology based on IBIS was discussed in [1]. The new methodology improved power and ground noise simulations using IBIS models. This was achieved by complementing the IBIS model with a black-box that injected current in the supply rails of the power and ground network. This accounted for the **Pre-Driver and Crossbar Current** insufficiencies.

The second issue briefly mentioned in [1] was the **Gate Modulation Effect**. This paper discusses this effect in more detail. The paper also describes the process of building the black-box for a DDR2 SDRAM I/O voltage mode driver from MICRON Inc. [3] along with a Ball Grid Array (BGA) package obtained from Xilinx [4]. The black-box is created for both the corrections listed above. The paper also describes system level simulations and validation of the improved behavioral model using S-Parameter model of the BGA package. The IBIS model of the driver was constructed using the transistor model of the driver (encrypted) from Micron with the help of S2IBIS3 [2]. Equivalent system level simulations were done with transistor models of the driver to compare with the IBIS model results.

Section 2 describes the gate modulation effect and the enhancement made to the black-box to accommodate the effect. Section 3 develops the black-box one step at a time for both the phases of the black-box, the pre-driver current error correction (phase 1) and the gate modulation effect error correction (phase 2). Section 4 gives brief details of the system validation tests. Section 5 consists of the results of the system simulations. Section 6 concludes the paper.

All simulations in this paper are performed in HSPICE version 2004.03 on a SUN SPARC Sun Blade 100. IBIS models are simulated using the B-element in HSPICE.

2. Gate Modulation Effect

The power and ground bounce due to SSN affects the gate-source voltage of the pull-up and pull-down devices in an I/O driver (fig. 1). This gate voltage fluctuation should result in a variation of current flowing through the pull-up and pull-down devices - thereby affecting the current flow in the overall driver. IBIS models do not reflect this. Fig. 2 shows the characteristic (Ids Vs Vds) curves of an NMOS device for different Vgs values (figure shows 3 characteristic curves for Vgs1, Vgs2 and Vgs3 for demonstration purpose) as per Eq. 1 which is the spice level 1 MOS transistor model. This makes the transistor model current a function of both Vgs and Vds (Eq. 2). When the power and ground sources bounce, the Vgs values vary allowing the transistor models to adapt by making the device stronger or weaker (by shifting vertically on the characteristic curves). On the other hand, each VI table in the IBIS models (pull-up, pull-down, power-clamp and ground-clamp) represents only one of the characteristic curves shown in fig.2. As such a fluctuation in the power and ground source does not produce the same effect in an IBIS model (Eq. 3). This effect is also known as the *gate modulation effect.*

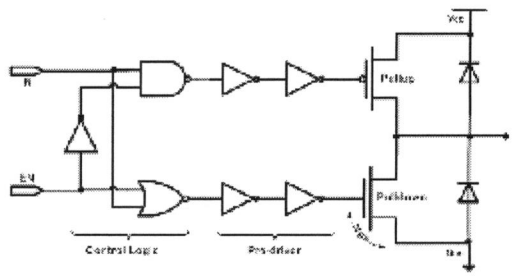


Figure 1: Tri-State Driver Schematic.

$$I_{ds} = \mu_n C_{ox} \frac{W}{L}[(V_{gs} - V_{th})Vds - \frac{1}{2}V_{ds}{}^2](1 + \lambda V_{ds}) \quad (1)$$

$$I_{ds}(trans) = f(V_{gs}, V_{ds}) \quad (2)$$

$$I_{ds}(IBIS) = f(V_{ds}) \quad (3)$$

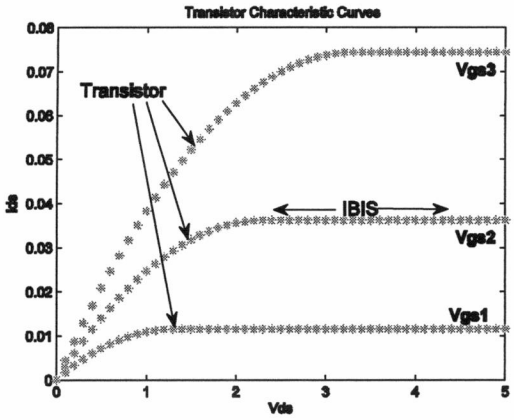


Figure 2: Ids Vs Vds Characteristic curves for NMOS transistors.

Gate Modulation Effect Error Correction

As in the case of the pre-driver error correction [1] where the current supply of the power pin was adjusted using the power and ground voltage, the gate modulation concerns the output current of the I/O driver. The difference current at the output is a function of the power and ground voltage as shown in (Eq. 5) and fig 3. This correction is improved by using a scaling coefficient K in (Eq. 6)

$$I_{diff,out} = I_{trans,out} - I_{ibis,out} = f(V_{ddIBIS} - V_{gndIBIS}) \quad (5)$$

$$I_{eff} = K \times I_{diff,out} \text{ where } K = N \times V_{inst}/V_{nom} \quad (6)$$

In most cases, Vnom is the normal value at which the I-V tables in the IBIS models are created. Vinst is the instantaneous (real time) voltage between the power and ground nodes of the I/O buffer. This voltage is not constant as the Vnom but reflects the noise due to switching in the local power and ground nodes. N (in (Eq. 6)) is a user dependent factor for adjusting the K factor and is usually the number of the drivers that are switching simultaneously in the system. SPICE implementation of the K factor is done in the following way:

```
Ek1 k1 0 vol = '(v(VDD1,GND1)-v(GND1))/vcc'
Ek2 k2 0 vol = '4*(v(k1)-1)'
```

where 'vcc' is the voltage at which the IBIS models were created (V_{nom}), 'VDD1' and 'GND1' are the local power and ground. The number of drivers used is 4 - hence N=4 (though this number is not always going to be the number of drivers as K is not linearly proportional to the number of drivers). The proposed error correction for the rising and falling edges individually for the "gate modulation effect" can be done by carrying out the following steps:

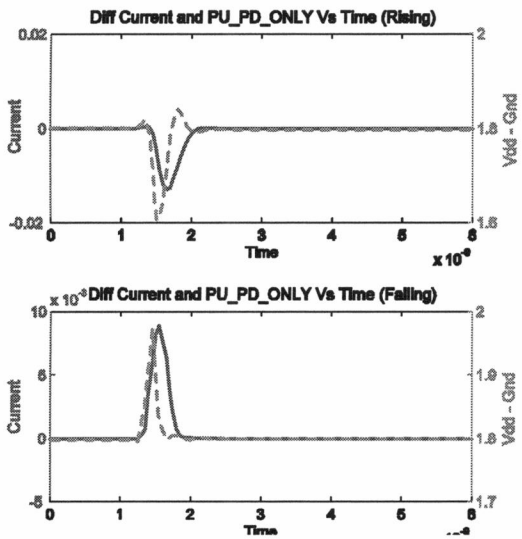


Figure 3: The difference current at the output between IBIS model drivers and transistor model drivers have a high degree of correlation with the voltage difference at the power andground pin in both the rising (top) and falling (bottom) transitions.

Step i): Setup circuit for rising and falling $I_{trans,out}$ and $I_{ibis,out}$: The correlation in Eq. 5 is captured in an nth order polynomial that can be used to recreate the difference in current. This is done using a circuit with IBIS model and another circuit with the transistor model as described in [1]. For gate modulation effect, the current at the output of the driver is collected.

Step ii): Obtaining the polynomial coefficients for VCCS implementation: Once IBIS and transistor circuit SPICE output is obtained for both rising and falling cases, they are read into MATLAB using the HSPICE toolbox [5]. The MATLAB script is used to find the difference in the current at the power pin for both the circuits for the rising and falling cases as shown below:

```
diff_current_Tran_IBIS_rise = Iout_Tran_r - Iout_IBIS_rise;
diff_current_Tran_IBIS_fall = Iout_Tran_f - Iout_IBIS_fall;
```

Polynomial coefficients are obtained using the *polyfit* function in MATLAB.

Step iii): VCCS implementation: Once polynomials for the rising and falling curves are obtained, the extra current that needs to be injected in the IBIS model is done using Voltage Controlled Current Sources (VCCS). The VCCS for gate modulation effect correction is placed between the output and the ground node

```
Gphase2rise1 ph2rise1 0 POLY(1) vdd_delayed 0 scale=3 -0.0573 0.0681 -0.0203
Gphase2fall1 ph2fall1 0 POLY(1) vdd_delayed 0 scale=3 0.02154 -0.0259 0.0077
```

While these steps describe the details to obtain the black-box parameters for the rising and falling edges separately, the method also holds if a single polynomial is required for both the edges. The only difference in the extraction process would be that a 010 pulse would be supplied to the input of the driver instead of rising or falling inputs in the step i) of the process.

3. IBIS Model and Black-Box Details

The IBIS model of the DDR2 SDRAM I/O driver from Micron Inc. was made using the North Carolina State University S2IBIS3 program [2]. The black-box to perform error correction for SSN simulations is made by following the procedure described in [1]. The following SPICE code is used to implement the first phase of the error correction part of the black-box (pre-driver, crossbar and termination current):

Edge detection: A delayed input is used to detect the edges.

```
Enrise nrise 0 vol='(((vcc-v(IN_VCCS11,0))*v(IN_VCCS1,0)))'
Enfall nfall 0 vol='(((vcc-v(IN_VCCS1,0))*v(IN_VCCS11,0)))'
```

VCCS implementation: A third order polynomial was used to represent the Voltage Source Current Source (VCCS) for the correction.

```
GVCCSRise1 risePoly1 0 POLY(1) VDD1 GND1 SCALE=1 0.1568 -0.373 0.265 -0.0589
GVCCSFall1 fallPoly1 0 POLY(1) VDD1 GND1 SCALE=1 -0.1586 0.2268 -0.11 0.0186
```

The second phase (Gate Modulation Effect) of the error correction was implemented using the SPICE code as follows:

Obtaining the scaling coefficient K:

```
Ek1 k1 0 vol = '(v(VDD_VCCS1,GND_VCCS1)-v(GND_VCCS1))/vcc'
Ek2 k2 0 vol = '4*(v(k1)-1)'
```

VCCS Implementation: A second order polynomial was used to represent the Voltage Source Current Source (VCCS) for the correction.

```
Gphase2rise1 ph2rise1 0 POLY(1) vdd_delayed 0 scale=3 -0.0573 0.0681 -0.0203
Gphase2fall1 ph2fall1 0 POLY(1) vdd_delayed 0 scale=3 0.02154 -0.026 0.0077
```

The gate modulation correction is done by adding a VCCS between the output and the ground nodes of the driver as described in the previous section. An improvement of 66.54% in simulation accuracy was achieved with the blackbox. The improvement was measured using the area under the error curve method discussed in [1]. A decoupling capacitor of 38pF per driver was used with the models in the system level tests as a part of the black-box. Validation of the IBIS model and the black-box is performed in the next section.

4. Test Details and Model Validation

For the system level tests, a 128 bits Pseudo Random Bit Sequence (PRBS) was generated for the input to the system. Bit time of the generated sequence was 1ns with a rise and fall time of 0.1ns. Tests were performed with both lossless transmission line (T element in HSPICE) and lossy transmission line (W element). Results for the near end node and the far end node of the transmission line are presented.

Before system tests can be performed with the behavioral model (IBIS), it is important to check the model for accuracy when compared directly to the SPICE netlist of the I/O driver. Another reason to perform this test is to make sure that the black-box does not affect the normal behavior of the behavioral model when put in a system without any noise. The black-box should only act as supplement to the main model when fluctuations in the power/ground voltage is detected. The test setup for model validation consists of the I/O driver connected to an ideal 50 transmission line and terminated with a 50 load. The driver was connected to the power and ground without any package parasitics. The driver was given a pulse (01010) with a 0.1ns rise/fall time with the bit period of 1ns.

5. System Simulations and Results

This section describes the system level tests performed with the plain IBIS model and the improved IBIS model and their comparison with the transistor level models. Fig. 4 shows the layout for the tests that were performed on the models. A similar circuit was constructed for the transistor level model of the Micron I/O driver. The package model used for simulation is an S-parameter BGA package and is used at the power/ground pin and the output pin. Tests are done with ideal transmission line (T element) as well as lossy 10" long 12mil wide stripline transmission line using RLGC model (W element). All the tests are performed with a receiver load of 50 ohms termination.

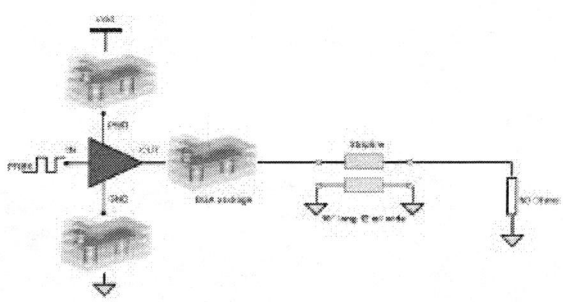
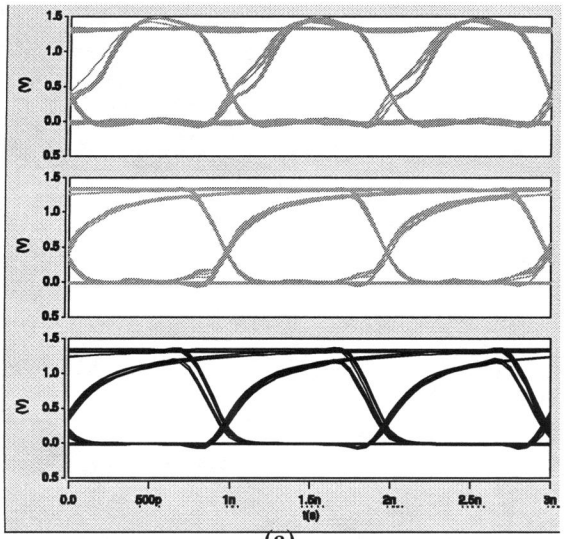
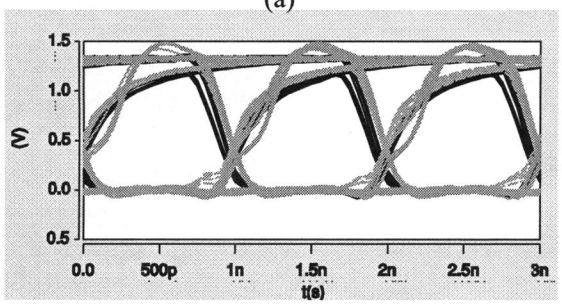


Figure 4: Test setup for System validation of IBIS model.



(a)



(b)

Figure 5: System simulation with power/ground package model, lossy transmission line. (a) Eye diagram for output for plain IBIS (blue, top), improved IBIS (purple, middle) and transistor model (black, bottom). (b) Overlay of the 3 model outputs

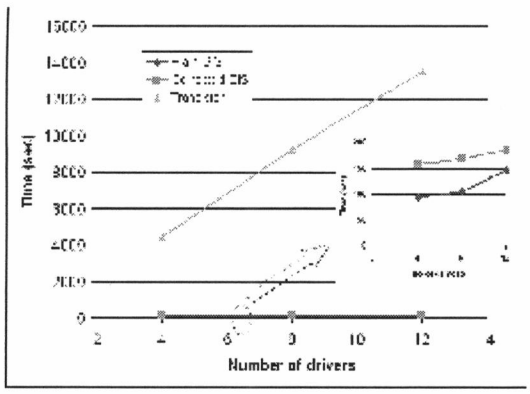


Figure 6: Simulation time (total CPU time) for SSN simulation for plain IBIS, Corrected

S-Parameter Package at power/ground, Lossy Transmission Line

As a representation of system simulation, fig 5 shows the eye diagrams at the output of the plain IBIS model, improved IBIS model and the transistor model of the driver (near end of the transmission line) individually. It presents the results of the driver model which is connected to a 10" w element stripline model at the output. The power and ground on the chip are connected to the power and ground plane through BGA package S-Parameter model. The system is terminated using a 50 resistor. Fig. 5(b) presents an overlay of the eye diagram for a comparison between the 3 models. It can be easily observed that the IBIS model with the black-box gives a much improved behavioral model and follows closely the transistor model results when compared with the plain IBIS model.

Simulation Time

Fig.6 shows a plot of the total CPU time for SSN simulations for the 3 type of models. SSN Tests were performed with 4, 8 and 12 buffers switching simultaneously with 1 quiet driver. IBIS model with the black-box has an overhead of nearly 45 seconds on an average for 4, 8 and 12 drivers switching. This simulation time overhead is still low when compared to the simulation time for transistor level models. The transistor model for the MICRON driver took nearly 4 hours of CPU time to simulate 12 drivers switching simultaneously with s-parameter package models while the IBIS models took an average of 3 minutes of simulation time to simulate the 12 drivers.

6. Conclusion

An IBIS model of a DDR2 SDRAM driver was created using an encrypted transistor netlist from MICRON Inc using S2IBIS3. For accurate SSN simulations with an IBIS model, an error correction black-box was also created for the same model that provided correction for the Gate Modulation Effect. The error correction black-box was created using a s-parameter model of a BGA package. System level simulations were performed with the improved IBIS models with a BGA package s-parameter model. An RLGC model of a stripline was also used to simulate a lossy transmission line. Eye diagrams of the 3 model types were observed for simulation accuracy. In each of the cases observed, the improved IBIS model (plain IBIS + black-box) gave better results consistently when compared with the plain IBIS model. SSN simulations with the BGA package was also completed with 4, 8 and 12 drivers switching simultaneously. An improvement in simulation accuracy of over 40% was achieved with little overhead in total cpu time for the simulations with the improved IBIS.

References

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