FreePDK: An Open-Source Variation-Aware Design Kit

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Abstract

This paper discusses an open source, variation aware Process Design Kit (PDK), based on Scalable CMOS design rules, down to 45nm, for use in VLSI research, education and small businesses. This kit includes all the necessary layout design rules and extraction command decks to capture layout dependent systematic variation and perform statistical circuit analysis. The kit also includes a standard cell and pad library with the necessary support files to enable full chip place and route and verification for System on Chip designs. Test chips designed with this PDK are designed in such a way so that they can be fabricated by fabrication facilities allowing validation of the design rules so that the rules may be used in future multi-project runs and design contests.

1. Introduction

Training the next generation of Very Large Scale Integration (VLSI) designers is becoming increasingly difficult due to the ever-changing landscape of tools and technology [1]. Large companies cope with this complexity by investing heavily in process design kits (PDKs) to communicate technology information and design flows, but universities and small companies lack the resources to develop these PDKs on their own.

Because of tight intellectual property (IP) controls on PDKs, universities are extremely limited in their ability to use them. To make matters worse, educators cannot teach fundamentals of large-scale VLSI design without these kits. And, researchers cannot make substantial progress in VLSI, because many of the ideas cannot be corroborated by implementations. Since corporations tend to use research from academic institutions in boosting their infrastructure, an obvious quagmire exists between commercial products that push the forefront of technology.

As we look to the future, the problem of obtaining adequate methods of validating designs will only continue to get worse. Ever increasing device and wire variations are leading to increasing yield loss in newer technologies. Some of these variations are random, but others are systematic. Learning how to make use of systematic variation is one of the main skills required of designers in next generation technologies in order to maintain control of the process. To enable this learning, PDKs **must** evolve to communicate layout dependencies to circuit simulators. It is likely that these new PDKs will be even more complex and have tighter IP controls, leading to a more pronounced gap between universities and large companies. It is of paramount interest that we must recognize that the problem of training VLSI designers to cope with variability surpasses the capability of any one company to solve. Therefore, it is imperative that VLSI educators and small business innovators must empower use and distribution of tools by developing up-to-date PDKs that are free from IP restrictions.

2 Design Methodology and Innovation

In order to avoid violating intellectual property, this kit is developed from the latest known set of free design rules,

which is the venerable Scalable CMOS (SCMOS) rule set. This paper makes the case that this FreePDK is necessary for three specific reasons:

1. Existing PDKs cannot be used in the classroom. With the exception of Cadence Design System's (CDS's) GPDK [2], existing PDKs from TSMC, IBM, Artisan, and others are allowed only for small research projects and are expressly forbidden to be utilized in a classroom setting. This requires universities to double their effort to support design kits for teaching and research which means that in the time between classes, professors must negotiate complicated licenses before they can begin to install the PDKs and train their students. A PDK that can be used in the classroom encourages more time investment and lead to a greater chance of success in fabrication and more productivity with research which can be translated towards advancing industrial tools and flows more efficiently.

2. Only fragmented PDKs are available to universities. Companies, such as TSMC and IBM, deliver only the basic design rules and SPICE models, without standard cell or Input/Output (I/O) pad libraries. Standard cells are available from Artisan and LSI Logic, but without complete layout views. The lack of these layout views prohibits the execution of detailed layouts.

3. Modification and redistribution of existing PDKs are prohibited . The CDS GPDK addresses the two limitations mentioned above, but CDS still prohibits any modification and redistribution of their GPDK. Given that the GPDK still lacks many features, such as variation awareness, each university must independently invest the effort to develop the GPDK for education, a task that outstrips their resources and main purpose. For these reasons, we firmly believe that there is no alternative but to recreate an open source PDK from the latest free set of design rules.

This work is designed in complete open design flows from $0.5\ \mu$m down to 45 nm using rules adapted from the Scalable CMOS rules, the Cadence Design Kit developed at NCSU, and previously developed System on Chip (SoC) standard-cell libraries and design flows [2][1]. For each minimum feature size, references to the ITRS [1] and conference publications, such as IEDM and IITC, are collected that indicate how the rule should be adapted at or below 90nm, as well as the amount of variation that should be expected.

The theory behind these design flows is to advance the state-of-the-art design tools by utilizing the innovate tools that are already on the market from major EDA vendors. However, interfaces between public-domain tools, such as

Electric and Magic, are also given to allow users to interface potential research-enabled academic third-party tools that may advance scientific discovery into VLSI and possibly lead to better tools for companies and potential academic-commercial research collaborations. The design flow has been successfully tested in a large VLSI class for junior and senior undergraduate students with great success. Students build a full-scale microprocessor composed of custom and standard-cell parts. Many students commented that they are able to comprehend VLSI design more intuitively, since they have first-hand knowledge of the issues pertaining to a large VLSI design.

Since the design flows should enable different VLSI vendors the opportunity to fully utilize design kits, each flow is designed to work completely or separately within each vendor. Currently, the tools are designed to work with complete Synopsys and CDS front-end and back-end tools, however, more tools will be integrated with other vendors in the future. This allows each user to use the tool they feel more comfortable with and opens up many more possibilities with interchanging design tools facilitating research-driven extensions.

Many commercial flows utilize heavy amounts of standard cells to allow different impedances to match against a library set. Most companies that provide standard cell flows have a large number of cells as well as IP cores that give them huge advantages over ones that are created in-house. In order to give more credence to the design library developed for this work, a large number of cells are automatically generated with a tool from Synopsys, called CADABRA, including CDS Encounter and Synopsys Astro support. I/O libraries are also automatically created using a custom-based CDS SKILL script.

3 Conclusion

A free and publicly available design kit is presented and available for researchers to utilize in research and education. The tools are developed based on SCMOS design rules and are available for fabrication through the MOSIS Educational Program. The tools developed in this work are heavily employed within undergraduate-based VLSI courses at both institutions.

References

[1] International Technology Roadmap for Semiconductors. Technical report, Semiconductor Industry Assocation, 2003.

[2] J. E. Stine, J. Grad, I. Castellanos, J. Blank, V. Dave, M. Prakash, N. Iliev, and N. Jachimiec. A Framework for High-Level Synthesis of System-on-Chip Designs. In *International Conference on Microelectronic Systems Education*, pages 67–68. IEEE Computer Society Press, 2005.

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[1]available at http://freepdk.ecen.okstate.edu and http://www.cadence.ncsu.edu/

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