Considerations for Transmission Line Design on MCMs using AC Coupled Interconnect with Buried Solder Bumps

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Abstract

AC Coupled Interconnect (ACCI) using buried solder bumps is a technology that provides a complete interconnect and packaging solution by integrating high-density, low inductance power and ground distribution with high-density, high-speed I/O. The mixture of solder bump technology and AC coupled I/O has the potential to improve yield during packaging and assembly since I/O channels are no longer dependent on the yield of a single solder bump. For the same reason, this technology has the potential to increase the long-term reliability of chip/carrier components of electronic systems used in harsh environments *(e.g. extreme vibration, shock, and temperature variation)*. An important consideration in systems using this technology is how the electrical properties of transmission line are altered when it is routed beneath a die that is in close proximity (< 5μm) to the surface of the substrate.

Keywords: ac coupled interconnect, acci, buried solder bumps, transmission lines, routing, MCM, stripline

Introduction

The key concept in ACCI is that DC connections are not needed to convey the high frequency content of AC signals. Instead, the information in these signals can be coupled via "AC connections", such as a series capacitor. Shown in Figure 1, is an illustration of the physical ACCI system with two chips mounted on a common substrate using buried solder bumps. The buried solder bumps provide power and ground to the mounted chips, and are also used to self-align the AC coupling elements and control the resulting gap between the chip and substrate. The resulting gap is determined by the size of the pads where the solder bumps reflow, the volume of solder, and the depth of the trench on the substrate.

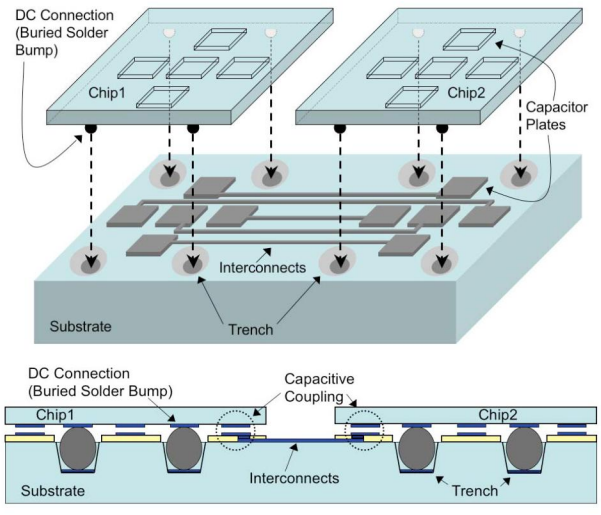


Figure 1: ACCI Structure: "3-D" view & cross sectional view

In a typical flip-chip assembled system, the distance between the substrate and the die is generally large when compared to the dimensions of the signal lines routed on the substrate. This large separation means that the die mounted above the substrate do not significantly affect the characteristic impedance of the lines on the substrate. However, as die come into close proximity with the surface of the substrate, the presence of conductive materials and high permittivity dielectrics, begin the influence the electrical properties of transmission lines routed on the substrate beneath the die. This influence needs to be considered and a method for controlling the characteristic impedance of lines routed beneath die on the substrate needs to be established.

Substrate with Buried Solder Bumps

To demonstrate ACCI with buried bumps, a multi-metal layer substrate was design and fabricated. The substrate was manufactured using a silicon wafer with five copper interconnect layers, each 2μm thick, and four BCB dielectric layers, of varying thickness. Benzocyclobutene (BCB) was chosen for the dielectric layers because of its low permittivity ($\varepsilon_r \sim 2.65$) and excellent planarizing properties. Shown in Figure 2 is an illustration of the substrate stack-up showing the thickness of each dielectric layer. The lower two metal layers (M1, M2) are used for power and ground distribution, as references planes, and to form the contacting layers for the buried bumps. The two metal layers (M3, M4) embedded in dielectric are used for the routing of transmission lines (T-lines) and the top metal layer (M5) is mainly used to form the AC I/O structures. In some situations, the top metal layer is also used to create low-loss micro-strip lines for long runs across the substrate. *(A demonstration of two CMOS chips communicating at 2.5Gb/s/channel across lossy transmission lines, on this substrate, has been reported [1].)*

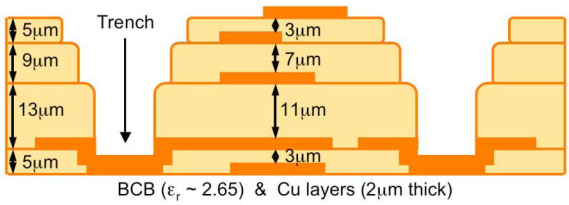


Figure 2: Multi-layer stack-up with trenches for buried bumps

Shown in Figure 3 is a cross section of an assembled substrate and CMOS chip. Coupling capacitors formed by the substrate and chip interface can be seen between the buried bumps. This intimate contact resulted in a separation between the chip and substrate capacitor plates of approximately 1μm and was chosen so that the performance at minimum separation could be established.

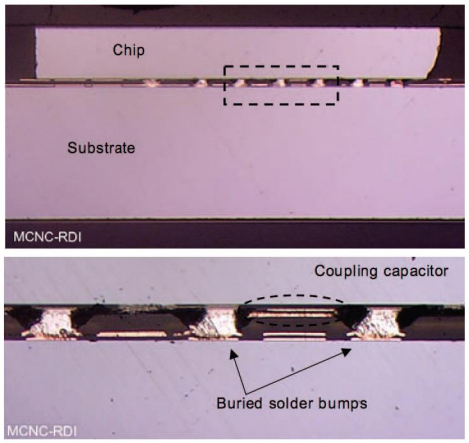
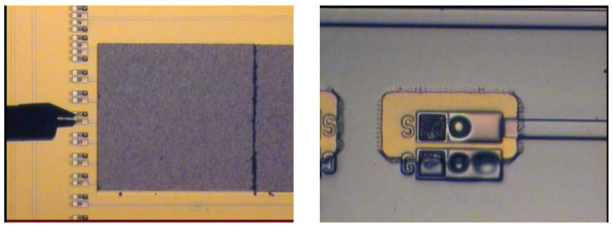


Figure 3: Multi-layer stack-up with trenches for buried bumps

Transmission Lines in ACCI: Impact of Die & Evaluation

During the evaluation of the initial qualification process run, it was determined that the top metal layer would also need to be used as a reference plane to form strip lines using M3 when transmission lines are routed beneath die. This enables the formation of transmission lines with predictable and controlled impedance to be routed beneath die.

Die were placed face down on the substrate and the characteristic impedance of transmission lines in M4 was measured using a Tektronix 11801B Digital Sampling Oscilloscope in TDR mode. Shown in Figure 4a are multiple die placed face down above a transmission line under test. The influence of the die was measured and shown to be significant. This forces the use of striplines when T-lines pass beneath die, and given the dimensions of the layer stack-up (see Figure 2), forced our design to use M3 lines when routing beneath die. To evaluate the conversion of embedded micro-strip lines to striplines, we measured a set of T-lines on a wafer and then deposited reference plane (0.8μm Ti/Cu) and measured the same lines again. Figure 4b shows a GS probe pad with the added metal that was opened for the signal probe tip.



(a) (b)

Figure 4: (a) die placed on substrate, (b) added reference plane

Shown in Figure 5 is a comparison of TDR measurements for a 46μm wide and 50mm long line in M4, with and without die placed on top of the substrate. The die (5 - each 2x2mm) were placed near the center of the line to emulate the presence of a bump attached die in close proximity to the substrate. It is evident from the change in the characteristic impedance, that these die have a significant influence on the underlying T-line.

The addition of the reference plane on the top surface of the wafer enables the routing of T-lines beneath die, and adds the benefit of reducing the required line width to achieve the desired system impedance of 50Ω. A comparison of the line impedance for 25mm long M3 lines (varied from 6-24μm in 3μm steps) is shown in Figures 6 and 7. The waveforms in Figure 6 show that the impedance of the embedded micro-strip lines vary from 50-95Ω. After the conversion to strip lines the range of impedance values varies from 40-75Ω, as shown in Figure 7. The conversion to strip line reduces the required line width by 50%, from 24μm to 12μm, and enables denser routing without the need for additional layers in the substrate.

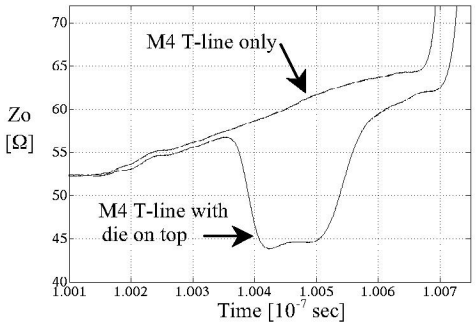


Figure 5: TDR measurement of T-line: with & without die

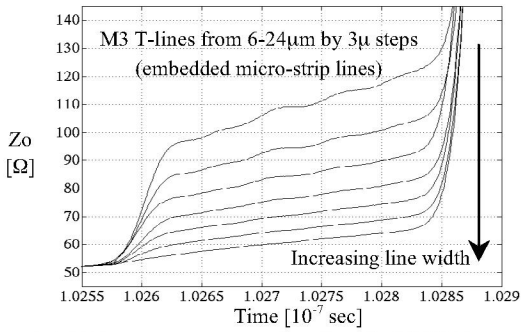


Figure 6: TDR measurement of embedded MS lines

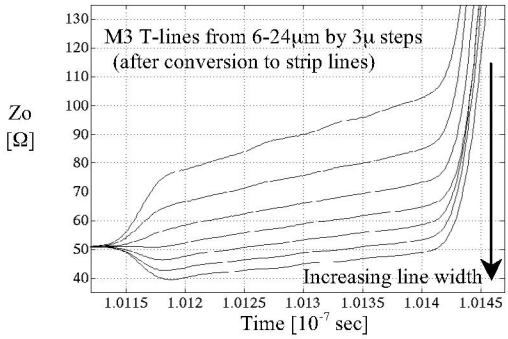


Figure 7: TDR measurement of striplines *(addition of Ti/Cu)*

Conclusions

It has been shown that the best topology for T-line design in MCMs using ACCI is a strip line structure when the T-line is routed beneath die. For the example shown in this work, the required line width was reduced by 50%. This saves routing area and is not limited to systems using buried bumps. Once routed lines escape the edges of the die, these lines can be converted to micro-strip, as the available periphery permits, to reduce the losses of the lines.

References

[1] J. Wilson, J. Xu, S. Mick, L. Luo, S. Bonafede, A. Huffman, R. LaBennett, P. Franzon, "*Fully Integrated AC Coupled Interconnect using Buried Bumps*", IEEE, 14th EPEP, Austin, TX, pp. 7-10, Oct. 2005.