AC Coupled Interconnect using Buried Bumps for Laminated Organic Packages

John Wilson[1], Lei Luo[1], Jian Xu[1], Stephen Mick[1], Evan Erickson[1], Hsuan-Jung Su[1],
Benson Chan[2], How Lin[2], Paul Franzon[1]
[1]North Carolina State University, Dept. of Electrical and Computer Engineering, Box 7911, Raleigh, NC 27695
{ jmwilson , lluo3 , jxu6 , semick , elericks , hsu , paulf } @ncsu.edu
[2]Endicott Interconnect Technologies, 1701 North Street, Endicott, NY 13760
{ benson.chan , how.lin } @eitny.com

Abstract

Various techniques for providing non-contacting, inter-chip signaling have been demonstrated, such as: ACCI [1,2], proximity communication [3], and wireless superconnect (WSC) [4]. ACCI using buried bumps is the only technology that provides a manufacturable solution for non-contacting I/O signaling by integrating high-density, low inductance power and ground distribution with high-density, high-speed I/O. This completely integrated solution has been demonstrated at 2.5Gb/s/channel across 5.6cm of micro-strip transmission line using 0.35um CMOS ICs that were flip-chip attached onto a silicon MCM-D [5].

Introduction

The combination of solder bump technology and AC coupled I/O has the potential to improve yield during packaging and assembly since the yield of an individual I/O channel is no longer dependent on the yield of a single solder bump. In other words, unless the assembled module loses so many power and ground bumps that the integrity of the power supply grid suffers, the yield of assembled modules should increase. For the same reason, this technology has the potential to increase the long-term reliability of chip/carrier components of electronic systems used in harsh environments *(e.g. extreme vibration, shock, and temperature variation)*. The buried solder bump technique can also be combined with a high-k dielectric underfill to reduce the required area for coupling capacitors while relaxing the requirements on inter-plate separation, and also provide stress relief between die and substrate [6].

Currently, state-of-the-art laminated organic packages use materials that are compliant and designed specifically to match the coefficient of thermal expansion (CTE) of the C4 bump attached die to a printed circuit board (PCB). This interposer must also accommodate and absorb any deviations in the planarity of the inexpensive PCB. These compliant interposers extend the physical size of the die that can be bumped attached without the use of solder columns; however, there is still an upper limit on die size. This paper explores potential methods for increasing the maximum die size allowed, or relaxing the CTE compensating requirements of the compliant interposer, by using AC coupled I/O and buried solder bumps. One method for accomplishing this is by clustering the buried bumps in a "common trench" located at the center of the die. The bumps placed in the center of the die will be comprised of power and ground bumps. *(If there is a requirement for having bumps for reference signals, such as a current bias signal, then these "critical bumps" should be located centrally so that the CTE mismatch will be near zero between the die and interposer. This assumes the neutral point is located at the center of the die.)* By placing all the solder bumps in this "common trench" located at the center of the die, the maximum size of the die can be increased as long as size of the solder bump array does not exceed standard die/package limits. All high-speed I/O are arranged around the periphery of the die, and use ACCI signaling techniques to communicate with the remaining system components. If there is a need for digital control signals, these can also be created using the AC coupled interface as long as they transition after start-up. Or they can be classified as "critical bumps" and placed at the center of the die. This combination of technologies also has the advantage of reducing the number of solder bumps required for a high I/O count chip and package interface, since the bumps used for power and ground are redundant and even the loss of a few bumps can be tolerated with sufficient over design. Another advantage is that larger solder bumps can be used. This helps to improve the reliability of the individual solder bump, since the strength of a solder bump increases with its volume. In addition, the induced strain decreases with increasing bump height .

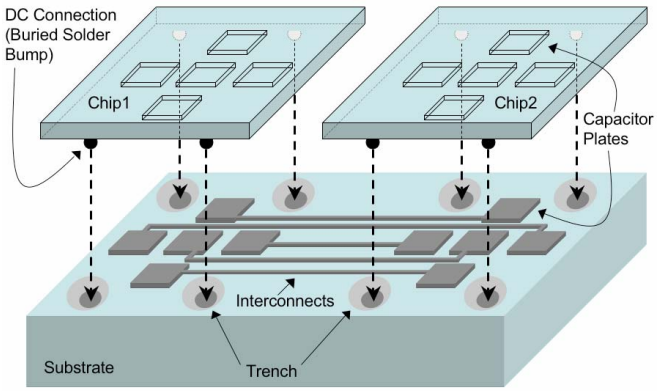
A test chip has been designed in 0.18um CMOS technology and a laminated organic interposer is being designed to demonstrate this technology. The test chip has demonstrated simultaneous operation of six channels at 6Gb/s/channel (36Gb/s aggregate) using on-chip metal-insulator-metal capacitors that were wire bonded to transmission lines on a FR4 PCB, but this only verifies the functionally of the transceivers across a range of appropriately sized coupling capacitors (85-185fF) and various lengths of transmission line (20-45cm). The results of this test chip are presented, along with the results of a demonstration of AC Coupled Interconnect where a coupling capacitor was formed when die and package where assembled to create a MCM-D.

ACCI Physical System

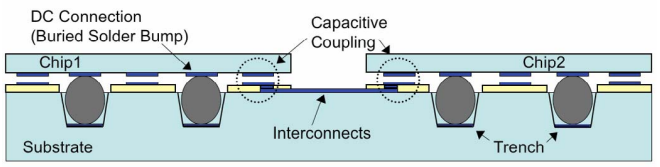
An illustration of the physical ACCI system with two chips mounted on a common substrate using buried solder bumps, is shown in Figure 1. The buried solder bumps provide power and ground to the mounted chips, and are also used to self-align the AC coupling elements and control the resulting gap between the chip and substrate. This example uses multiple die to communicate on a common substrate; however, the package can be also an interposer, which will be considered in this paper.

The key concept here is that DC connections are not needed to convey the high frequency content of AC signals. Instead, the information in these signals can be coupled via "AC connections", such as a series capacitor, via the fast edges of digital signals. The goal of using AC connections is

to make circuit design considerations the limiting factor to achieving high I/O density. The challenges for laminate packages are more sever than those of silicon or ceramic packages, and will require careful consideration and incorporate many technologies to become a viable solution.



(a)



(b)

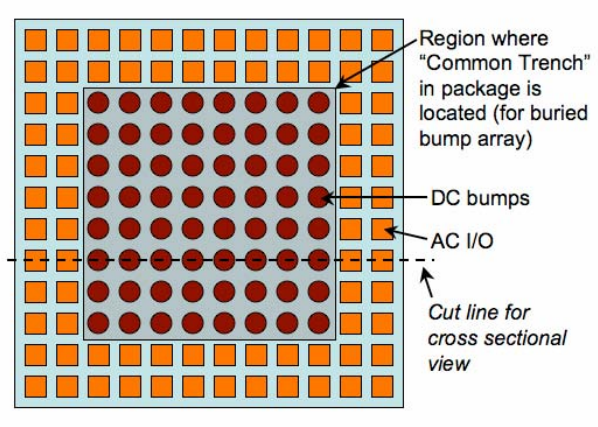
Figure 1: ACCI Physical Structure: (a) 3D view, (b) cross sectional view

ACCI for Laminated Organic Packages

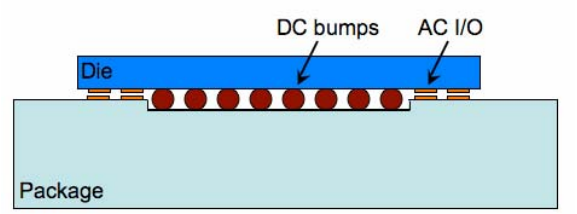
There are numerous methods to implement ACCI using buried bumps. The buried bumps could be distributed evenly with the AC I/O, or the buried bumps could be arranged around the periphery with the AC I/O located near the center of the die. One of the main challenges for large die attached to laminate interposers is dealing with the thermo-mechanically induced stresses due to the CTE. Since the strain induced on a solder ball is reduced by decreasing its distance from the neutral point (DNP), it is beneficial from the stand point of increasing bump reliability to cluster the bumps in a "common trench" and locate the AC I/O around the periphery of the die. This topology has the potential to increase the maximum allowed die size for a particular packaging technology.

Figure 2 illustrates the concept of ACCI using buried bumps for laminated interposers. In this example, the DC bumps are centrally grouped in a "common trench" that can be easily manufactured with the addition of a few processing steps that are currently available in the standard process. Currently, an effort to demonstrate this using Endicott Interconnect Technologies' HyperBGA [7] interposer is in progress. The goal is to demonstrate ACCI using the HyperBGA package with a minimum number of additional manufacturing steps.

Figure 3 is a cross sectional view of an assembled die and HyperBGA package, showing a C4 solder bump used to attached the die and provide electrical connectivity. The copper-invar-copper, various dielectric and metal layers of the package are visible in the image.



(a)



(b)

Figure 2: ACCI Physical Structure for laminated interposers: (a) Top view of package, (b) cross sectional view of assembled die and interposer (package)

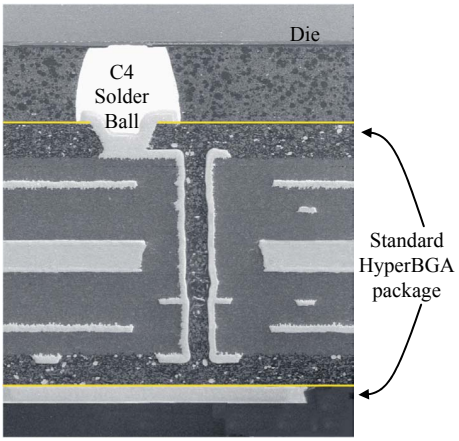


Figure 3: Cross sectional view of die attached to HyperBGA package

There are two main modifications that have to be made to this package to make it possible to incorporate ACCI and buried bumps. The first modification is to create the "common trench" for the buried bumps. Since this is planned to be a large trench that is centrally located beneath the die, there is no need to create individual trenches for each solder bump, which greatly simplifies the manufacturing. A photo definable dielectric layer, with a thickness sized appropriately with the bump height, will be used to create the trench. This dielectric

layer will also be processed to create filled and flattened vias that form AC I/O pads to interface with attached die. The second modification is the incorporation of embedded resistors to provide termination, if required, for the transmission lines on the PCB. Figure 4 is an illustration of the HyperBGA package modified for ACCI using buried bumps.

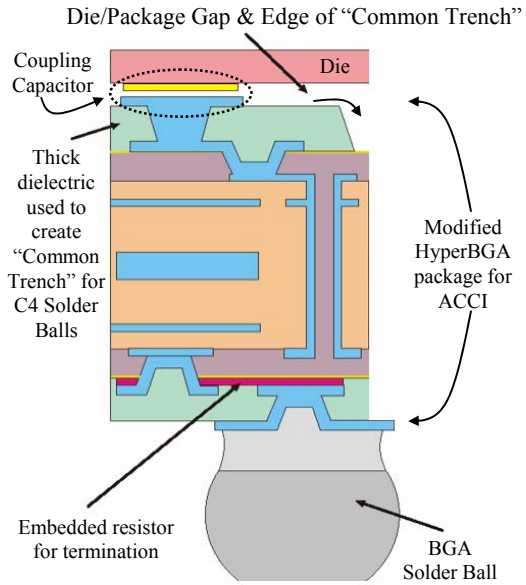


Figure 4: Cross sectional view of HyperBGA package modified for ACCI using buried bumps

An important consideration is how a stress-relieving underfill will be dispensed between the die and package. Different solutions are being considered, but since the most popular techniques use edge-dispensed underfills, which "wick" beneath the die and package via capillary forces, we have chosen to investigate a compatible solution. When using the "common trench" approach for the buried bumps, the gap between the die and package will be significantly smaller around the periphery of the die. This small gap will prevent capillary underfills from penetrating the void between the die and package. To mitigate this problem we are investigating the use "underfill inlets" at each corner of the attached die, that would have a depth approximately the same as the typical die-to-package separation in a standard HyperBGA die/package assembly. The underfill would be dispensed as needed until a thorough application was achieved. There are other methods for applying stress-relieving underfills, and they are being considered as well. One trade-off of this approach is that the area on the die above the "underfill inlet" cannot be used for AC I/O. At this point, it has not yet been determined if these inlets can still be populated with DC bumps, but the limits of the die/package thermo-mechanics may prevent this option. In addition, the presence of bumps in the inlet may impact the ability of underfills to wick beneath the die and package effectively. Figure 5 illustrates the concept of creating "underfill inlets" on the package side. Also, illustrated are "critical bumps" located in the center of the die package interface.

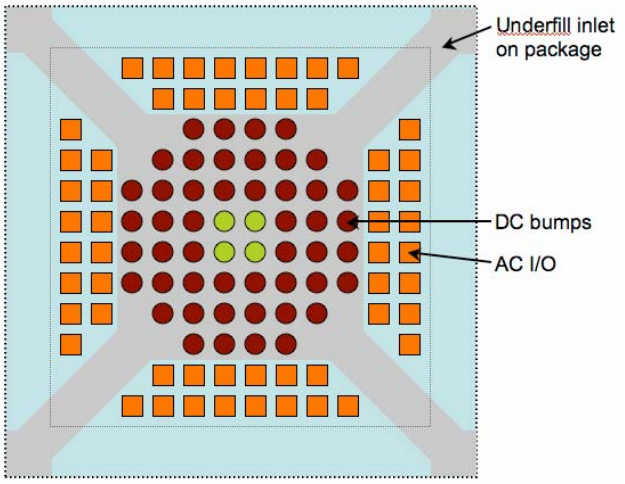


Figure 5: Top view of package modifications to create "underfill inlets"

As the die size for large digital systems continues to grow, their I/O needs also increase. It is estimated that the die size for high-performance digital systems will be 804mm^2 by 2011 [8], and the projection for maximum flip-chip I/O count is 10,000 with a minimum pitch of 150µm by 2010 [9]. To investigate the use of ACCI and buried bumps in an application with similar specifications, we have presented some approximate figures in Table I. These figures were generated by assuming a die area of 804mm^2 (28.35mm x 28.35mm) and a pitch that ranged from 333µm down to 166µm, for both DC bumps and AC I/O. We assumed that by 2011 a high-performance package would be able to accommodate up to a 22mm x 22mm die area for C4 bumps (484mm^2), and that the remaining area would be used for AC I/O, and any die area above the "underfill inlet". Our estimate shows that 47% of the die area could be used for DC bumps (379 mm^2 / 804mm^2), 25% of the die area could be used for AC I/O pads (201 mm^2 / 804mm^2) with an additional 9% (75 mm^2 / 804mm^2) allocated to create large coupling capacitors to provide a close proximity common-mode return path for differential signaling, with the remaining die area being that which is above the "underfill inlet". Figure 6a is an illustration of this estimate for a 250µm X/Y pitch and includes the area void of DC bumps and AC I/O due to the "underfill inlet" on the package. Figure 6b is a zoomed in view showing all the features on the die *(i.e. DC bumps, AC I/O, return path coupling pads, area over "underfill inlets").* Each underfill inlet is 5mm wide x 8mm deep in this example.

Table I: Potential DC and AC I/O Count for 804mm^2 die

X/Y Pitch / **I/O Type**	333µm	**250µm**	200µm	166µm
DC Bump Count *(379 mm^2 / 804mm^2 = 47% of area)*	3411	**6064**	9475	13644
AC I/O Pad Count *(201 mm^2 / 804 mm^2 = 25% of area)*	1809	**3216**	5025	7236

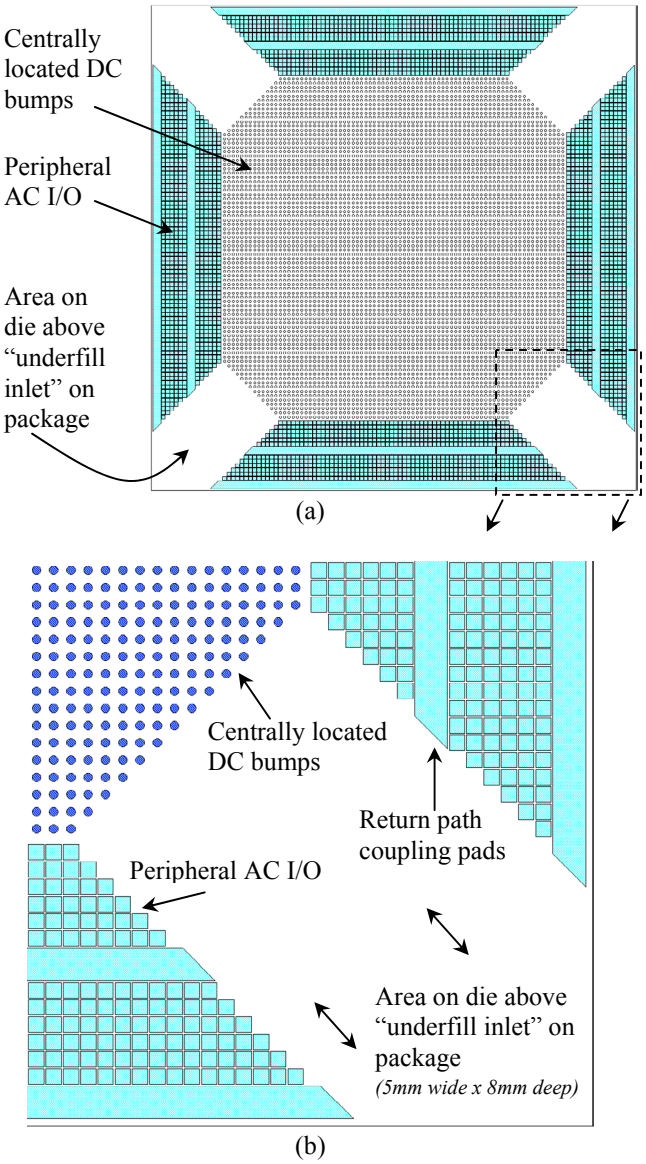


Figure 6: (a) Potential DC and AC I/O arrangement using a 250µm X/Y pitch for 804mm^2 die, (b) zoomed in view showing features

Wire Bonded ACCI Test Chip in 0.18µm CMOS

A test chip with multiple TX and RX circuits was fabricated in the TSMC 0.18µm CMOS process, and is shown in Figure 7. This test chip includes experiments to evaluate ACCI using on-chip metal-insulator-metal (MIM) capacitors that are wire bonded to a PCB, and coupling plates used to create inter-chip/package capacitors for a complete system using buried bumps. This chip has been designed so that these inter-chip/package capacitors can be formed with both a MCM-D and a laminate package (HyperBGA). The centrally located DC bumps are on a 200µm X/Y pitch, with C4 bump landing pads having a diameter of 30µm for the MCM-D, and 100µm for the laminate package. The dotted box in Figure 7 indicates where the DC bumps are bound, and the area outside the box shows what portion of the die periphery is used for the AC I/O and wire bonded experiments. It was not necessary to allocate any of the die for underfill related experiements, given its small size (~ 3.3mm x 3.3mm). *(Separate tests using large die, are in place, to evaluate underfill related research.)* Figure 8 shows the floor plan of the experiments on the test chip, the DC bump and wire bond pad use, and probe pads.

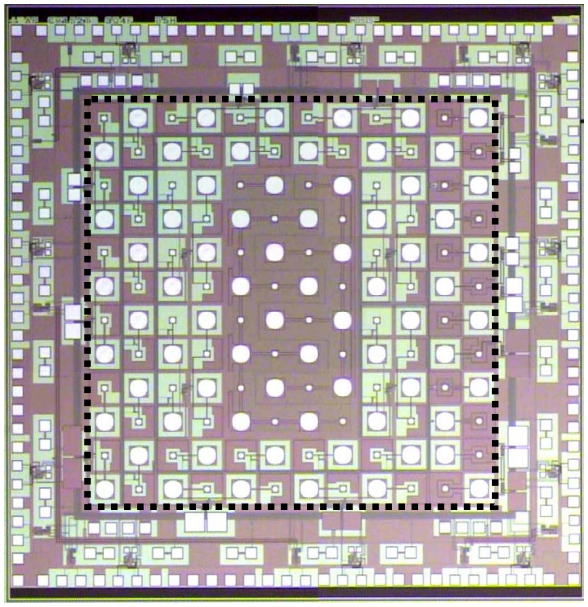


Figure 7: TSMC 0.18µm CMOS test chip to evaluate ACCI using buried bumps on laminate packages *(boxed region delineates DC bumps from AC I/O and wire bonded experiments)*

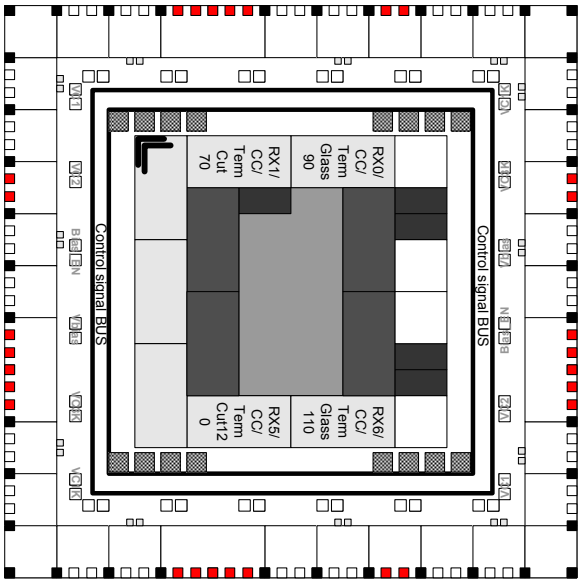


Figure 8: TSMC 0.18µm CMOS test chip floor plan

Test Setup for Wire Bonded ACCI

The measurements reported in this paper are for the wire bonded experiments located around the periphery of the test chip. Each TX and RX layout occupies an area of 40µm×20µm and 60µm×60µm, respectively. All the TX, RX, coupling capacitor landing pads, and power supply pads are

located around the periphery of the chip. The coupling capacitors vary from 85 - 185fF to determine the range for valid operation. The ACCI link is composed of on-chip Metal-Insulator-Metal (MIM) capacitors and the coupled micro-strip T-line on FR4. Figure 9 shows one test case with 30cm long 50Ω T-lines with a pair-to-pair space of 20mil. Measurements show that 6 channels can work simultaneously at 36Gbps, while all are subject to crosstalk noise and switching noise generated from the RZ pulse signaling. This experiment has two chips that are wire bonded to a FR4 PCB.

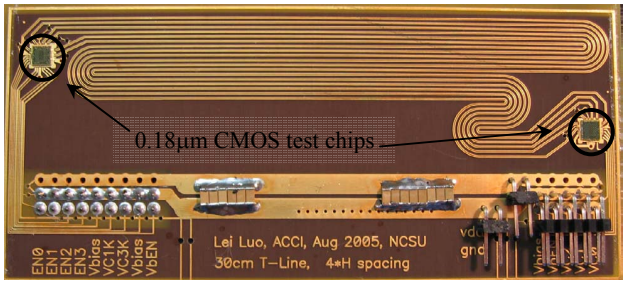
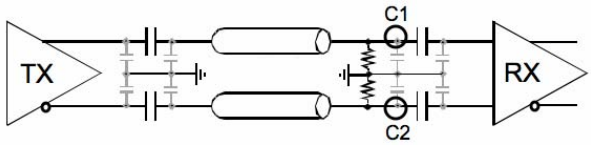


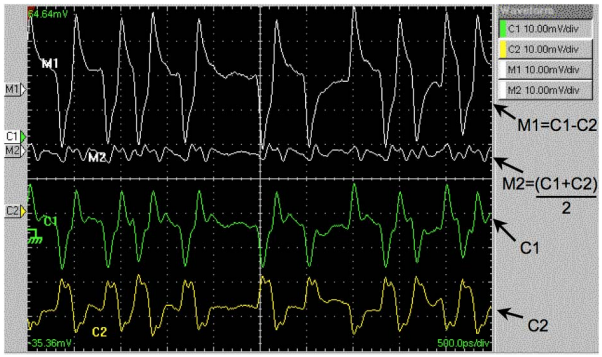
Figure 9: TSMC 0.18µm CMOS test chips wire bonded to a FR4 PCB with 6 channels, each a 30cm long coupled micro-strip transmission line with 5mil W/S and 20mil separation

Measurement Results for Wire Bonded ACCI

Figure 10 shows a schematic of the tested system and where the measured RZ pulse signals (C1, C2) were measured on the transmission line side of the RX side coupling capacitor. It also shows the differential mode (M1) and common mode (M2) of the two RZ pulse signals. The swing and width of the pulse depends on the size of the coupling capacitors and T-line length.



(a)



(b)

Figure 10: Measured results for wire bonded TSMC 0.18µm test chip – before coupling capacitor at RX input: (a) system schematic showing measurement point, (b) measured waveforms

Summaries of the simulated and measured results are shown in the shmoo plot of Figure 11. The grey and white blocks indicate simulated pass and fail for a range of coupling capacitance (CC) and T-Line values. The "P/F" shows the actual measured pass/fail values. The measurement results agree with the simulation results, showing two possible failure regimes. One is the ISI limited area and the other is the swing limited area. Figure 12 shows a schematic of the tested system and where measurements of the differential signal and single ended signals of the pulse receiver's output were taken. Also included are eye diagram measurements based on a PRBS-127 input, with all six channels running at 6Gb/s/channel with no detectable errors.

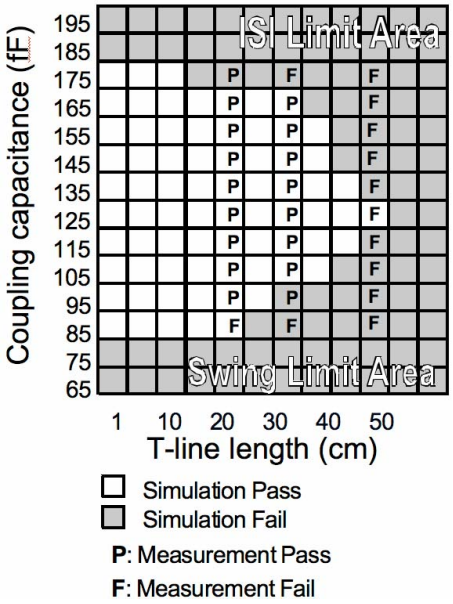
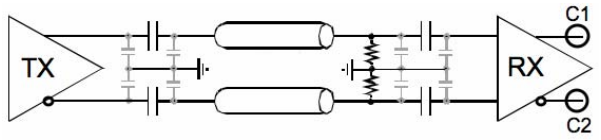


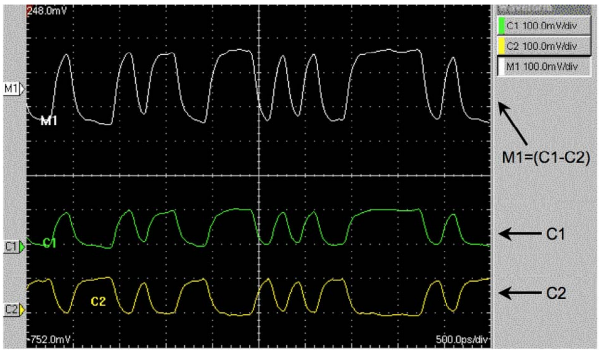
Figure 11: Summary of system pass and fail for simulations and measurements across simultaneous variations in coupling capacitor size and transmission line length

In these simulations and measurements, the coupling capacitance was simultaneously varied on both sides of the channel. This demonstrates the functionality of the transceivers on the test chip across a wide range of coupling capacitor values. The range of coupling capacitor values could result from variations in the height of the solder balls (i.e. variations in the gap between the chip and package coupling plates). This robust performance will help to compensate for manufacturing variability. Also demonstrated was the range of transmission line lengths that can be used as a function of coupling capacitor variations.

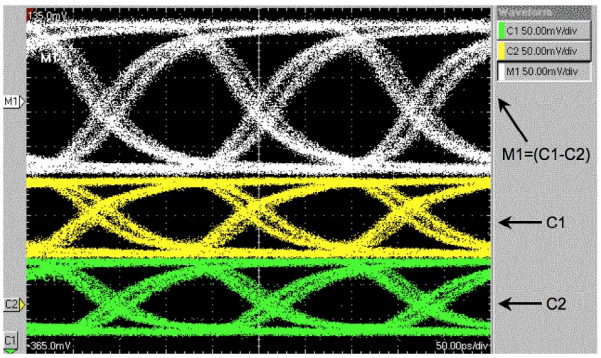
To summarize, this test chip demonstrates 36Gbps chip-to-chip communication over a 6-bit wide ACCI bus, with coupling capacitors as small as 95fF, using a 30cm micro-strip line on FR4, while subject to crosstalk and switching noise. The total transceiver power consumption is only 12mW per I/O at 6Gb/s/channel (PRBS-127). This work shows that capacitively coupled links can achieve the same data rates as conductive links with low power dissipation.



(a)



(b)



(c)

Figure 12: Measured results for wire bonded TSMC 0.18µm test chip – at RX output: (a) system schematic showing measurement point, (b) measured waveforms, (c) measured eye diagrams

Demonstration of ACCI using a MCM-D

A complete demonstration of ACCI using a silicon MCM-D as a substrate and test chips fabricated in the TSMC 0.35µm CMOS process is presented in this paper. In this demonstration two channels operated simultaneously at 2.5Gb/s/channel. The silicon substrate used in this demonstration has five copper metal layers for power, ground, signal routing, and coupling element formation. Benzocyclobutene (BCB) was chosen for the dielectric layers because of its low permittivity (ε_r ~ 2.65) and excellent planarizing properties. Figure 13 shows the stack-up of the five metal layer substrate with trenches for buried bumps.

Figure 14 shows the ACCI equivalent circuit for the system. It includes the transmitter and receiver chip, and the substrate with a 5.6cm long 50Ω micro-strip line. The capacitive coupling element is formed between the top metal layer on the substrate and the top metal layer on the CMOS chip. The conformal, 1.7µm thick glass from fabrication is left as-is covering the portion of the capacitive element on the CMOS chip. The corresponding portion of the capacitive element on the substrate is not covered by a dielectric. The capacitor plate size for this work is 200µm x 200µm *(i.e. a 270fF coupling capacitance for a 1µm air gap between capacitor plates)*, and this element could be used for I/O pitches just above 200µm, because of the comparatively low lateral coupling. Scaling to a 0.18µm circuit technology allows the coupling capacitor to be less than 80µm x 80µm.

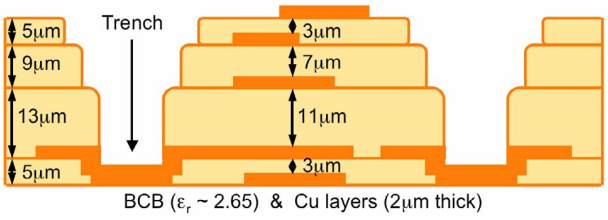


Figure 13: Substrate with trenches for buried bumps

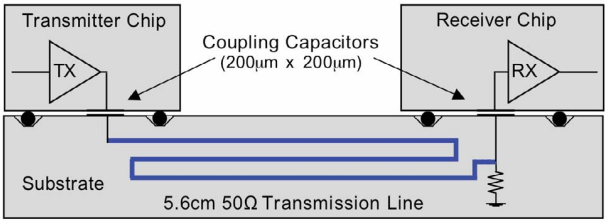
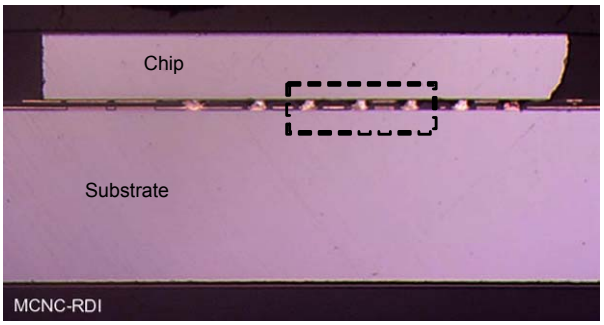


Figure 14: ACCI MCM-D Demonstration System

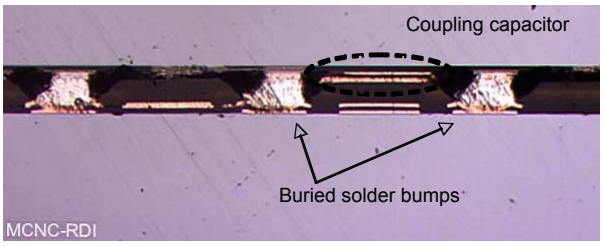
Assembled Chips and Substrate using Buried Bumps

Figure 15 shows the cross section of an assembled substrate and CMOS chip. Coupling capacitors formed by the substrate and chip interface can be seen between the buried bumps. From the images in Figure 15 it can be seen that there is slight misalignment in coupling elements (~5µm). Misalignment in this case is due to the fact that the chips and substrates were deliberately brought into contact and friction at the interface prevented the solder bumps from self-aligning. This intimate contact resulted in a separation between the chip and substrate capacitor plates of approximately 1µm and was chosen so that the performance at minimum separation could be established. By controlling the solder ball volume and re-flow parameters, any specific gap distance can be achieved. The capacitor shown in Figure 15 is smaller than that used in this demonstration.

The ACCI system can be scaled to interconnect multiple ICs. Shown in Figure 16 is a photograph of an assembled substrate populated with two CMOS ICs and eight decoupling capacitors. The substrate has two chips mounted, but can accommodate up to four chips and includes eight sites for C4 solder ball style de-coupling capacitors (two per chip). Figure 16 also shows a die photo of the TSMC 0.35µm CMOS chips used in this system demonstration and a zoomed in view of a mounting site for the IC on the substrate. The zoomed in view shows solder bump trenches that are 30µm deep, and plates corresponding to the capacitive AC coupling elements on the surface of the substrate. The substrate is 25mm x 12.5mm and each chip is 3.2mm x 3.2mm.

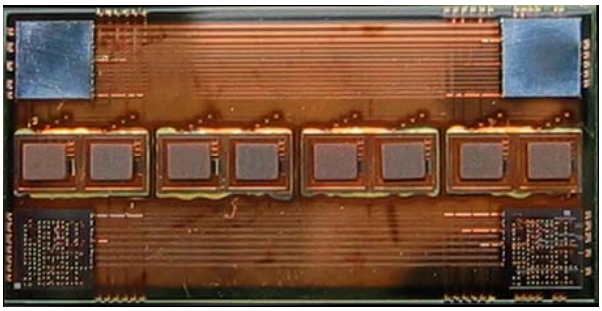


(a)

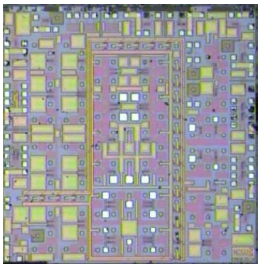


(b)

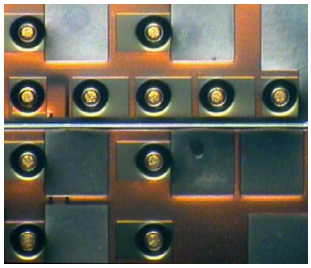
Figure 15: Cross sectional views: (a) substrate and chip, (b) buried bumps and coupling capacitor



(a)



(b)



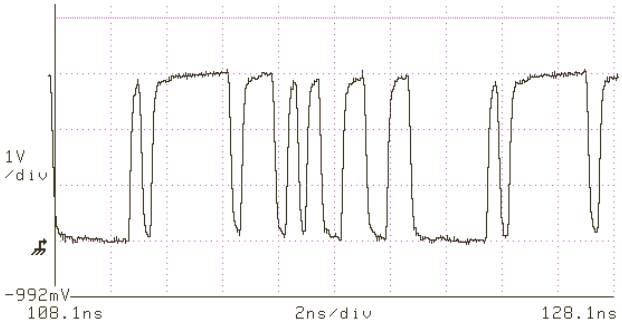
(c)

Figure 16: ACCI Demonstration System: (a) assembled MCM-D, (b) chip, (c) trenches for buried bumps and AC I/O

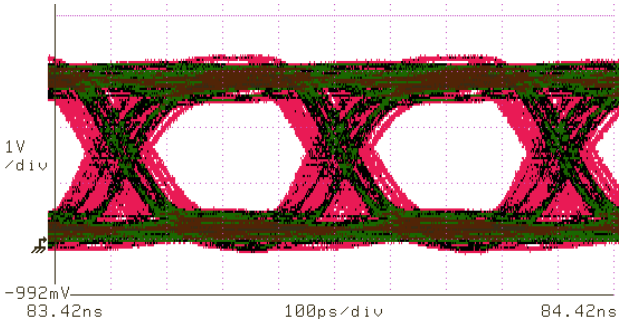
Measured Results for ACCI using a MCM-D

For testing, two CMOS chips were mounted to a substrate, as shown in Figure 16, and to facilitate measurements this system was then mounted to a PCB. Although both CMOS ICs are identical, only the transmitter circuits were used on one IC to drive data across the channel, and only the receiver circuits on the other IC were used to recover data from the channel. Input data was provided by an Agilent PRBS source and output data was measured with a Tektronix DSO and Agilent BERT using GGB high-impedance active probes. Two transmitters on the TX chip were driven by separate channels from the PRBS source at 2.5Gb/s/channel for a total throughput of 5Gb/s, across two 5.6cm long meandering 50Ω micro-strip lines on the substrate. With a 3.3V Vdd, the transmitter consumed 10.3mW and the receiver consumed 15.0mW, for a total power of 25.3mW, at 2.5Gb/s/channel. Table II summarizes system specifications and performance.

Figure 17 shows the measured output of the RX chip for both a 32-bit arbitrary data pattern and PRBS (2^7-1) data on channel-1, while channel-2 transmits and receives PRBS (2^7-1) data. Each channel operates without error in the presence of power supply noise from the adjacent channel. The peak-to-peak jitter on the PRBS data of channel-1 is less than 120ps. Bit error rate (BER) measurements of the system at 2.5Gb/s/channel are better than 10^{-12}.



(a)



(b)

Figure 17: Measured output for two channels operating at 2.5Gb/s/channel: (a) 32-bit arbitrary pattern, (b) PRBS-127 eye diagram

Table II: Performance Summary for MCM-D Demonstration

Supply Voltage	3.3V
Technology	0.35µm CMOS & MCM-D
Data Rate	2.5Gb/s/channel
Interconnect Length	5.6cm
Power Dissipation (TX)	10.3mW
Power Dissipation (RX)	15.0mW
Bit Error Rate (BER)	Better than 10^{-12}

Conclusions

Though similar "capacitively coupled interconnect" schemes have been presented, they lack a solution for providing robust power and ground distribution that is also compatible with current manufacturing methods. This technology demonstrates a complete solution for high-density, high-speed I/O and high-density, low inductance power and ground distribution by using buried solder bumps and ACCI. It also has the potential to improve yield during packaging and assembly since I/O channels are no longer dependent on the yield of a single solder bump.

Measurements and simulation have demonstrated that ACCI is robust to capacitor value and transmission line length variations, while capable of 6Gb/s/channel using a 0.18µm CMOS process. ACCI using buried bumps, with an inter-chip/package capacitor created upon the assembly of a module, was also demonstrated at 2.5Gb/s/channel using a 0.35µm CMOS process.

The main challenges to demonstrating ACCI on laminated organic packages are the resulting gap of the assembled system, and the co-planarity of the die and package. Methods for controlling the gap and planarity of the package are being considered, and high-k deposited underfills using nano-composites are being developed to mitigate the issue. To create a technology that is compatible with current processing, careful consideration must be given to thermal budgets and manufacturing flows.

Acknowledgments

This work was supported by AFRL contract F29601-03-3-0135, SRC task 1094, and NSF under grant CCR-0219567. The authors would like thank Liang Zhang and Steve Lipa for their valuable discussions on this work. We would also like to thank Jay Diepenbrock of IBM's Integrated Supply Chain for the use of IBM's test equipment.

References

1. S. Mick, L. Luo, J. Wilson, and P. Franzon, "Buried solder bump connections for high-density capacitive coupling" IEEE Electrical Performance of Electronic Packaging, Oct. 2002, pp. 205-208.
2. L. Luo, J. Wilson, S. Mick, J. Xu, L. Zhang, and P. Franzon, "3Gb/s AC-Coupled Chip-to-Chip Communication using a Low-Swing Pulse Receiver," *ISSCC Dig. Tech. Papers*, pp. 522-523, Feb. 2005.
3. R. Drost, R. Hopkins, R. Ho, and I. Sutherland, "Proximity Communication," JSSC *Vol. 39, No. 9, Sept. 2004,* pp: 1529-1535.
4. K. Kanda, D. D. Antono, K. Ishida, H. Kawaguchi, T. Kuroda, and T. Sakurai, "A 1.27Gb/s/pin 3mW/pin Wireless Superconnect (WSC) Interface Scheme," *ISSCC Dig. Tech. Papers*, pp. 142-143, Feb. 2004.
5. J. Wilson, J. Xu, S. Mick, L. Luo, S. Bonafede, A. Huffman, R. LaBennett, P. Franzon, "*Fully Integrated AC Coupled Interconnect using Buried Bumps",* IEEE, Electrical Performance of Electronic Packaging, Austin, TX, pp. 7-10, Oct. 2005.
6. T. Kim, J. Nath, J. Wilson**,** S. Mick, P. Franzon, M. Steer, A. Kingon, *"A high K nanocomposite for high density chip-to-package interconnections",* MRS Symposium Proceedings, Materials, Integration & Packaging Issues for High- Frequency Devices II, Vol. 833, pp. 201-206, 2005.
7. http://www.endicottinterconnect.com/, HyperBGA Package, Endicott Interconnect Tech., Endicott, NY.
8. International Road Map for Semiconductors 2005 Edition, Assembly and Packaging, page 5.
9. Rao R. Tummala, Fundamentals of Microsystems Packaging, McGraw-Hill, page 391.