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Developing Improved IO Buffer Behavioral Modeling Methodology Based on IBIS

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Abstract:

A new macromodeling methodology based on IBIS (Input/Output Buffer Information Specification) models is proposed. IBIS models are known to lack information regarding power and ground bounce [2][5] resulting in incorrect system level simulations. The new macromodel works with available simulators and produces models that can be simulated accurately for Simultaneous Switching Noise (SSN). To demonstrate the solution, a CMOS voltage-mode driver circuit and a MICRON DDR2 driver are simulated using HSPICE and compared with equivalent circuits created with IBIS models of the same drivers.

1. Introduction

IBIS models are the most common way of representing behavior of an IO driver. They are used in lieu of SPICE models that contain low level circuit details of the buffer. Creating IBIS models is easy and efficient but as driver technology is advancing and complexity of the IO circuits are increasing, IBIS is proving to be lacking in areas of simultaneous switching noise (SSN) [2] and representing advanced features (such as pre-emphasis and de-emphasis.)

Misrepresentation of noise might result in overestimation of signal strength and quality resulting in huge bit error rate (BER) and poor signal to noise ratio (SNR) at the receiver end. IBIS signal overshoots quite considerably but at the same time, in some voltage conditions, the output voltage under predicts the noise on the quiet line as well as the power and ground plane [2].

The lack of any noise information in IBIS models is mainly due to 2 known reasons.

1) **Lack of pre-driver and crossbar currents.** IBIS models do not include information on the currents that flow in the pre-driver or other currents that flow in a normal transistor level circuits such as crossbar (leakage) current or termination current [5], affecting the noise performance of the IBIS model.
2) **Gate Modulation effect.** IBIS models rely on V-I tables to get the values of the current sources in the driver. These tables are obtained for a fixed value of V_{gs} and the drivers rely on these recorded values, even when the actual V_{gs} changes.

We have identified a new approach that addresses the first issue above without the need of changing anything in the simulator. The solution will allow for the behavior model to perform simultaneous switching noise simulations.

A general introduction to the macromodel is given in section 2. A new method of accommodating SSN information in circuits that use IBIS models is presented in section 3. Section 4 includes results of simulation of the new technique on voltage mode drivers. Section 5 discusses future direction of research and concludes the paper.

2. IBIS Macromodel

Fig. 1 (left) below shows the basic components of the black box that is proposed to be used with the basic IBIS model. Fig. 1 (right) shows the high level system view of the setup. The main components of the black box are the voltage controlled current source (VCCS) and the power network model of the driver. Both these components could be integrated with the basic IBIS model creation using s2ibis3 [1]. The automatic creation of the black box would remove any user inconsistency and will produce network independent, highly accurate macromodels based on the basic IBIS models.

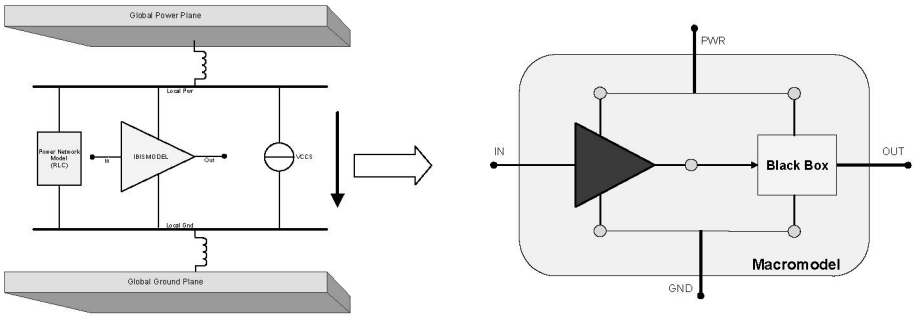


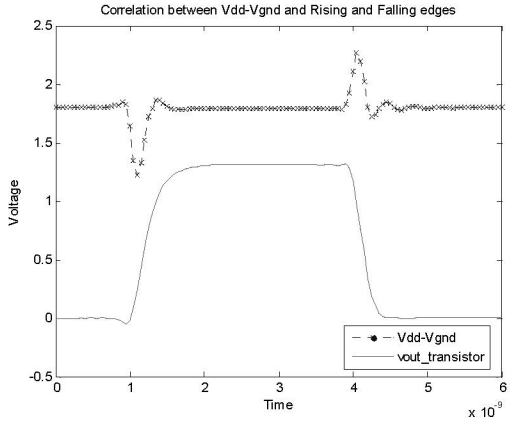
Figure 1:(left): Breakdown of various components of the proposed macromodel,(right): High level overview of the macromodel with the IBIS element and the black box.

3. Approach

Previous solutions have struggled to address the problem of insufficient representation of the extra current in IBIS model and have proposed methodologies that have extracted the signatures of the missing current at the VDD node - but have demonstrated the usefulness in a restricted environment [5]. These current signatures are obtained at a certain power/ground voltage. However, with varying voltage at the power and ground rails, current signature would change, thus rendering the correction inaccurate. Our macromodeling methodology, which we describe in this paper, allows for a more robust solution where the correction is a function of the variation in the voltage levels at the power and ground pins – thus useful even when the supply rails are affected by SSN.

The crossbar current along with all the other currents that is absent from the IBIS model can be estimated by comparing 2 similar circuits - one with IBIS model and the other with its equivalent transistor model. The difference current is then compared to the difference in the voltage levels between the V_{dd} and V_{gnd} ($V_{diff} = V_{dd}-V_{gnd}$). It is observed that this difference in voltage level only occurs during a transition in the voltage level at the buffer output (fig 2). As the buffer switches, it draws (or sinks) current from or to the power supply. Fast changing current passing through the package parasitics generate a drop in the power signal and a bounce in the ground signal [3][4]. When the difference current at the V_{dd} pin (I_{diff}) is compared against V_{diff}, a correlation is observed (fig 3) between the difference in current values of the transistor level model and the behavioral (IBIS) model and the difference of voltage levels in the power and ground pins – ie:

$$I_{diff} = I_{transistor} - I_{ibis} = f(V_{dd} - V_{gnd})$$



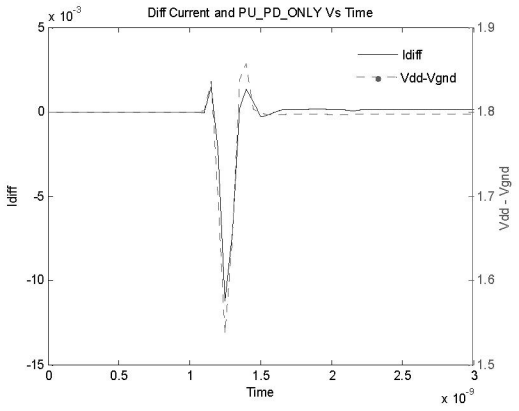
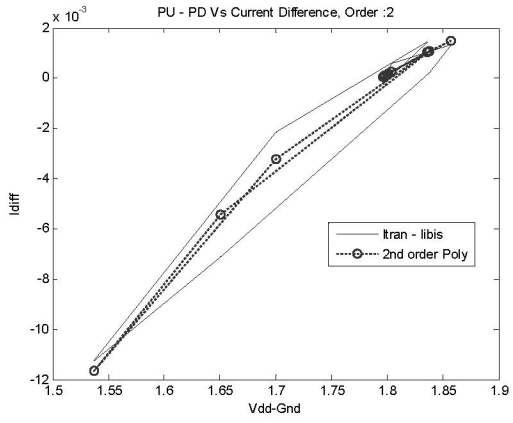


Figure 2 (left): Power droop and ground bounce correlate with the switching of the buffer

Figure 3 (right): Comparing I_{diff} and V_{diff} together. There is a high correlation between the difference in current between the transistor level model and the behavioral (IBIS) model and the difference of voltage levels in the power and ground pins

The correlation is captured in an n^{th} order polynomial (fig. 4) that can be used to recreate the difference in current. Once polynomials for the rising and falling curves are obtained, the extra current that needs to be injected in the IBIS model is done using Voltage Controlled Current Sources (VCCS).

Fig. 5 compares the recreated difference current using the polynomial with the original. It can be observed that the current function generates very accurate difference current.



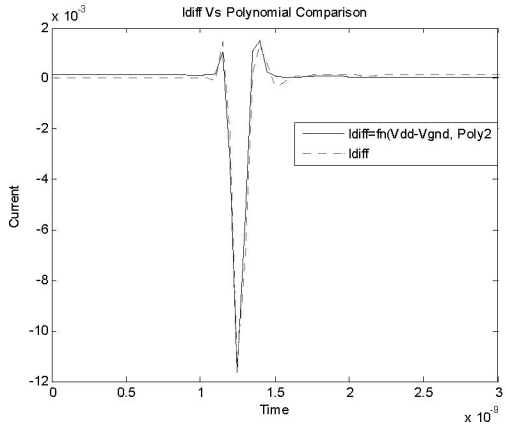
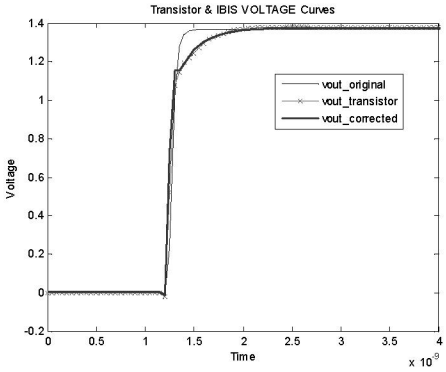


Figure 4 (left): The correlation in fig.3 is captured in a 2nd order polynomial that can be used to recreate the difference in current.

Figure 5 (right): This figure shows the comparison between the curves obtained using the polynomial and the actual current curve of the rising waveform of a sample driver.

As can be seen in fig 6 below, there is almost a 50% improvement in the simulation accuracy. The improvement is judged throughout this paper using an integrated voltage difference method where area under the error curve is measured when plain IBIS (shown by 'original' in the figures) and corrected IBIS (shown by 'corrected' in the figures) are compared with the transistor level driver. These tests were performed on a simple CMOS voltage mode driver [2] and verified on a more complicated 512MB DDR2 driver (part no.

MT47H128M4BT-5E) from Micron Inc. All the steps needed to obtain the polynomial for the VCCS are automated using MATLAB and can be integrated to a macromodel tool such as the North Carolina State University's S2IBIS3[1]. These polynomials can be generated along with the IBIS model by the model maker and once accuracy tests are performed, could be shipped with the IBIS models as a black box as described in section 2.



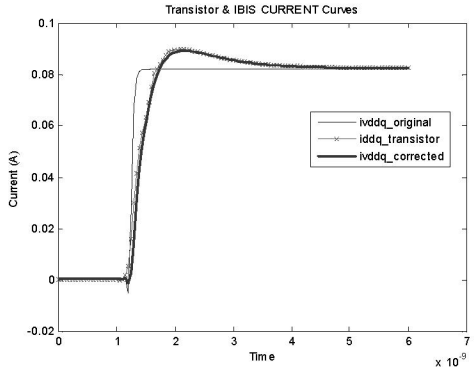
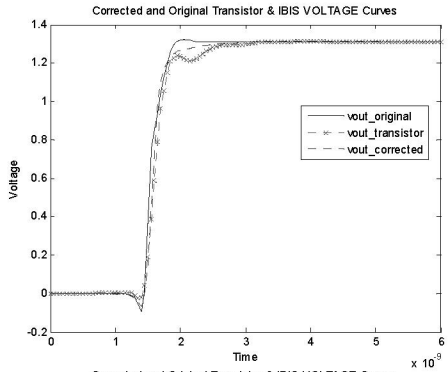


Figure 6 (left): Rising waveform voltage at the output pin before and after correction compared to the transistor level circuit.

Figure 7 (right): Rising waveform current at the output pin before and after the correction compared to the transistor level circuit. These tests were performed using simple voltage mode drivers with 3 switching simultaneously and 1 quiet.

4. Simulation Results

This method was tested on a real life DDR2 voltage mode driver from Micron Inc. Initially, rising and falling waveforms were tested as shown in the output voltage (fig 8 and fig 10) and the current at the Vdd pin (fig 9 and fig 11). Once rising and falling edges were tested separately, this method was tested for a pulse. Tests were done with lumped elements modeling the power and ground parasitics in 2 different combinations. In the first case, the inductance (which is the primary cause of SSN [4] and is used here to model it) was placed only on the power pin (as described in [5]) while in the second instance, both the power and ground pins were connected to inductance (as described in [2]). In the second instance, only self inductance was used and mutual inductance was ignored with the assumption that the result in all the three cases (original IBIS, corrected IBIS and SPICE), even without mutual inductance, should produce similar results.



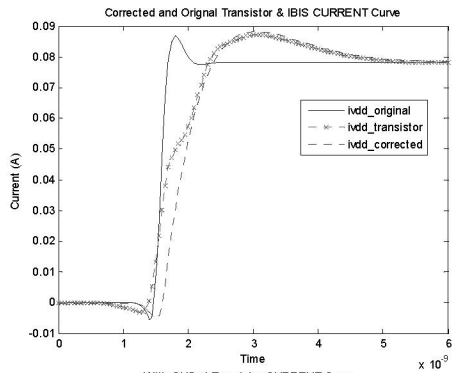
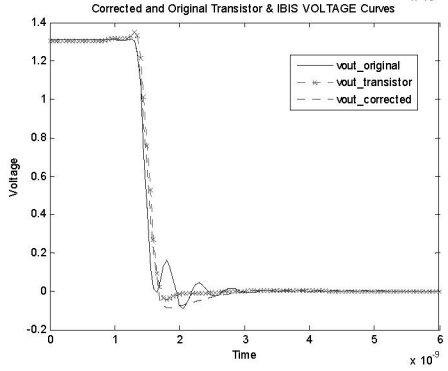


Figure 8 (left): Rising voltage waveform at the output pin of the DDR2 Micron driver. The three curves shown are the original IBIS curve (solid), the corrected curve (broken) and the transistor level curve (broken with X)

Figure 9 (right): Rising current waveform at the Vdd pin with the 3 different curves as described above.



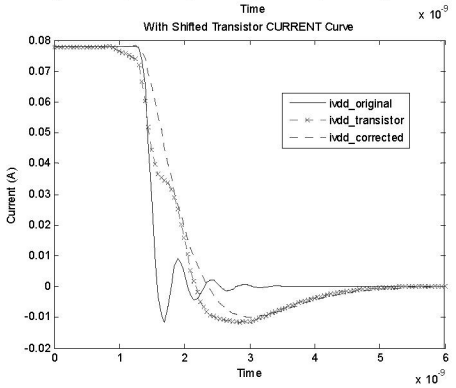


Figure 10 (left): Falling voltage waveform at the output pin of the DDR2 Micron driver. The three curves shown are the original IBIS curve (solid), the corrected curve (broken) and the transistor level curve (broken with X)

Figure 11 (right): Falling current waveform at the Vdd pin with the 3 different curves as described above.

The above tests were performed with 3 drivers switching simultaneously and 1 quite driver. Decoupling capacitors are also used as a part of the solution to improve SSN response of the IBIS models. Fig 12 shows the output voltage of the original IBIS, corrected IBIS and transistor level circuit of the DDR2 voltage mode driver. An improvement of nearly 28% over the plain IBIS model is observed. Figure 13 shows the current at the Vdd pin.

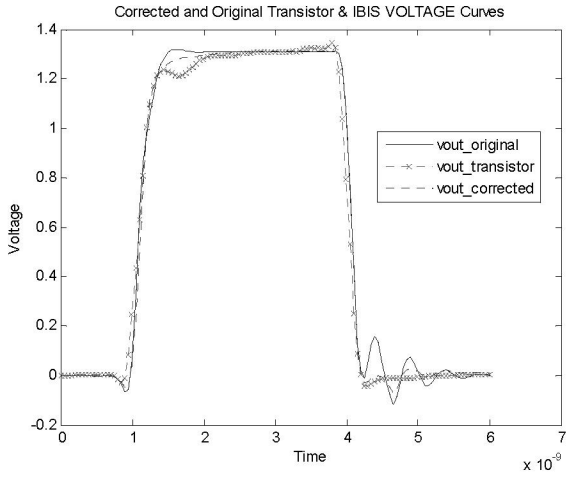


Figure 12: Output Voltage of the DDR2 Micron driver with the original IBIS, corrected IBIS and the transistor level curves.

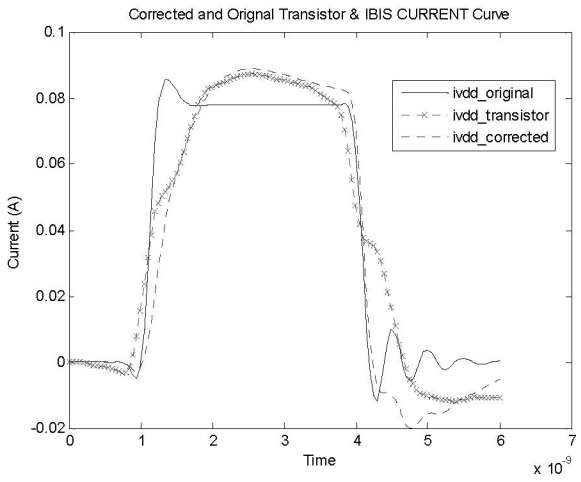


Figure 13: Vdd Current of the DDR2 Micron driver with the original IBIS, corrected IBIS and the transistor level curves.

Table 1 shows the percent improvement in the DDR2 driver when this method is applied to simulation setup with parasitics only of power pin (case 1) and parasitics on power and ground pin (case 2). The improvement is judged by calculating the area under the error curve when comparing plain IBIS and corrected IBIS with the transistor level driver.

	DDR2 Voltage Mode (MICRON)		
	Rising	Falling	Pulse
Case 1	57.4828	55.5063	22.9584
Case 2	34.9291	38.2169	27.66

Table 1: Percentage improvement of the macromodel over plain IBIS when compared with the transistor level curve. 2 cases were investigated, case 1 had lumped elements modeling the parasitics at the power pin only while in case 2, parasitics were present on power as well as ground pin. Tests were done on a voltage mode DDR2 driver from Micron Inc.

5. Conclusion

As shown in this paper, an IBIS model can be complemented by a black box that primarily injects currents in the power/ground rails to produce more accurate results. On an average, the simulation accuracy of circuits with the black box improves by around 25% when compared with HSPICE circuits over circuits without the black box.

We have demonstrated a system that would create accurate models that are not only good standalone but are equally useful in a large network that has multiple drivers switching simultaneously along with all the other parasitics involved.

References

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