Deterministic Nanowire Fanout and Interconnect Without Any Critical Translational Alignment

Neil H. Di Spigna, *Student Member, IEEE*, David P. Nackashi, Christian J. Amsinck, *Student Member, IEEE*, Sachin R. Sonkusale, *Student Member, IEEE*, and Paul D. Franzon, *Fellow, IEEE*

***Abstract*—Interfacing the nanoworld with the microworld represents a critical challenge to fully integrated nanosystems. Solutions to this problem have generally required either nanoprecision alignment or stochastic assembly. A design is presented that allows complete and deterministic fanout of regular arrays of wires from the nano- to the microworld without the need for any critical translational alignment steps. For example, deterministically connecting 10-nm wires directly to 3-μm wires would require a translational alignment to within only about 6 μm. The design also allows for nanowire interconnect and is independent of the technology used to fabricate the nanowires, enabling technologies for which alignment remains very challenging. The impact of potential fabrication errors is analyzed and a structure is fabricated that demonstrates the feasibility of such a design.**

***Index Terms*—Alignment, crossbar architectures, fanout, interconnect, nanoscale interfacing, nanotechnology.**

I. Introduction

THE ABILITY TO fabricate wires at a nanoscale pitch has advanced tremendously in recent years. Whether through photolithography, electron and ion beam lithography, scanning probe lithography, edge-based lithography, nanoimprint lithography, or self-assembly, wire pitches at the nanoscale have been demonstrated [1]–[9]. One challenge that still remains is connecting to these nanowires. Physically interfacing the nanoworld with the microworld presents a critical challenge for testing, nanocomputing, and fully integrated nanosystems [4], [10], [11]. Successful interface strategies require physical connection to the nanoworld without compromising functional density. This typically requires both limiting the frequency of this interface as well as connecting a large set of nanowires with a smaller set of microwires [12].

Several innovative techniques have been proposed as potential solutions to this challenge. Zhong *et al.* have demonstrated an approach based on chemically modified crosspoints in a nanowire FET crossbar architecture to achieve decoded nanowire addressing [10]. Ziegler and Stan have proposed a crossbar architecture in which nanowires and microwires are separately etched [13]. DeHon has proposed the use of nanoscale vias combined with customizable nano-via decoding patterns [11]. Alternatively, in hopes of avoiding lithographic processes to pattern nanoscale features, DeHon *et al.* have proposed a stochastic architecture in which controlled doping profiles of silicon nanowire FETs are used for addressing [14]. Another stochastic approach would be Williams and Kuekes' proposed random assembly of functionalized gold particles in between micro- and nanowires, followed by discovery of the existing address space [15]. Generally, these solutions have required either nanoprecision alignment, which remains very challenging, or stochastic assembly, which can result in incomplete connectivity.

In this paper, a simple approach is presented that permits fully deterministic cross connect of orthogonal wiring arrays without the need for nanoprecision alignment. It is independent of the technology used to fabricate the nanowires, enabling interconnect and fanout for technologies in which alignment remains very challenging, such as in nanoimprint lithography [16], [17]. The design exploits the system geometry, particularly angles, to solve the problem of pitch reduction, a common theme of several approaches [13], [18]. However, no restrictions are placed on the minimum size of the nanowire pitch. Rather than mask alignment precision, the challenge of pitch reduction is shifted to the ability to fabricate structures at the micrometer scale. In addition, the process is relatively simple and is presented from a fabrication perspective, critically addressing the effect of potential processing errors on the structure. A demonstration of this concept has been fabricated and characterized.

II. Theory

A. Design and Novelty

The basic process flow, shown in Fig. 1, begins with fabrication of the nanowire array at a target spacing and wire width s_1 and w_1, respectively. The wires are then covered with a thin insulator. A cut is made in the insulator at a target angle to the nanowires, ϕ, and with a target cut width w_c. Finally, perpendicular connecting wires are fabricated at a target spacing and wire width s_2 and w_2, respectively. Ideally, each nanowire is connected to exactly one connecting wire.

The novelty of this design is that there exists a set of values for the physical dimensions of the system such that the two orthogonal wire arrays can connect without any critical x–y alignment, as demonstrated in Fig. 2. In this example, the connecting wires are increasingly "misaligned" in the horizontal direction. The first system depicts a configuration in which microwire m_1 connects nanowire n_1, m_2 connects n_2, and m_3 connects n_3. As shown in the second system, a slight misalignment of the microwires has no affect on the connectivity of the system. In the

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The authors are with the Department of Electrical and Computer Engineering at North Carolina State University, Raleigh, NC 27695 USA (e-mail: nhdispig@ncsu.edu).

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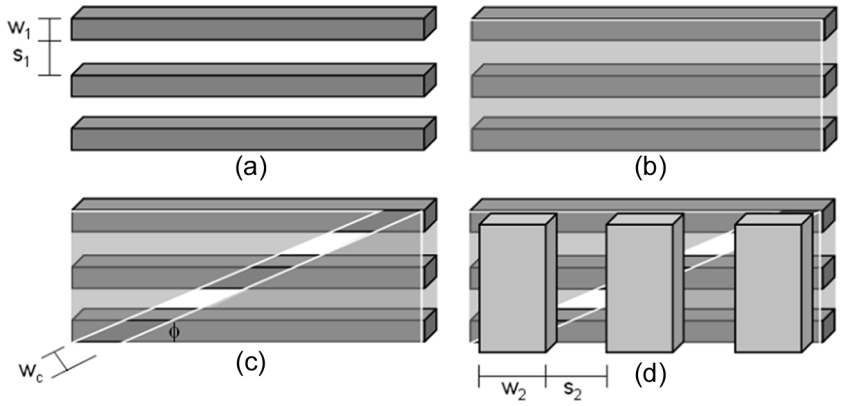

Fig. 1. Basic process flow: (a) fabricate nanowire array; (b) cover with insulator; (c) open cut in insulator; and (d) fabricate connecting wire array.

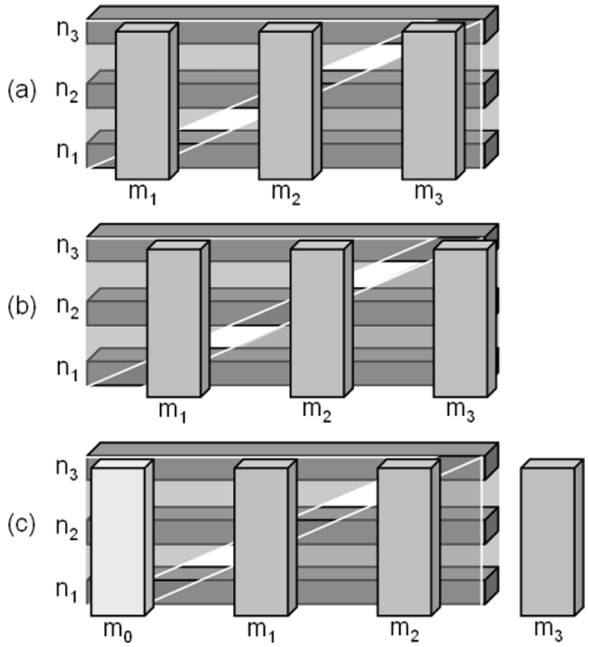

Fig. 2. Demonstration of novelty. As the connecting wires are increasingly "misaligned" from (a) to (c), the system remains one-to-one connected.

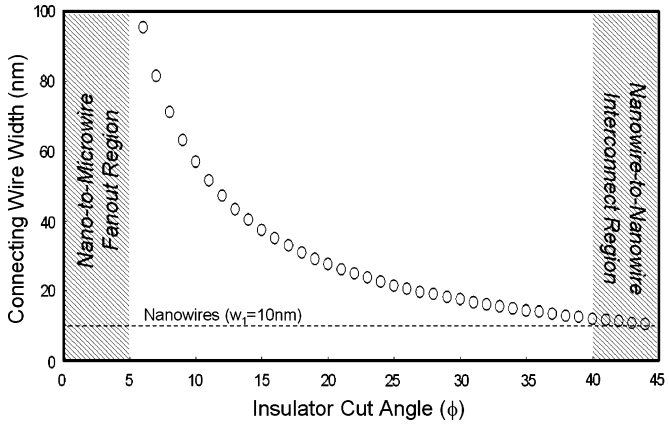

Fig. 3. Connecting wire width versus insulator cut angle (ϕ) for a nanowire width of 10 nm. The insulator cut angle is governed by the desired application.

final system, the wires are "misaligned" beyond a certain tolerable allowance, resulting in an alternate configuration in which an additional microwire m_0 connects n_1, m_1 now connects n_2, and m_2 now connects n_3. By padding with extra wires, e.g., m_0, complete connectivity can still be guaranteed despite any gross misalignment. Thus, complete cross connect of regular arrays of wires can be achieved without the limitation of any critical x–y alignment.

B. Unique Connectivity

Only systems whose geometry meets a certain set of criteria will be able to exploit the novelty of this design. The fundamental equation relating the two wire array pitches and the insulator cut angle is

$$\phi = \tan^{-1}\left(\frac{s_1 + w_1}{s_2 + w_2}\right). \tag{1}$$

Investigating the relationship between the size of the connecting wires and the insulator cut angle helps to illustrate the versatility of this structure. Fig. 3 depicts this relationship for an assumed nanowire width of 10 nm. Choosing the appropriate insulator cut angle depends upon the desired connecting wire width. To fan out from 10-nm wires to wires greater than 100 nm in width, cut angles less than 5° would be necessary. Alternatively, at a cut angle of 45°, the two sets of wires would have equivalent dimensions and nanowire interconnect is achieved. Thus, the desired application of this design governs the choice of the cut angle. It is important to note that as the connecting wire width increases, the nanowires must run defect free over relatively longer distances. Thus, there exists a tradeoff between full fanout and the ability to fabricate long nanowire arrays. Hierarchical application of this technique is one way to balance this tradeoff.

Guaranteeing one-to-one connectivity introduces two additional criteria: to avoid shorts, no connecting wire can contact multiple nanowires, and to avoid opens, each connecting wire has to contact at least one nanowire. From these requirements, the optimal connecting wire dimensions necessary to guarantee unique connectivity are derived

$$s_{2\_opt} = \frac{w_c}{\sin\phi} + \frac{w_1}{\tan\phi}, \quad w_{2\_opt} = \frac{s_1}{\tan\phi} - \frac{w_c}{\sin\phi}. \tag{2}$$

C. Deterministic Connectivity

Fabricating the optimal dimensions guarantees that the system will be uniquely connected, but there is no guarantee on what that connectivity will be. In fact, in the example given to demonstrate the novelty of this design, the connectivity of the system changed after a certain "tolerable allowance" in the alignment. Microwire (m_i) no longer connected nanowire (n_i), but rather nanowire (n_{i+1}). This is adequate for applications that simply require complete connectivity, or for those in which the resulting connectivity can be discovered postfabrication or reconfigured, but *not* for applications in which a predetermined connectivity is required. Deriving this alignment tolerance, given below for both the cut and connecting wires, is essential to establishing the alignment boundaries of the target connectivity.

$$\text{Cut\_Align\_Tol} = s_1 + s_2 \tan\phi - \frac{w_c}{\cos\phi} \tag{3}$$

$$\text{ConnectingWire\_Align\_Tol} = \frac{s_1}{\tan\phi} + s_2 - \frac{w_c}{\sin\phi}. \tag{4}$$

These two variables form an alignment window that dictates the connectivity of the system. Targeting the center of this window will result in the maximum contact area between the connecting wires and the nanowires. The cut alignment tolerance represents the maximum vertical offset of the cut before connecting wire (m_i) would connect to nanowire $(n_{i\pm1})$ rather than nanowire (n_i). Fortunately, as long as the cut is made to intersect each of the nanowires, any misalignment in the cut can be compensated for during alignment of the connecting wires. This effectively eliminates any critical restriction on the cut alignment.

The connecting wire alignment tolerance represents the maximum horizontal offset before connecting wire (m_i) would connect nanowire $(n_{i\pm1})$. Its impact is significantly different depending upon the application of the structure: fanout from the nano- to the microworld $(\phi < 5^\circ)$ or nanowire interconnect $(\phi \approx 45^\circ)$. The allowable tolerance is very small for nanowire interconnect applications, suggesting that predetermined connectivity may not be achievable, but complete connectivity can still be obtained through the padding of additional wires. Alternatively, the connecting wire alignment tolerance becomes very large for fanout applications and is generally on the order of the connecting wire pitch, $s_2 + w_2$. This implies that connecting micrometer-scale wires to target nanowires requires only a micrometer-scale precision alignment. For example, connecting 10-nm wires directly to 3-μm wires separated by about 3 μm would only require translational alignment precision to within about 6 μm. Thus, for fanout applications, it is possible to guarantee both complete *and* deterministic connectivity. This represents another significant feature of this design: that "nano-alignment" can be achieved at the micrometer scale.

D. Effects of Potential Fabrication Errors

In practice, the fabricated connecting wire dimensions will be different than the targeted optimal dimensions due to processing issues such as etch or develop biases. This will not impact the total connecting wire pitch $(s_2 + w_2)$, but it will change the distribution of that pitch into the spacing and wire width. When w_2 is fabricated to the optimal dimension, the probability for either an open or a short is zero, thus the novelty of the design. If the connecting wires are fabricated thicker/thinner than targeted, then there exists some probability for a short/open, given below:

$$P_{\text{short}} = \begin{bmatrix} 0 & w_2 \le w_{2\_opt} & \frac{w_{2\_opt} - w_2}{s_2 + w_2} \\ \frac{-(w_{2\_opt} - w_2)}{s_2 + w_2} & w_2 > w_{2\_opt} & 0 \end{bmatrix} = P_{\text{open}}.$$

Now consider offsets in the cut width or in the nanowire dimensions, which would alter the target optimal dimensions of the connecting wires. These offsets can be compensated for during fabrication of the connecting wires simply by targeting the altered optimal dimensions.

The probability for a short or open derived above is dependent upon the alignment. Continuing with the working example, suppose that the target 3-μm connecting wires were actually fabricated to be 3.3 μm wide. This would result in a 5% chance of a system short. Fortunately, when fanning out from the nano- to the microworld, it was shown that the alignment tolerance is on the order of the connecting wire pitch. In this example, one would still have a 5.7-μm alignment window to avoid shorts. Thus, these errors have minimal impact on fanout applications, since the alignment tolerance is very large, and the percentage error would be relatively small. For nanowire interconnect applications, however, these probabilities could surface as yield hits.

Another potential fabrication error that must be considered is the effect of rotational misalignment on the system. Although any translational alignment is eliminated, rotational alignment of the insulator cut, Fig. 4(a), and the perpendicular connecting wires, Fig. 4(b), is still necessary.

The cut should be made at the angle ϕ derived in (1), and the connecting wires should be made perpendicular to the nanowires. To analyze the impact of deviation from these angles, the conditions in which a single open or short first occurs was derived for both rotational misalignments. Angular offset from the target cut angle is denoted by θ, whereas angular offset from perpendicular connecting wires is denoted by τ. A summary of the results can be seen in Fig. 5, which compares the rotational misalignment before a single open/short occurs for both θ and τ over various cut angles to achieve a desired system size. The system size is defined as the number of nano- to microwire connections. As expected, the rotational misalignment tolerance falls off with increasing system size. At smaller cut angles, there is significantly more tolerance for rotational misalignment of the connecting wires than there is for deviance from the cut angle. As one approaches nanowire interconnect applications $\phi = 45^\circ$, the two cases converge. Thus, the best case for rotational misalignment of the cut is only equal to the worst case for rotational misalignment of the connecting wires. This implies that the cut rotational alignment is more critical, and represents the greater limitation to the scalability of this structure for fanout applications. However, it is important to note that any rotational misalignment between the two sets of orthogonal wires can adversely impact pitch reduction interface

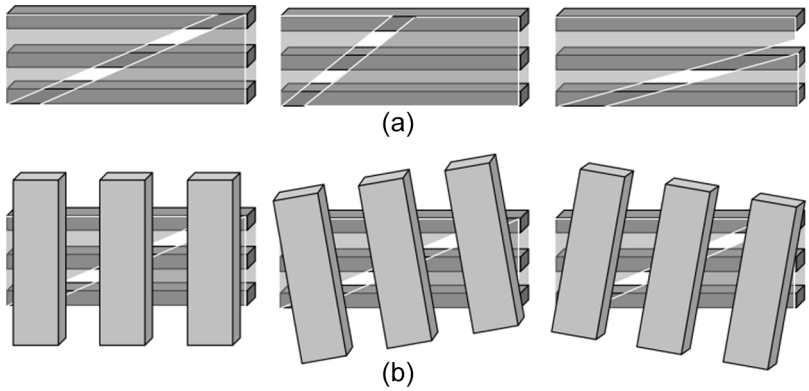

Fig. 4. Rotational misalignment of: (a) the insulator cut (offset from target cut angle is defined as θ) and (b) connecting wires (offset from orthogonality is defined as τ).

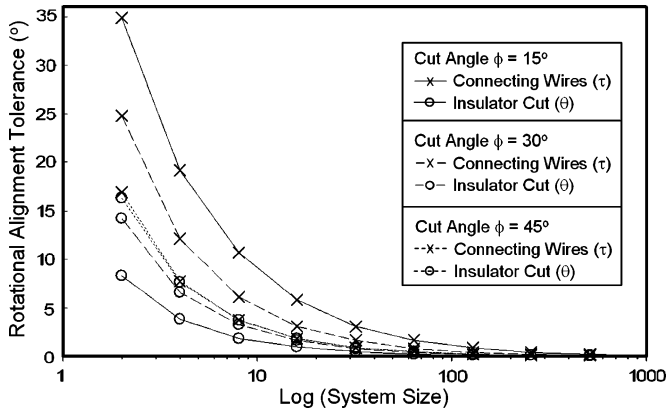

Fig. 5. Rotational alignment tolerance versus log (system size). This figure compares the tolerable rotational misalignment for both angular offset τ from the desired perpendicular orientation of the connecting wires, and angular offset θ from the target cut angle, ϕ for three different cut angles ranging from fanout to nanowire interconnect. The tolerance is defined as the maximum angular offset in which the first open/short occurs. As the number of nano- to microwire connections increases, the rotational alignment tolerance decreases.

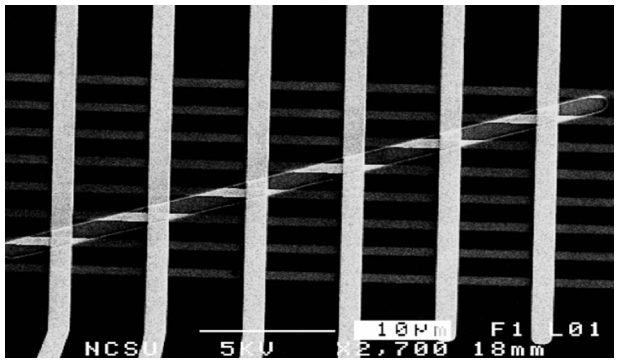

Fig. 6. Fabrication of proof-of-concept structure. This SEM shows that each vertical connecting wire connects one and only one horizontal "nanowire."

strategies. Fortunately, using alignment marks placed towards the edge of large wafers, relatively precise rotational alignment can be achieved.

III. Fabrication and Characterization

Structures demonstrating this concept were fabricated on top of a 1000-Å-thick silicon dioxide film, thermally grown on a $4''$ (100) p-type, 1–10 ohm-cm silicon wafer. An i-Line GCA 800 DSW wafer stepper was used to pattern 600-nm "nanowires." The wires were formed using a bilayer resist stack for liftoff patterning of a 350-Å layer of gold on top of a 50-Å adhesion layer of titanium. Honeywell Accuglass 111 Spin-On Glass was applied and then annealed at 300 °C to form a 1500-Å interlevel dielectric. The oxide cut was patterned, followed by an anisotropic reactive ion etch (RIE) of the underlying dielectric. Finally, the connecting wires were fabricated by depositing 75 Å of titanium and 925 Å of gold, once again patterned using a liftoff process. The structures yielded wafer scale, an example of which is shown in Fig. 6.

From this figure it is apparent that each connecting wire connects one and only one "nanowire." This is further evidenced by the current–voltage characteristics shown in Fig. 7. Target connections are made successfully while nontarget connections remain electrically isolated. Conductivity differences between the target connections are caused by the wire resistance of the "nanowires." Due to the angle of the cut, the connections to each "nanowire" are at different distances from the probe pads. Overall, each intended connection resulted in ohmic contact, while each unintended connection remained electrically isolated, successfully demonstrating the utility of this structure for fanout applications.

Scaling the "nanowires" into the nano regime should have no theoretical impact on the design, thus allowing 600-nm wires to be fabricated for the proof-of-concept structure. However, there are some practical issues that need to be considered as the nanowires are more aggressively scaled, the first of which is contact resistance. Clearly, the novelty of this design is such that a structure can result in which the connecting wires are only infinitesimally contacting the nanowires. This possibility is unavoidable, but as previously mentioned, it can be mitigated by targeting the center alignment, and thus the maximum contact area. In addition, ensuring that the insulator cut is completely opened is essential to reducing the contact resistance.

Another issue to consider when scaling to the nano regime is any nonuniformity in the nanowire width. Oftentimes nanowires are fabricated with some degree of width and spacing nonuniformity [19], [20]. It is unlikely that this will have any significant impact on the connectivity of the structure, causing only random individual shorts or opens. Any full-scale connectivity effects

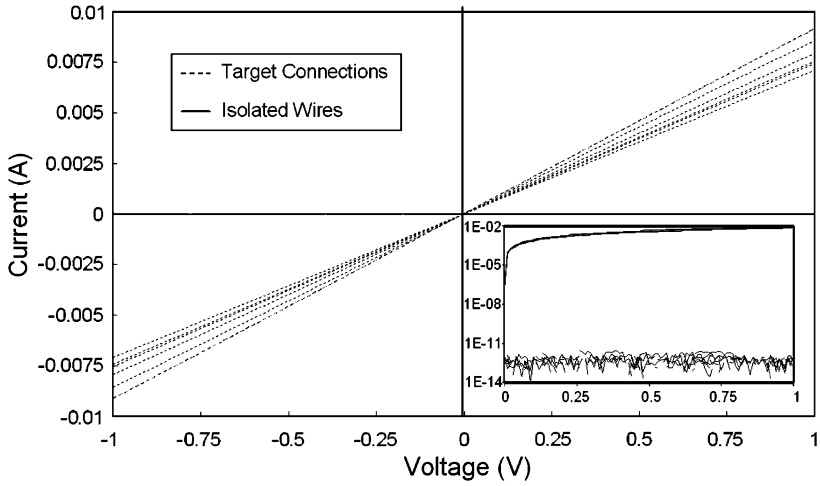

Fig. 7. Current–voltage characteristics. The target connections are made successfully while the nontarget connections remain electrically isolated.

can be modeled using the probability analysis for nontarget optimal dimensions considering the average deviation caused by the imperfections in the nanowire fabrication.

Finally, it was stated that successful interface strategies require both physical connection to the nanoworld and retention of functional density. This latter requirement can often involve connecting a larger set of nanowires with a smaller set of microwires. Although it is not the goal of this paper, there is nothing intrinsic about this design that would prevent some form of decoding. An extension of this technique using multiple cuts with active elements at the cross points could accomplish decoding. A simpler solution would be to separate the pitch reduction from the decoding and program the latter into the nanowire crossbar fabric, as previously suggested [13].

IV. Conclusion

A design was presented that allows complete and deterministic fanout from the nano- to the microworld without the need for any critical translational alignment. Deterministically connecting microwires to nanowires requires only a micrometer-scale alignment. The effects of potential fabrication errors were analyzed and offsets from the optimal dimensions were shown to have minimal impact on fanout applications, although such errors could surface as yield hits for nanowire interconnect applications. Rotational misalignment of the cut was shown to be the ultimate limitation to the scalability of this design. A proof-of-concept structure was fabricated and characterized, showing the feasibility of this design for fanout and interconnect applications, and practical issues involved with further scaling of the design were addressed.

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Neil H. Di Spigna (S'02) received the B.S. degree majoring in applied physics, computer science and mathematics from the State University of New York, Geneseo, in 1999, the M.S. degree in electrical and computer engineering from Duke University, Durham, NC, in 2001 and the Ph.D. degree in electrical engineering from North Carolina State University, Raleigh, in 2006.

His research is in the area of molecular electronics, nonvolatile memory, and nano-interconnect structures.

David P. Nackashi received the B.S. degree in electrical engineering from the Georgia Institute of Technology, Atlanta, in 1993 and the M.S. degree in computer engineering and the Ph.D. degree in electrical engineering from North Carolina State University, Raleigh, in 1999 and 2004, respectively.

Before his graduate studies, he worked at Alcatel Telecom, Raleigh, on the development of an OC-48 SONET Multiplexer. He is currently a cofounder of a startup that designs and manufactures advanced support films for electron microscopy for both materials and life science applications.

Christian J. Amsinck (S'01) received the B.S and M.S. degrees in computer engineering from North Carolina State University, Raleigh, in 2000 and 2001, respectively. He is currently working toward the Ph.D. degree in computer engineering at North Carolina State University; his research area is in molecular electronics.

Mr. Amsinck received the departmental outstanding computer engineering graduate award in 2000, and is a member of Phi Kappa Phi.

Sachin R. Sonkusale (S'04) received the B.Tech degree in electrical engineering from Indian Institute of Technology, Kanpur, in 2000 and the M.S. degree in electrical engineering from North Carolina State University, Raleigh, in 2002. He is currently working toward the Ph.D. degree in electrical engineering at North Carolina State University, working in the field of nanofabrication of nanowires and nanostructures.

Paul D. Franzon (S'85–M'88–SM'99–F'06) received the Ph.D. degree from the University of Adelaide, Adelaide, Australia, in 1988.

He is currently an Alumni Distinguished Professor at North Carolina State University, Raleigh. He has also worked at AT&T Bell Laboratories, DSTO Australia, Australia Telecom, and Communica Ltd. His current interests center on the technology and design of complex systems incorporating VLSI, MEMS, advanced packaging, and molecular computing. Application areas currently being explored include novel advanced packaging structures, network processors, SOI baseband radio circuit design for deep space, on-chip inductor and inductance issues, RF MEMS, and moleware circuits and characterization. He has led several major efforts and published over 120 papers in these areas.

Dr. Franzon received the NSF Young Investigators Award in 1993 and was selected to join the North Carolina State University Academy of Outstanding Teachers in 2001.