Controlled nanowire fabrication by PEDAL process

Sachin Sonkusale
ECE Department
North Carolina State University
Raleigh, North Carolina, USA
srsonkus@ncsu.edu

Dr. Paul Franzon
ECE department
North Carolina State University
Raleigh, North Carolina, USA
paulf@ncsu.edu

***Abstract*—In earlier publications [1,2] we proposed and successfully demonstrated an unconventional lithographic technique called PEDAL process (Planar Edge Defined Alternate Layer) to define wafer scale sub 25 nm nanowires and nanoimprint template. In this publication, uniformity analysis of the width and spacing of an array of sixteen line-width structures with approximately 42 nm pitch and twenty four line-width structures with approximately 23 nm pitch, fabricated by PEDAL process, is presented. Results on routing capability of this process along with results of palladium nanowires obtained by PEDAL lift-off process done on the template with 42 nm pitch is also reported. In the case of template with array of sixteen lines, the average pitch of array across the 4 inch wafer was measured to be 40. 83 nm with the standard deviation of 2.29 nm where as the average pitch of the lines in an array was found to be 41.5 nm with the standard deviation of 4.64 nm. After Pd lift-off the average pitch in nanowire array was measured to be 41.88 nm with standard deviation of 1.83 nm, close to the values obtained for the template. In the case of array of twenty four line-widths, average pitch of array across the 4 inch wafer was measured to be 21.1 nm with the standard deviation of 5 A where as the average pitch of the line in an array was found to be 22.6 nm with the standard deviation of 9 A. The experimental results presented in this paper prove the efficacy of PEDAL process in making nanowire template of sub-25 nm wide lines with good routing capability.**

Keywords-PEDAL, nanoimprint, mold, nanowires, palladium, unifromity

I. INTRODUCTION

Nanoscience and nanotechnology cover many different areas, but one key set of methods for both is nanofabrication. As defined by the US national science foundation ,"nanofabrication is the process of making functional structures with arbitrary patterns having minimum dimensions currently defined to be less than 100 nm". The development of microelectronic circuits with less than 100-nm-scale features is proceeding rapidly by extensions of existing, conventional photolithographic techniques. Nanofabrication has applications not only in semiconductor devices and integrated circuits but also in widely different areas such as biology, materials science, and optics. There are many opportunities of cost-effective unconventional nanofabrication techniques for fabricating simple patterns like arrays of lines and dots in various areas including (i) chemical and biological sensors (ii) Chemical catalysts (iii) High frequency filters and resonators (iv)Data storing device (v) Printed, low-cost organic microelectronics; (vi) nanofluidics and (vii) nanoelectrical mechanical systems (NEMS). One approach to fabricate nanoscale features is to modify and etch the patterns on the resist layer, by exposing it to light or scanning electron beam through a mask, or by maskless lithography which includes direct writing using electron beam and focused ion beam. Extending photolithography beyond the wavelength of 157 nm faces significant issues in terms of availability of light sources, optics, masks and need of new photoresist material. Lithographic techniques using extreme UV, X-ray, electron beams, and ion-beams, are growing in importance. High per capita and operating costs and limited availability have restricted the use of these techniques to semiconductor IC industry. Another approach of nanofabrication, the so called unconventional techniques, utilizes the interaction between molecules or colloidal particles to assemble these particles into two dimensional or three dimensional structures. The unconventional techniques, include embossing [3,4], printing [5-8], scanning probe lithography [9-15], molding [16,17], edge defined lithography [18-26], and self-assembly [27-30]. The development in some unconventional lithographic tools, like molding, dip pen and nanoimprint have reached the level of commercial production. These techniques provide the high-yield low cost nanofabrication on non-planar surface and over large areas, an alternative to high-cost and low yield conventional lithographic processes. One method of unconventional patterning is to replicate nanoscale patterns or masters on organic soft layer. These patterns are transferred into materials by molding, embossing, or printing and these technique have demonstrated their ability to make nano size features repeatedly on the large surface area and seems promising candidates of nanofabrication. The other method of nanofabrication uses scanning probe to write nanofeatures by organic material with nanoscale resolution [9,13,15,31-33]. Edge lithography and self-assembly, other unconventional nanofabrication techniques, are more limited in terms of the patterns they can generate, but are very promising approaches towards low-cost fabrication of regular arrays of nanostructures. In most of the unconventional techniques, initial mold or template making still depends on the conventional techniques like lithography and the cost of one 100 mm mold with sub-50 nm size features can be over million dollars. Low cost, high yield methods are needed to reduce the overall fabrication cost of simple nanostructures. Currently, ebeam lithography, Nanoimprint lithography, step and flash lithography and immersion lithography seems to be

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the promising candidate for making sub-25 nm nanowires. In our previous work [1, 2] we demonstrated a reliable and cost-effective process for making wafer scale sub-25 nm nanowires and nanoimprint molds. The PEDAL technique, although limited to making linear structures, has applications in fabricating high density chemical and biological sensors, crossbar memory structures and high frequency filters and resonators. In this publication a detailed analysis of quality of nanoimprint molds obtained by PEDAL technique and Palladium nanowires obtained by PEDAL lift-off technique has been presented.

II. Overview of Concept

PEDAL process involves defining the path and location of nanowires by etching a trench directly in silicon wafer, or in the layer deposited on the silicon wafer. As shown in fig. 1(a), a trench is etched into silicon wafer by anisotropic etch. After defining the trench, a buffer layer of a-silicon is deposited on the trench {figure 1b} followed by conformal deposition of alternate layers of silicon nitride and amorphous silicon {fig. 1c}. Width of lines and spaces is decided by the thickness of the deposited thin films and number of depositions decides number of lines and spaces in an array. To planarize the topography of trench a thick layer of a-silicon is deposited for filling the trench followed by spin coating of a polymer {fig. 1d}. The stack of polymer, a-silicon and silicon nitride is planarized down to the required depth {figure 1e} using single etch process which is nonselective to silicon nitride, amorphous silicon and polymer or using combination of etch processes, involving a process which is nonselective to polymer and amorphous silicon to etch to level A and other etch process nonselective to silicon nitride and amorphous silicon to etch to level B {figure 1d}. The lines and spaces are revealed by selectively etching a-silicon material {figure 1f}. This gives a template with silicon nitride lines which can be used for nano-imprinting. Nanowires can be directly patterned on the template by using the lift-off process. In this process lines and spaces are revealed by selectively etching silicon nitride {figure 1g} followed by e-beam evaporation of metal on the wafer {figure 1h} and lift-off of the metal by etching a-silicon {figure 1i}. This gives us metal nanowires on insulting silicon nitride layer. Various modifications of the PEDAL process discussed above are possible to give the desired end results; however, the basic method of defining lines and spaces remains the same.

III. PEDAL-Pros and Cons

Advantages of PEDAL process:

1. PEDAL is a wafer-scale process to define sub-25 nm array of aligned nanowires and nanowire template i.e. instead of writing one nanowire at a time (e-beam serial writing lithography) or making one die at a time (step and repeat photolithography), nanowires are fabricated all across the wafer simultaneously.
2. Minimum wire width and spacing is limited by thickness of the film deposited and not by the wavelength of light, optics of lithography tools, or the resist material (as in photolithography or scanning beam lithography).

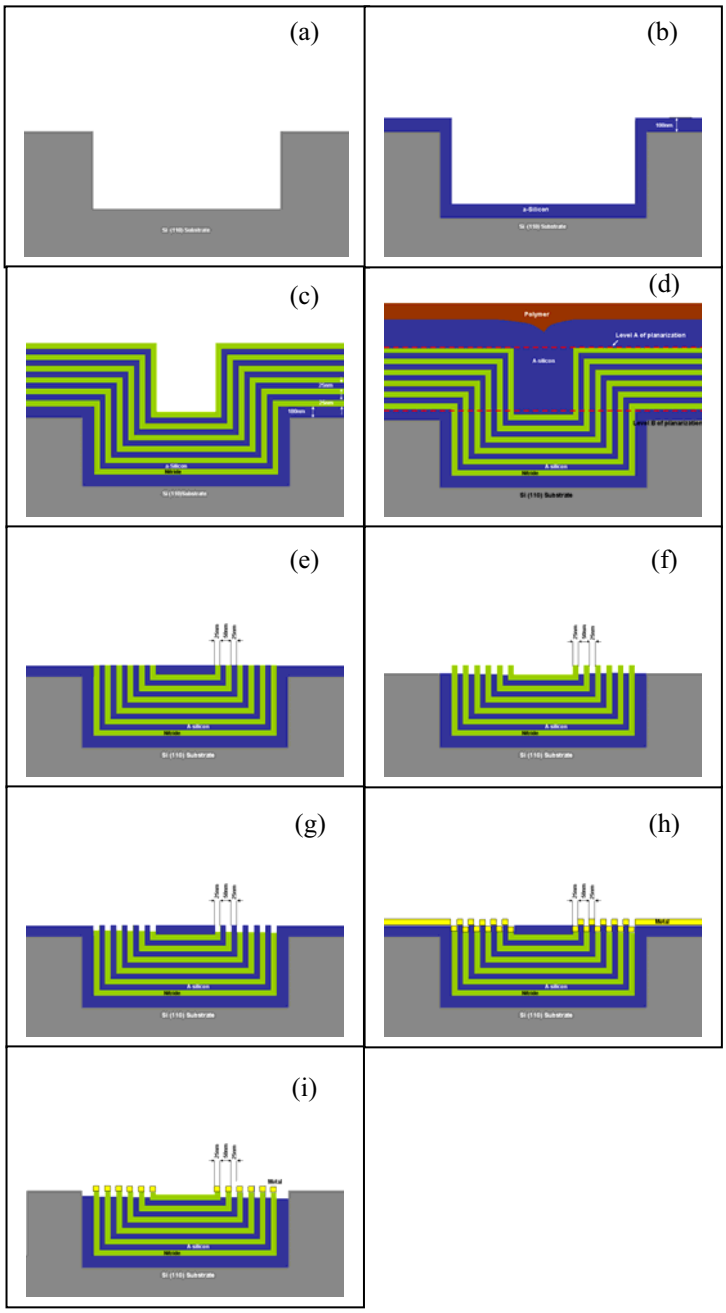


Figure 1: PEDAL and PEDAL lift-off process flow.

3. Metal nanowires with well defined spacing, length and route can be fabricated unlike non-templated self-

assembly process and superlattice nanowire transfer process.

4. Nanowires can be aligned to other layers of the integrated circuit with alignment accuracy dependant on the initial lithography step used to define the step edge.
5. PEDAL process has the potential to make sub-5 nm nanowire structures by integrating with Atomic layer deposition, which has the capability of depositing conformal monolayer of wide range of materials with nanometer accuracy and control.
6. PEDAL process is feasible and fits in existing fabrication infrastructure and does not need costly lithographic tools like ebeam lithography or EUV lithography tools which are needed in most of the existing nanofabrication techniques to make initial masks, molds or templates.

Limitations of PEDAL process:

1. Looping of lines and spaces fabricated by PEDAL process needs truncation.
2. PEDAL technique is limited to fabrication of continuous lines and spaces. Designs like T-junctions, Cross junctions and other designs which need intersection of two lines are difficult to make using PEDAL process.
3. The process of fabricating array of lines and spaces can be slow depending on the deposition method and number of lines and spaces in an array.

IV. EXPERIMENT

P-type Silicon (110) wafers were cleaned in JTB solution for 10 minutes followed by DI water rinse and spin drying. Using 100 nm thick silicon nitride as a mask, trenches 1.8 micron deep were was etched in the silicon <110> wafer in 40 % KOH solution at 80 C. The edges of the trench were aligned to the (1 -1 -2) and (1 -1 2) directions along which <110> plane intersects <1-11> and <-111> plane at right angle giving smooth vertical sidewalls of the trench along the length of the line. However, in and around the regions where the two axis (1 -1 -2) and (1 -1 2) meet, corners obtained are not sharp due to process limitations and non-vertical etch fronts other than <1-11> and <-1 1 1> are revealed. However along the length of the trenches, sidewalls are vertical and the uniformity results shown in this report are based on the nanowire structures obtained along the length and not the corners of the route. Highly anisotropic etches using DRIE or ICP RIE systems have been published [35, 36] providing the smooth vertical sidewall along the entire route of the trench, however those processes have not been used in this research. After defining trench the wafers were divided into two batches. On batch 1, thin silicon nitride film with average thickness of 242 A is deposited in a horizontal hot-wall LPCVD system at 300 mTorr and 775 C using Dichlorosilane and ammonia gas. These wafers were later put in a-silicon LPCVD furnace to deposit thin a-silicon film at 130 mTorr and 535 C using Silane. The average width of a-silicon film measured was 232 A. On batch 2, thin silicon nitride film with average thickness of 131 A is deposited followed by a-silicon deposition with average film thickness 132 A. On both the batches thin silicon nitride films and amorphous silicon films are alternately deposited depending on the number of lines and spaces for each case. After deposition of thin films, a sacrificial layer of 8000A thick a-silicon is deposited to fill the trench completely. The topography of trench is then planarized by spinning organic polymer, Shipley 1813 of average thickness 13800 A. In order to reveal vertical line-width structures, each wafer is made planar till level A ,shown in figure 1 (d), by RIE etch recipe non-selective to polymer and a-silicon, and then wafer is made planar till level B using RIE etch recipe non-selective to silicon nitride and a-silicon. To planarize the wafer till Level A, RIE was done at 30 mTorr and 100 Watts using 15 sccm SF_6 and 12.5 sccm O_2. For this recipe, the selectivity between silicon <110>, a-silicon and Shipley 1813 obtained was 1.05:1:0.98. To Planarize the wafer till Level B RIE was done at 30 mTorr and 100 Watts using 88 sccm Ar, 5 sccm SF_6 and 10 sccm CHF_3. For this recipe the etch rate selectivity of silicon nitride, a-silicon and polymer Shipley 1813 varied from 1:1:0.96 to 1:1.13:0.93. After planarization, line and spaces are obtained by selectively wet etching either a-silicon or silicon nitride. Silicon nitride mold for nanoimprinting nanowires is created by selectively wet etching 50 nm of a-silicon in solution of HNO_3 and HF. If the heights of silicon nitride line are not even, then the whole wafer is spin-coated with polymer and planarized again using Ar, SF_6, CHF_3 recipe as mentioned above till the desired level. This etch-recess-coat and repeat process has given excellent uniformity of heights of silicon nitride lines. Height of linewidth structures in the mold can be increased by increasing the amount of a-silicon etched. PEDAL lift-off process to fabricate metal nanowires directly on the template is demonstrated on LOT 1. In PEDAL lift-off process, after planarization, lines and spaces are revealed by selectively wet etching 100 nm silicon nitride, and if necessary followed by etch-recess-coat and repeat process. After etching 100 nm silicon nitride, 100 A of Pd is deposited on the template by e-beam evaporation followed by Pd lift-off done by wet-etching a-silicon. This leaves 100 A thick Pd nanowires on silicon nitride lines with average expected width of 242 A spaced at 232 A.

V. RESULTS -UNIFORMITY AND PLANARITY

The uniformity and repeatability of a-silicon and silicon nitride deposition process directly influences the uniformity of lines and spaces obtained in PEDAL template as well as metal nanowires fabricated after hard lift-off. The measurements showed that from run to run the wafer scale average amorphous silicon thickness varies from 225.6 A to 237.7 A with overall average thickness of 231.9 A and standard deviation between 1A to 8A. Considering the observed 81 % conformality of deposited a-silicon films, we can predict that if a-silicon layers define spaces on template then average

space width will be 184 A with the standard deviation less than 1nm. In silicon nitride deposition process, measurements showed that from run to run wafer scale average silicon nitride thickness varies from 237.5 A to 246.2 A, with overall thickness of 242 A and standard deviation between 4A to 9 A. Considering 100 % conformality of silicon nitride films we can predict that average width of silicon nitride lines in an array on the template will be 242 A with standard deviation less 1nm.

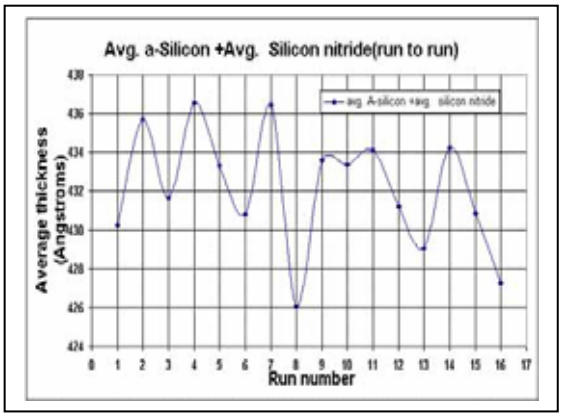
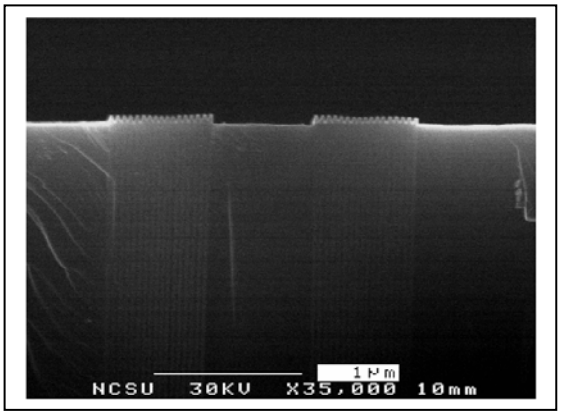


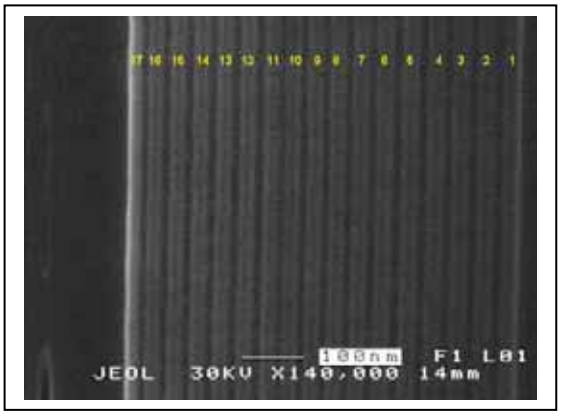
Figure 2: Average pitch of the nanowire template on LOT 1 calculated from the film thickness measurements after considering non-conformality of a-silicon.

From the graph shown in figure 2 we find that average of the calculated estimated pitch is 432.17 A with standard deviation of these average value less than 3.1 A. Figure 3 shows SEM of the cross-section and top view of the template obtained after selectively wet-etching 50 nm of a-silicon and figure 4 shows the top view of the 100 A thick Pd nanowires obtained after hard lift-off process. In order to assess the uniformity in the nanowire width and spacing of template across the entire 4 inch wafer, width of line and space number 1 {figure 3b} was measured and the results are shown in the graph in figure 5. From the measurements, average width of line was found to be 23.75 nm with standard deviation of 1.7 nm, whereas average spacing was found to be 17.1 nm with the standard deviation of 1.23 nm. This gives us the average pitch of the array of lines and spaces on template as 40.83 nm with standard deviation of 2.29 nm. Average values of widths of lines and spaces on templates differ by over 10 A from the values for first line and space predicted by thin film deposition measurements, and the standard deviation observed is more than twice the predicted. One of the possible reasons can be limitations of the measurement technique used to determine the values of line and space width. Some of the factors adding to errors in the measurements done by SEM are the charging of the silicon nitride layer, and the tilt in sample loading. More elaborate measurement technique like TEM will be needed for more accurate measurements and comparison with thin film data.

SEM measurements were also done to assess the uniformity of the adjoining lines and spaces in an array on the template. These results are shown in figure 6. From the measurements it is observed that in an array average width of the line is



(a)



(b)

Figure 3: SEM of the template obtained by PEDAL process in LOT 1 (a) cross-section of the template (b) top view of the template, obtained after selectively etching a-silicon films

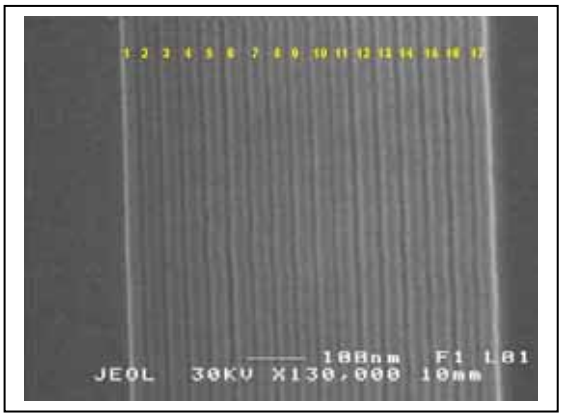


Figure 4: SEM of the top view of 100 angstroms thick Palladium nanowires obtained after hard lift-off on PEDAL template on LOT 1.

around 23.94 nm with the standard deviation of 3.64 nm and average spacing is around 17.27 nm with standard deviation of 2.11 nm. This gives us the average pitch to be around 41.5 nm with the standard deviation of 4.67 nm in an array on the PEDAL process defined template.

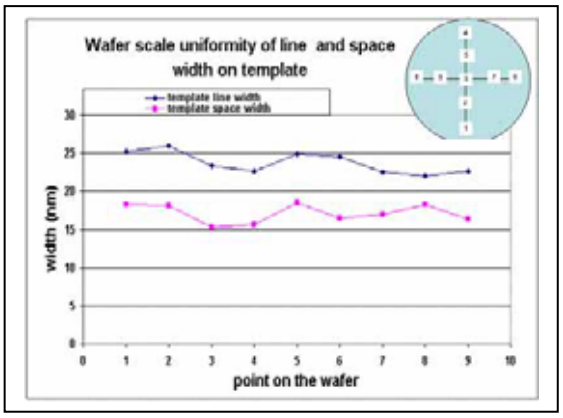
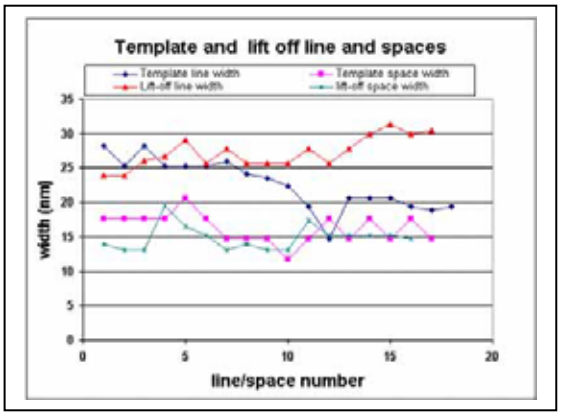


Figure 5: Wafer scale uniformity of line and space width on template in LOT 1fabricated using PEDAL process.

The average width of the Pd nanowires in an array, obtained after lift-off was found to be 27.26 nm with the standard deviation 2.28 nm and the average spacing was measured to be 14.83 nm with the standard deviation of 1.83 nm. This gives us the average pitch of the Pd nanowire arrays to be 41.89 nm with standard deviation of 3.30 nm. These measurements show that after lift-off the width of the nanowire increases and spacing decreases from the value of the lines and spaces on the template. One cause for observing increase in Pd nanowire width and decrease in spacing can be rounding of top edges of lines on the template causing the deposition of Pd on the sidewalls of lines as well. Other reason might be erroneous nonvertical or shadow evaporation of metal on these templates in E-beam evaporation process depending on the position of the wafer with respect to the metal source as well as the mounting of sample. Hence, more process control is needed to avoid evaporation of metal on sidewalls of line to get the desired result in PEDAL Lift-off process.

Measurements were also done on LOT2 to evaluate the efficacy of PEDAL process for making nanoimprint template as the line widths are scaled below 15 nm. From measurements done using ellipsometer, it was found that wafer scale average amorphous silicon thickness deposited in LOT 2 varies from 126 A to 142 A with overall average value of 135.3A and standard deviation ranging from 1 to 11 A. In the case of silicon nitride deposition, the wafer scale average of silicon nitride film thickness obtained varied from 124.3 A to 136.2 A with overall thickness value of 131.5A and standard deviation ranging from 3 A to 9 A. If silicon nitride defines lines and amorphous silicon defines spaces, then from calculations we will get lines of average width of 131.5 A and standard deviation between 3A to 9A, the values same as that of silicon nitride film thickness due to 100 % conformality of silicon nitride films. Considering 80% conformality of deposited a-silicon films, average space width in the PEDAL template will be 110.9 A with standard deviation less than 1nm. The graph in figure 7 shows the calculated run to run estimated pitch. The average of the estimated pitch of nanowire array in PEDAL defined template in LOT 2 is



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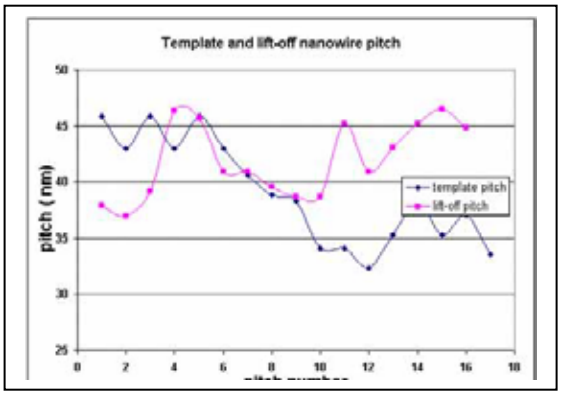


(b)

Figure 6 (a) shows the measurements of widths and spaces of template and Pd nanowires in an array obtained after lift-off in LOT 1(b) shows the pitch in LOT 1.

241.9A with the standard deviation of these average values of 4.10 A. SEM in figure 8 shows the typical top view and cross-section of nanowire template in LOT 2. In order to assess the uniformity in the nanowire width and spacing of template across the entire 4 inch wafer, width of nanowire and space number 1 (from figure 8) was measured and the results are shown in the graph in figure 9(a). From the measurements, average width of line was found to be 13.1 nm with standard deviation of 2.6 A, whereas average spacing was found to be 8.0 nm with standard deviation of 5.1 A. This gives us the average pitch as 21.1 nm with standard deviation of 5 A.

Measurements were also done to assess the uniformity of the adjoining lines and spaces in an array on the template. These results are shown in figure 9 (b). From the measurements it is observed that in an array average width of the line is around 13.12 nm with the standard deviation of 2.7 A and average

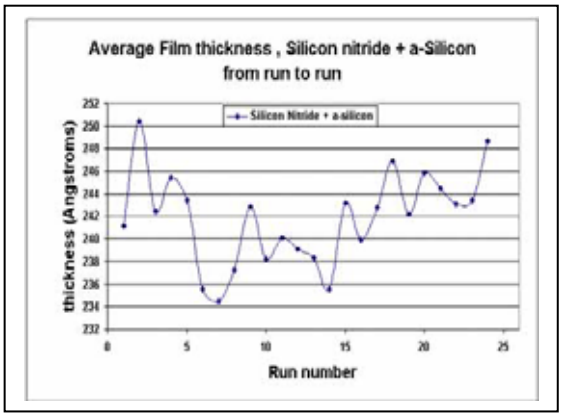
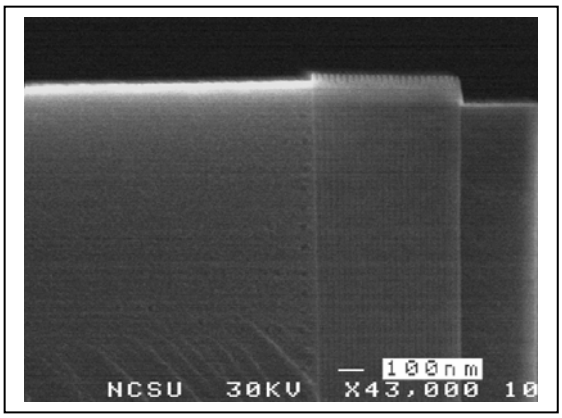


Figure 7: Average pitch of the nanowire template on LOT 2 calculated based on the film thickness measurements after considering non-conformality of a-silicon.



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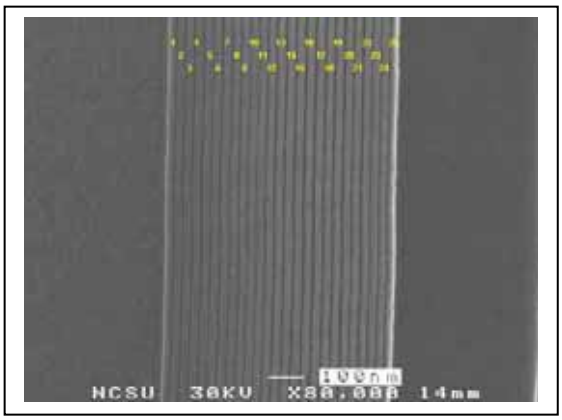
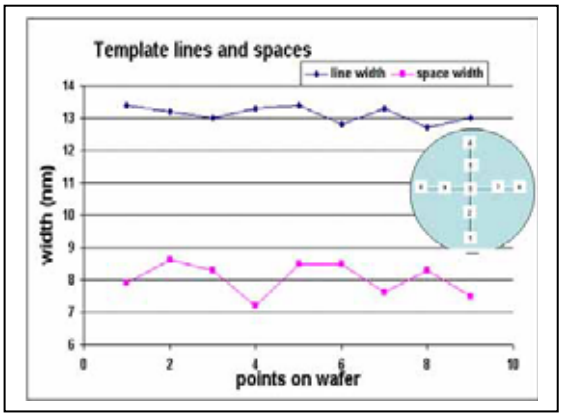


(b)

Figure 8: SEM of the template obtained by PEDAL process in LOT 2 (a) cross-section of the template (b) top view of the template, obtained after selectively etching a-silicon films

spacing is around 9.42 nm with the standard deviation of 9.1 A. This gives us the average pitch of the lines in an array to be around 22.6 nm with the standard deviation of 9.3 A. The values of silicon nitride lines on the template are close to the values calculated from the film thickness measurements which gives average width of lines as 131.5 A but the average space width is over 2 nm less than value predicted by thin film measurements of 110.9 A. This might be due to the underestimation of non-conformality of a-silicon films as well



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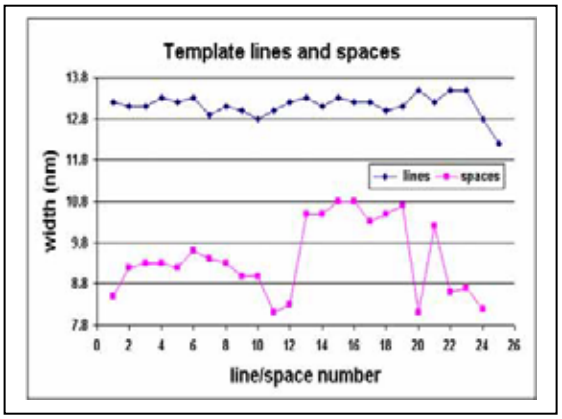


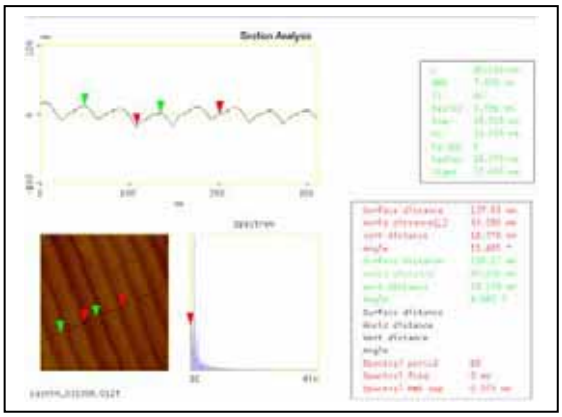
(b)

Figure 9: (a) Wafer scale uniformity of line and space width on template in LOT 2 fabricated using PEDAL process (b) measurements of widths and spaces of template in an array obtained after lift-off in LOT 2

as the limitations of SEM measurements at such small dimensions. PEDAL lift-off technique using 100 A thick Pd films was not successful on the template of LOT2. One of the main problems encountered was the adhesion of metal on adjoining lines, probably due to sloped sidewalls of template lines or non-vertical evaporation of palladium, making the lift-off the palladium difficult in the lift-off solution.

In order to evaluate the planarity of the nanoimprint mold obtained in lot 1 as well as lot 2, AFM measurements using super sharp silicon tips were done. As shown in figure 10 maximum difference between the silicon nitride lines on the LOT 1 was measured to be around 10 nm and on LOT 2 the value was measured to be less than 3 nm. These were the results obtained after doing one repeat process in etch-recess-coat and repeat RIE technique on both the lots. From the

simulations results of the planarization process, it was found that even better planarization with the maximum difference in silicon nitride heights less than 5 A can be obtained by one more repeat process in the etch-recess-coat and repeat planarization technique.



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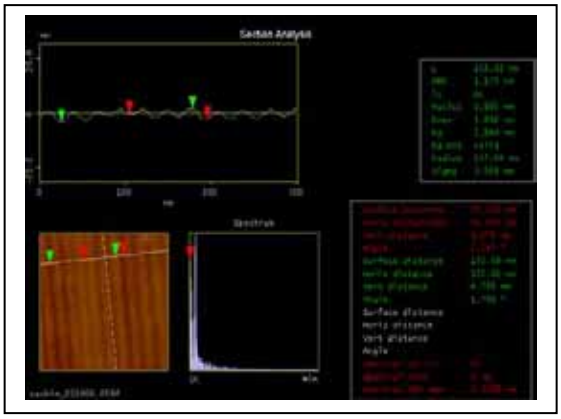

(b)

Figure 10: AFM using super sharp tips, of the nanoimprint template fabricated by PEDAL process shows planarity of silicon nitride lines with maximum difference between heights of silicon nitride lines measured to be around (a) 10 nm in LOT 1 (b) 3 nm in LOT 2. (Sharp edges are not observed in the AFM images due to AFM tip convolution)

VI. Results - Routing Capability

One of the important attributes of PEDAL process for defining nanowires is its ability to route the sub-25 nm nanowires. Successful routing of nanowires greatly depends on the topography of trenches. In PEDAL process, trenches are fabricated by either reactive ion etching or by using anisotropic wet etch solutions like KOH solution. Each of these methods has limitations based on the equipment used. RIE experiments done in parallel plate SEMIGROUP RIE etch system using CHF_3 and O_2 gases for various gas concentrations were unable to provide vertical sidewalls of etched trenches. The best anistropicity using RIE method was observed for 20 sccm CHF_3 and 20 sccm O_2 at 30 mTorr and 150 W, in which the the side wall angle of 15 degres was observed. Along the route of trenches, the sidewall angle didn't change much; hence the trench profile is preserved along the corners of the route. Whereas in case of etching trench in Silicon<110> using 40 % by wt KOH solution the sidewall angle was near 90 degrees along the linear region but along the corners, the

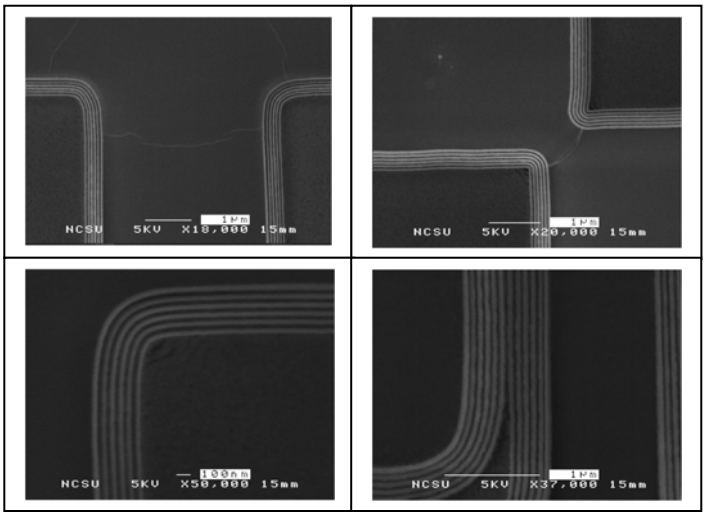

Figure 11: Shows nanowire routing capability of PEDAL process for fabricating nanoimprint template.

sidewall angles deviated significantly from 90 along the corners of the route. This deviation is the result of exposure of non-vertical etch front planes other than vertical <-111> and <1-11> planes caused by rounding of the masking features at acute corners of the route due photolithographic limitations. In the simulations, nanoimprint template with trench sidewall angle of 15 degree gave just 3 % deviation from the initial design values in the imprinted feature size. Depending on the nanowire design tolerance the template fabricated on these trenches can be used for nanoimprinting. Hence for demonstrating the nanowire routing capability of the PEDAL process, RIE process has been used to define routes of the trenches and the results shown here are for the templates obtained on these trenches. Since these experiments were aimed at demonstrating the various routing capability of lines on the template, SEM was done to verify the continuity of these lines around the corners of the route without doing actual dimensional measurements. Figure 11 shows various routes of lines and spaces on a template fabricated using PEDAL process. From the figure it's evident that the lines and spaces retain their integrity at the corners of the routes, thus proving routing capability of PEDAL process.

VII. Conclusion

Uniformity analysis of the PEDAL template suggests that average width of lines and spaces obtained on the template show a good match with the deposited film thickness measurements in case of array fo nanowires with 43 nm pitch after taking non-conformality of a-silicon into account.

However for the case of template with 23 nm pitch, width of silicon nitride matched well with thin film measurements but a-silicon lines were narrower by over 2nm possibly due to underestimation of non-conformality of a-silicon films in sub 15 nm range or due to the limitations of SEM measurements at such small dimensions. The standard deviation in the width of the lines and spaces across 4 inch wafer and in an array for the case of 43 nm pitch template was less than 2 nm and for the case of 23 nm pitch template standard deviation was less than 1 nm, making PEDAL an effective method of fabrication of waferscale nanowire imprint template. Lift-off of 100 A thick Palladium done directly on PEDAL template with 43 nm pitch lines and spaces showed shrinkage of the spaces and increase in nanowire width after lift-off. This was possibly due to rounding of top edges of silicon nitride lines on the template, causing evaporated Palladium to deposit on the sidewalls or due to the erroneous shadow deposition of evaporated metal on the template depending on the tilt and placement of the sample. AFM measurements done on the template showed that the planarity of the template is suitable for nanoimprinting application and the planarity improved for the template with narrower nanowires. Routing of lines and space on the template obtained by PEDAL process using RIE for defining the trench showed no discontinuity of the lines and spaces around the corners or the length of the route. The comprehensive analysis done in this paper suggests that PEDAL is an effective method for fabricating waferscale nanowire template with good critical dimension control.

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REFERENCES

[1] Sonkusale. S, Amsinck C. J, Nackashi D. P, Di Spigna N. H, Barlage D, Johnson M, Franzon P. D, " Fabrication of wafer-scale, aligned Sub-25 nm nanowires and templates using Planar Edge Defined Alternate Layer (PEDAL)Process," Physica E. Low Dimensional Systems and Nanostructures 28 (2005), pp. 107-114

[2] Sonkusale. S, Amsinck C. J, Nackashi D. P, Di Spigna N. H, Barlage D, Johnson M, Franzon P. D, "Wafer scale aligned sub-25nm Metal Nanowires on Silicon (110) using PEDAL lift-off process," Proceedings of Nano Science and Technology Institute (NSTI) conference 2005, v3, pp. 255.

[3] Chou, S. Y.; Krauss, P. R.; Renstrom, P. J. *Science* 1996, *272*,85.

[4] Xia, Y.; Whitesides, G. M. *Angew. Chem., Int. Ed. Engl.* 1998, *37*, 550.

[5] Xia, Y.; Rogers, J. A.; Paul, K. E.; Whitesides, G. M. *Chem. Rev.* 1999, *99*, 1823.

[6] Gates, B. D.; Xu, Q.; Love, J. C.; Wolfe, D. B.; Whitesides, G. M. *Annu. Rev. Mater. Res.* 2004, *34*, 339.

[7] Xia, Y.; Whitesides, G. M. *Annu. Rev. Mater. Sci.* 1998, *28*, 153.

[8] Eigler, D. M.; Schweizer, E. K. *Nature* 1990, *344*, 524.

[9] Quate, C. F. *Surf. Sci.* 1997, *386*, 259.

[10] Piner, R. D.; Zhu, J.; Xu, F.; Hong, S.; Mirkin, C. A. *Science* 1999, *283*, 661.

[11] Ginger, D. S.; Zhang, H.; Mirkin, C. A. *Angew. Chem., Int. Ed.* 2004, *43*, 30.

[12] Kraemer, S.; Fuierer, R. R.; Gorman, C. B. *Chem. Rev.* 2003, *103*, 4367.

[13] Nyffenegger, R. M.; Penner, R. M. *Chem. Rev.* 1997, *97*, 1195.

[14] Wouters, D.; Schubert, U. S. *Angew. Chem., Int. Ed.* 2004, *43*, 2480.

[15] Aizenberg, J.; Black, A. J.; Whitesides, G. M. *Nature* 1999, *398*, 495.

[16] Xia, Y.; Kim, E.; Zhao, X.-M.; Rogers, J. A.; Prentiss, M.; Whitesides, G. M. *Science* 1996, *273*, 347.

[17] Xia, Y.; McClelland, J. J.; Gupta, R.; Qin, D.; Zhao, X. M.; Sohn, L. L.; Celotta, R. J.; Whitesides, G. M. *Adv. Mater.* 1997, *9*, 147.

[18] Aizenberg, J.; Black, A. J.; Whitesides, G. M. *Nature* 1998, *394*,868.

[19] Pfeiffer, L.; West, K. W.; Stormer, H. L.; Eisenstein, J. P.; Baldwin, K. W.; Gershoni, D.; Spector, J. *Appl. Phys. Lett.* 1990, *56*, 1697.'

[20] Flanders, D. C.; White, A. E. *J. Vac. Sci. Technol.* 1981, *19*, 892.

[21] Melosh, N. A.; Boukai, A.; Diana, F.; Gerardot, B.; Badolato, A.; Petroff, P. M.; Heath, J. R. *Science* 2003, *300*, 112.

[22] Xu, Q.; Gates, B.; Whitesides, G. M. *J. Am. Chem. Soc.* 2004, *126*, 1332.

[23] Gates, B. D.; Xu, Q.; Thalladi, V. R.; Cao, T.; Knickerbocker, T.; Whitesides, G. M. *Angew. Chem., Int. Ed.* 2004, *43*, 2780.

[24] Toh, K. K. H.; Dao, G.; Singh, R.; Gaw, H. *Proc. SPIE-Int. Soc. Opt. Eng.* 1991, *1496*, 27.

[25] Zach, M. P.; Ng, K. H.; Penner, R. M. *Science* 2000, *290*, 2120.

[26] Whitesides, G. M.; Mathias, J. P.; Seto, C. T. *Science* 1991, *254*, 1312.

[27] Lehn, J. M. Supramolecular Chemistry: Concepts and Perspectives; John Wiley & Sons: New York, 1995.

[28] Balzani, V.; Credi, A.; Raymo, F. M.; Stoddart, J. F. *Angew. Chem., Int. Ed.* 2000, *39*, 3349.

[29] Boncheva, M.; Bruzewicz, D. A.; Whitesides, G. M. *Pure Appl. Chem.* 2003, *75*, 621.

[30] Yang, P.; Deng, T.; Zhao, D.; Feng, P.; Pine, D.; Chmelka, B. F.; Whitesides, G. M.; Stucky, G. D. *Science* 1998, *282*, 2244.

[31] Wilder, K.; Soh, H. T.; Atalar, A.; Quate, C. F. *Rev. Sci. Instrum.* 1999, *70*, 2822.

[32] Geissler, M.; Xia, Y. *Adv. Mater.* 2004, *16*, 1249.

[33] Zaidi, S. H.; Brueck, S. R. J. *J. Vac. Sci. Technol. B* 1993, *11*, 658.

[34] G.S. Mathad, D.W. Hes, Y. Horiike, T. Lii, D. Misra, L. Simpson, Electrochem. Soc. Proc. 99(30) pp. 13, 173, 193, 226.

[35] Y.-K. Choi, J. Zhu, J. Grunes, J. Bokor, G.A. Somorjai, J. Phys. Chem. B 107 (15) (2003), pp. 3340.