3 Gb/s AC Coupled Chip-to-Chip Communication Using a Low Swing Pulse Receiver

Lei Luo, John M. Wilson, Stephen E. Mick, Jian Xu, Liang Zhang, and Paul D. Franzon, *Fellow, IEEE*

***Abstract*—A 120-mV$_{\rm ppd}$ low swing pulse receiver is presented for AC coupled interconnect (ACCI). Using this receiver, 3 Gb/s chip-to-chip communication is demonstrated through a wire-bonded ACCI channel with 150-fF coupling capacitors, across 15-cm FR4 microstrip lines. A test chip was fabricated in TSMC 0.18-μm CMOS technology and the driver and pulse receiver dissipate 15-mW power per I/O at 3 Gb/s, with a bit error rate less than 10^{-12}. First-time demonstration of a flip-chip ACCI is also presented, with both the AC and DC connections successfully integrated between the flipped chip and the multichip module (MCM) substrate by using the buried bump technology. For the flip-chip ACCI, 2.5 Gb/s/channel communication is demonstrated across 5.6 cm of transmission line on a MCM substrate.**

***Index Terms*—AC coupled interconnect, bandlimited communications, buried bump technology, capacitive coupling, multichip modules, pulse receiver, pulse signaling.**

I. Introduction

TECHNOLOGY scaling demands high-density and low-power off-chip input/output (I/O). The ITRS predicts the need for a 110-μm pad pitch for cost-performance area array flip-chip applications in 2008 [1], a pitch that is difficult to achieve with available technologies. Recently, several technologies have been reported using capacitive coupling to replace physical pin/solder bumps for high-density, low-power chip-to-chip communications [3]–[8]. This is based on the fact that non-contacting AC connections can be built more densely than DC connections and the AC component actually carries all the information of a digital signal. Instead of using traditional bonding wires as the DC connections at edge of chips, in AC coupled interconnect (ACCI), the buried solder bump technology provides a solution for both high-density signal I/O and power/ground pin distribution [4].

In contrast to most of the recent results focusing on stacked ICs [5]–[7], the work presented here, ACCI, is optimized for lossy, board-level, capacitively-coupled interconnect. This work enables long distance communication among multiple chips, while retaining the high-density and low-power properties of capacitive coupling. ACCI can not only satisfy the increasing demand for high-density signal I/Os, but it also saves precious chip area for more $V_{\rm dd}/G_{\rm nd}$ pins to improve power system signal integrity.

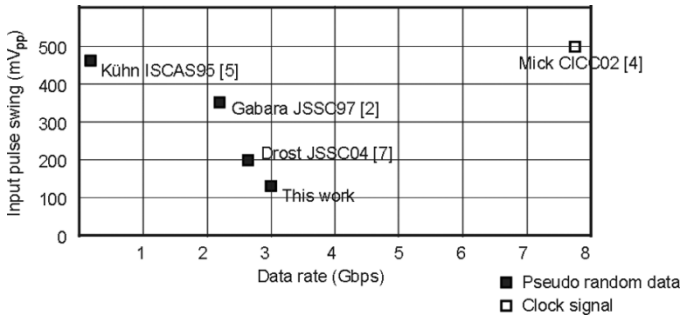

Fig. 1. Comparison with previous CMOS high-speed pulse receivers. (All scaled to 0.18 μm. To be on the same base line, single-ended $V_{\rm pp}$ is used for single-ended pulse receivers in [4]–[7]; differential $V_{\rm ppd}$ is used for differential pulse receivers in [2] and in this paper).

In this paper, the unique band-pass channel response and equalization scheme of ACCI channel are discussed and compared with the traditional low-pass response of a transmission line (T-line) channel. Coupling capacitor and T-line design rules and design margins are discussed. A voltage-mode driver is used for the ACCI channel and saves more than 70% power, when compared to a traditional current-mode driver with conductive signaling. Interconnect power dissipation is minimized by using low swing-pulse signaling. For receiver design, previous CMOS single-ended [4], [5], [7] and differential [2] pulse receivers are reported with more than 200-mV$_{\rm pp}$ input swing when scaled to 0.18-μm technology, as shown in Fig. 1. In this paper, a 3-Gb/s differential pulse receiver requiring only 120 mV$_{\rm pp}$ input swing is proposed. The three times reduction of input swing made possible by this receiver enables ACCI with a five times smaller coupling capacitance which translates to a five times higher I/O density, and a signal across longer T-lines than the previous work [4].

Chip-to-chip communication at 3 Gb/s is demonstrated through two 150-fF coupling capacitors across a 15-cm FR4 microstrip line. On the test chip, the pulse receiver converts pulses into nonreturn-to-zero (NRZ) data without a clock signal; then a semidigital dual DLL successfully recovers the receiver-side clock phase from the recovered NRZ data. An on-chip BER tester indicates errors less than 10^{-12} through one ACCI channel for rates up to 3 Gb/s. Given the density made possible by ACCI with this pulse receiver, the ITRS milestone of a 110-μm pad pitch can be achieved.

In addition, a flip-chip demonstration of ACCI is presented to show the feasibility of creating coupling capacitors and buried bumps across the same interface—between chip and

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The authors are with the Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC 27695 USA (e-mail: lluo3@ncsu.edu; jmwilson@ncsu.edu; semick@ncsu.edu; jxu6@ncsu.edu; lzhang3@ncsu.edu; paulf@ncsu.edu).

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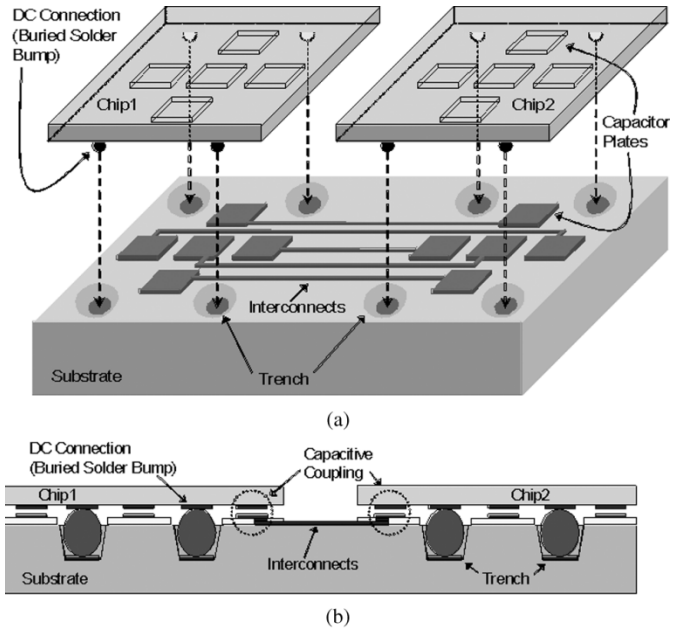


Fig. 2. ACCI physical structure. (a) Top-down view. (b) Cross-section view.

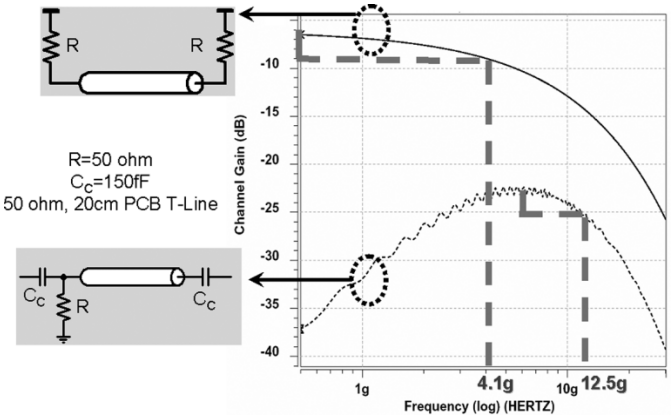


Fig. 3. Channel response of (solid curve) a T-line channel and (dotted curve) an ACCI channel.

MCM substrate. Over this flip-chip ACCI channel, two channels at 2.5 Gb/s/channel are demonstrated, across 5.6 cm of transmission line, with a measured BER less than 10^{-12}, using a single ended version of this transceiver in 0.35-μm CMOS technology.

Section II describes the ACCI physical structure and the corresponding channel response. Section III discusses pulse signaling in ACCI and its equalization scheme. Section IV presents the ACCI transceiver circuit details and the test-chip configuration. Section V and Section VI describe the wire bonded and flip-chip ACCI test setup and measurement results for each method. Section VII discusses conclusions of this research.

II. AC Coupled Interconnect

A. Physical Structure

The top-down and cross section view of ACCI are shown in Fig. 2. The key concept here is that DC connections are not needed to convey the high-frequency content of AC signals. Instead, the information in these signals can be transported by AC connections, such as a series capacitor. The advantage of AC connections is that circuit design considerations can be made the limiting factor to achieving high I/O density rather than physical limitations such as the manufacturability of dense arrays of sub-100-μm solder bumps [10]. The buried solder bump has two purposes. First, the solder bumps provide evenly distributed DC connections (e.g., for power, ground, and bias signals) across the interface with normal size solder bumps. Second, the buried solder bumps provide a means to self-align the chip and package surfaces while maintaining a close, controlled proximity between corresponding capacitor plates [4]. In this way, evenly distributed AC and DC paths are simultaneously created across the same interface between chip and package (though a MCM is shown, it can be used for conventional packaging). Although capacitive coupling is demonstrated here, inductive coupling is an alternative implementation for ACCI [4].

B. Channel Response

As shown in Fig. 3, instead of the low-pass channel response of a traditional T-line, in ACCI, the combination of serial coupling capacitors, parasitic capacitors, and the T-line create a channel from transmitter (TX) to receiver (RX) with a band-pass response. The T-line and parasitic capacitors define the low-pass characteristics while the coupling capacitors define the high-pass characteristics of the ACCI channel response. The series coupling capacitors filter out the low-frequency components of transmitted data, thereby reducing ISI and effectively extending channel bandwidth to higher frequencies. For example, the 3-dB bandwidth of the ACCI circuit shown in Fig. 3 is three times larger (12.5 versus 4.1 GHz) when compared with a traditional channel having the same T-line length. However, low-frequency attenuation needs to be compensated through equalization and this will be addressed in Section III. It should be noted that there is a need to increase sensitivity of the receivers due to the broad approximate 20-dB loss for the ACCI channel compared to the conventional conductive channel.

C. Impedance Matching at Transmitter Side

To minimize reflections, either or both sides of the transmission line should be impedance matched. Terminating at the transmitter side reduces reflections and allows the receiver side to remain high impedance which in turn provides for voltage doubling as a transmitted pulse encounters the high impedance receiver. As shown in Fig. 5(b), although there is about 6 db attenuation on T-line, the signal swing at far end T-line is about same as that at near end T-line due to this voltage doubling. When compared with terminating only at the receiver side, transmitter side termination will lead to a smaller pulse swing on the T-line, which causes less crosstalk noise to neighboring lines. Fig. 4(a) shows the termination scheme, where $M_{\rm p}$ and M_n form the output stage of the transmitter, C_c is the coupling capacitor, C_{p0} and C_{p1} are the parasitic capacitance and R_t is the 50 Ω termination resistor. Fig. 4(b) shows Z_t, the impedance looking back from transmission line to coupling capacitor and transmitter. As long as Z_t equals 50 Ω, the backward wave from receiver side is terminated at the driver side and thus no further reflections are generated. This is proved in the simulation waveforms in Fig. 5(b). There is reflection noise at near end

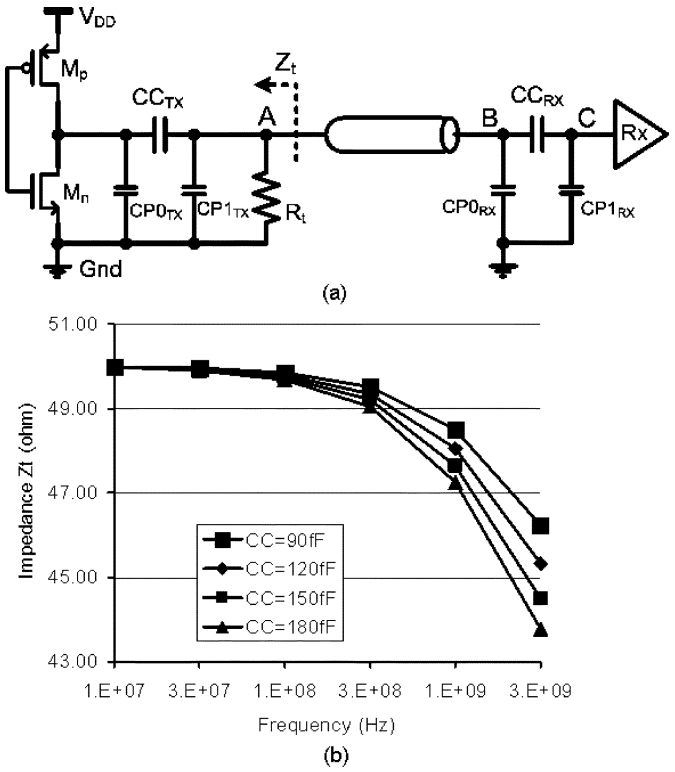


Fig. 4. (a) Transmitter side termination scheme. (b) Impedance looking back from T-line to coupling capacitor and transmitter.

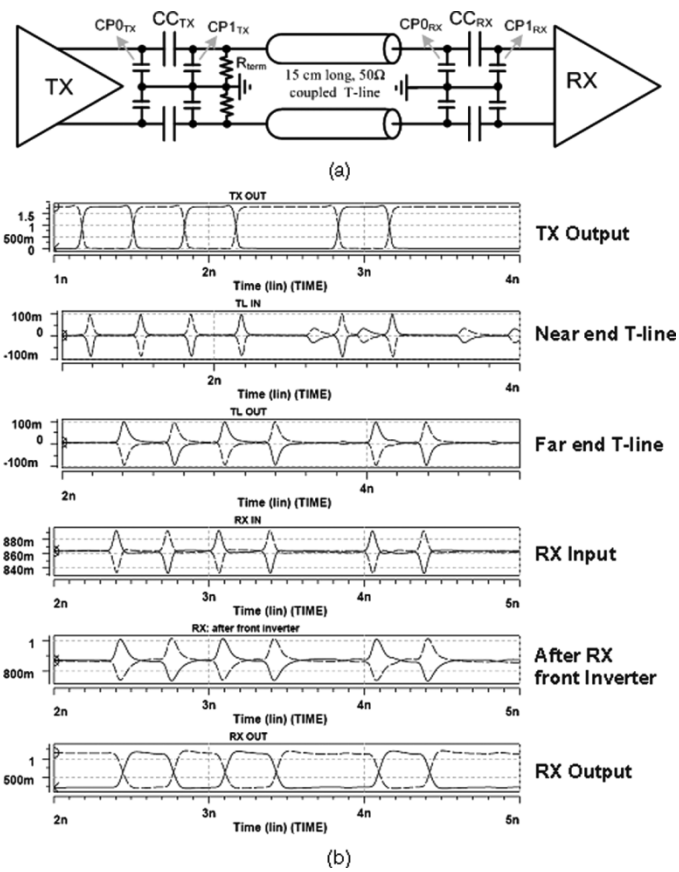


Fig. 5. Circuit view and transient waveforms of ACCI. (a) Circuit view of ACCI. (b) Pulse signaling waveforms.

T-line due to the backward reflection at un-terminated far end T-line. This backward reflection noise is absorbed by the near end termination resistor and thus no further forward reflection noise shown at far end T-line. The driver output impedance is isolated by the coupling capacitor and thus does not have to be 50 Ω. Z_t is equal to R_t at low frequencies. Though at higher frequencies, the parasitic and coupling capacitors reduce Z_t, the impedance still matches well across a wide range of coupling capacitor values.

III. Pulse Signaling

A. Pulse Signaling on ACCI

In contrast to NRZ signaling, pulse signaling has been used to reduce power consumption on interconnect by only dissipating dynamic power [4], [8], [9]. The band-pass characteristic of the ACCI channel produces return-to-zero pulse signaling, which minimize the power dissipation in the ACCI channel. Fig. 5 shows the ACCI circuit overview and the transient waveforms at the nodes associated with pulse signaling and pulse receiver. In Fig. 5, CC are the coupling capacitors and CP are the parasitic capacitors. Driver-side termination is used here, although receiver side termination is another option. The first two waveforms are time shifted 1 ns to compensate part of the delay on T-line. A pseudo-differential driver outputs full-swing, high-edge rate NRZ data; the first coupling capacitor with a T-line load acts like a differentiator, converting the data into return-to-zero (RZ) pulses at the data transitions. With the two coupling capacitors isolating the DC levels, the RZ pulses on T-line have a DC level of zero. The pulse receiver auto-generates the DC level at RX input, amplifies the incoming small pulses and converts them back into NRZ data. When compared with stacked ICs [5]–[7], ACCI has a long T-line and an additional series coupling capacitor which produce both broad-band and high-frequency channel loss. These additional elements allow the benefits of capacitive coupling to be extended to scenarios requiring long-range chip-to-chip communication, but it introduces the need for a more sensitive pulse receiver for ACCI.

B. Equalization for Pulse Signaling in ACCI

The band-pass characteristic of ACCI channels uses a different equalization scheme than that used with traditional T-line channels. High-frequency compensation used in traditional T-line channels is not required in ACCI because the 3-dB bandwidth is already extended by three times, as shown in Fig. 3. On the other hand, low-frequency compensation is necessary.

In the frequency domain, as shown in Fig. 6, the pulse receiver, is essentially a latch or edge detector, and is used to compensate the low-frequency loss and ensures a compensated channel response before the sampler. The latch detects and captures pulses, and remains stable until detecting the next opposite polarity pulse regardless of the width of the current NRZ data stream, thereby, implementing an adaptive low frequency compensator. As long as the pulse data rate is less than the latch bandwidth, the low-frequency compensation dynamically adapts to changes in pulse width caused by the T-line and coupling capacitor variations. Furthermore, as long as the NRZ

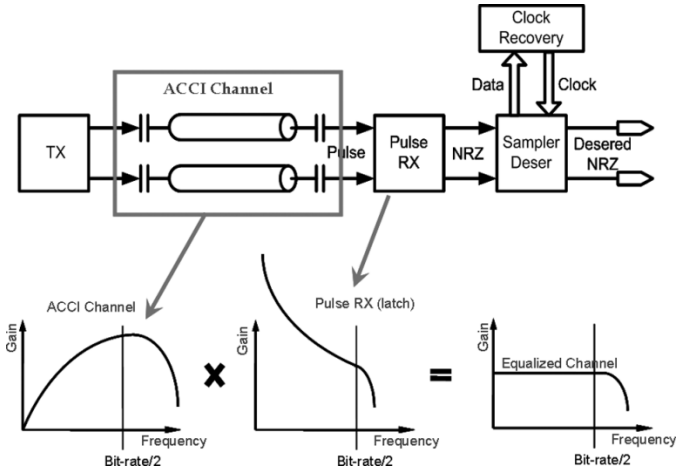


Fig. 6. Frequency domain equalization scheme for pulse signaling in ACCI.

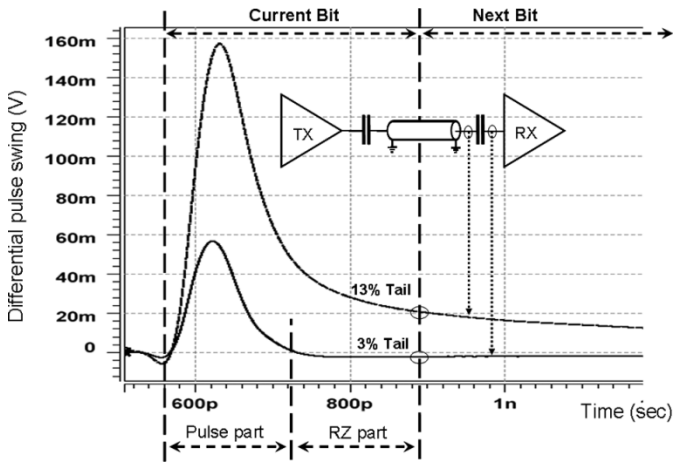


Fig. 7. Coupling capacitors provide passive high-frequency compensation in time domain. The ISI is 3% at the RX input.

signal edge rate fits in the pass band of the ACCI channel, any digital signal can pass the ACCI channel and be recovered by the pulse receiver. Theoretically, this corresponds to a digital signal with a data rate approaching dc. On the other hand, it also explains how the latch-based pulse receiver can recover long sequences of consecutive "1"s or "0"s.

Fig. 7 shows, in the time domain, how ACCI extends the bandwidth in the high frequency range. A step input to the channel results in a pulse signal on the T-line and at the receiver input. The T-line has a low-pass response due to the skin effect and dielectric loss, resulting in a long tail on the pulse signal. Without equalization, this tail would cause inter-symbol-interference (ISI) and reduce the timing margin at the receiver. The second coupling capacitor de-emphasizes the low frequency components by filtering the long pulse tail, thereby, reducing energy that interferes with adjacent pulses. This inherent passive behavior allows ACCI to save chip area and power dissipation typically associated with active high frequency compensation.

C. Valid Range of Coupling Capacitance and T-Line Lengths

The coupling capacitors and T-line parameters define the ACCI channel response and thus the pulse swing and width

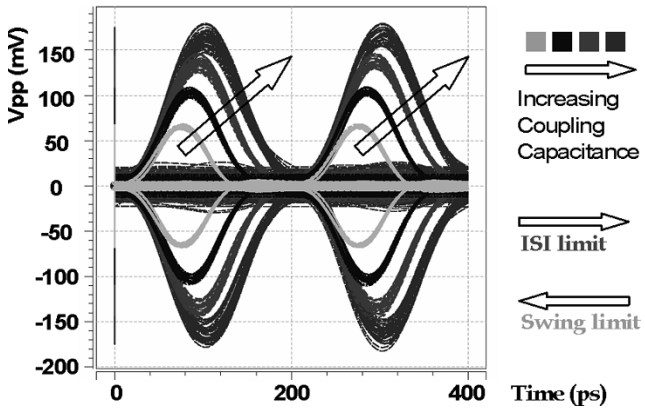


Fig. 8. Differential pulse eye diagrams with increasing coupling capacitances.

at the receiver. For a given data rate and pulse receiver input sensitivity, there is a range of coupling capacitor sizes and T-line lengths, within which a pulse receiver is able to recover the NRZ data.

Fig. 8 shows the differential pulse eye diagram after the second coupling capacitance (i.e., at the input of the receiver). The arrow shows the trend resulting from increasing the coupling capacitor size. Larger coupling capacitors will increase the peak-to-peak pulse swing and overall pulse duration. The increased swing relaxes the constraint on the receiver input sensitivity but the increased pulse width may introduce ISI. On the other hand, a smaller coupling capacitance is more efficient at filtering the pulse signal tail and mitigating ISI, but the corresponding reduction in signal swing increases the input sensitivity requirement for the pulse receiver. Therefore, the maximum coupling capacitance is constrained by the ISI limit, or the data period limit; while the minimum coupling capacitance is constrained by the swing limit, or pulse receiver input sensitivity.

Similarly, the T-line also affects channel response and pulse shape. Longer T-lines result in more attenuation, especially high frequency attenuation. This not only extends pulse width (increasing ISI) but also limits pulse swing. Thus, the maximum T-line length is constrained by both the ISI limit and swing limit.

As long as signal-to-noise ratio (SNR) allows, it is desirable to have a low-swing pulse receiver. This enables performance increase in following aspects: higher I/O density (from the use of smaller coupling capacitors) can be used; T-lines can be lengthened; the ISI constraint can be relieved and the data rate can be increased.

IV. Implementation

A. Voltage-Mode Driver

High-speed serial-link transceiver circuits typically use a current-mode driver as shown in Fig. 9(a) [15], but ACCI enables a voltage-mode driver as shown in Fig. 9(b). There are three reasons why a voltage-mode driver such as a complementary inverter pair is the best choice for ACCI. First, as show in Fig. 4(a), return impedance matching at the driver side is already provided by the parallel termination, and since the driver is blocked by the driver-side coupling capacitor it is not necessary to use a

50 Ω driver to match the T-line impedance. Secondly, the input impedance of the ACCI channel is high and more easily driven by a voltage mode driver. Finally, severe channel loss and the high frequency pass-band channel characteristic requires a full swing and high edge rate driver output, which is only possible from a voltage mode driver.

The voltage-mode driver draws dynamic current and thus, consumes much less power than a current-mode driver. Fig. 10 compares simulated 0.18 μm current-mode and voltage-mode driver power for data rates from 1 to 5 Gb/s, with a data activity of 0.5, both include appropriate parasitics for a MCM implementation. To get the same output swing (either a NRZ or return-to-zero pulse), the voltage mode driver saves 70% to 90% power depending on data rate. Dynamic supply current will introduce synchronous switching noise (SSN), which could be reduced by adding slew rate control for low data rate communications and adequate power supply filtering/decoupling.

B. Low-Swing Pulse Receiver

A pulse receiver is used to recover NRZ data from the ACCI channel. In ACCI, since the coupling capacitors block the DC signal, the receiver needs to self-bias, then amplify and convert the pulse signal into NRZ data. Fig. 11 illustrates the low swing pulse receiver. Two inverters, with negative feedback $(M_1 - M_6)$, self-bias and amplify the differential pulse signal at the receiver input. The feedback structure not only sets up the bias level but also continuously clamps the inverter into the high gain region. There are two feedback mechanisms employed here to achieve both adaptive swing control and a stable bias level to accommodate variations in coupling capacitor size and T-line length. The diode connected feedback $(M_1 - M_4)$ limits the swing at the output of the inverters by adaptively controlling the feedback strength. It also sets up a coarse bias voltage, which is sensitive to the data pattern and both the width and swing of the incoming pulses. To mitigate this problem, the NMOS devices (M_5 and M_6) tied to $V_{\rm dd}$, provide a weak but constant feedback to stabilize the bias voltage, making it less sensitive to the input pulses. The source coupled logic $(M_7 - M_9)$ further amplifies the pulses, while the cross-coupled PMOS load (M_{11} and M_{12}) serves as a clock-free latch to recover NRZ data. A clamping NMOS device (M_{10}) limits the swing of long 1 s or 0 s and enables latch operation for short pulses which improves the latch bandwidth. Fig. 12 shows the recovered NRZ data without and with the clamping NMOS device (M_{10}). The recovered NRZ data is then fed to a traditional clock and data recovery circuit to recover Rx side clock and re-sample the NRZ data.

C. Receiver Input Offset

Receiver side offset is set up by the feedback transistors. The top two curves in Fig. 13 shows the auto-biased offset voltage tracks well to the ideal inverter switching threshold voltage. This ensures the front end inverter is always biased at the switching threshold point across the fabrication corners. The bias voltage will deviate around the offset due to data activity, as shown in the bottom curve in Fig. 13. Simulation shows the peak-to-peak deviation of this bias voltage is well controlled within 10% of the total pulse swing across all the process corners.

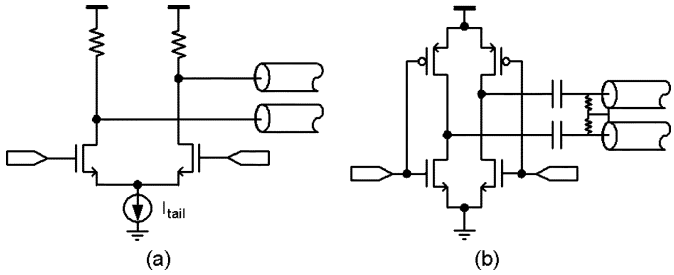


Fig. 9. Current-mode driver and voltage-mode driver.

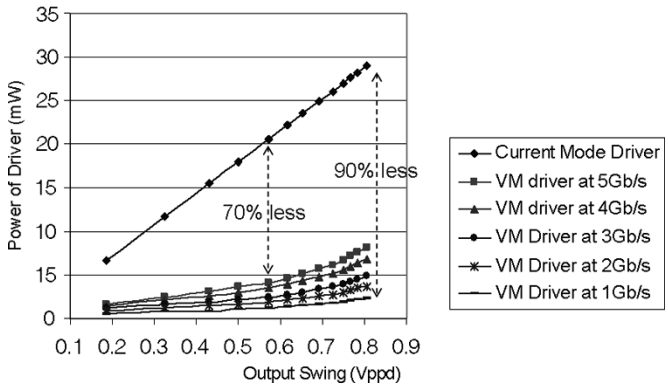


Fig. 10. Power savings on voltage mode driver, with a data activity of 0.5.

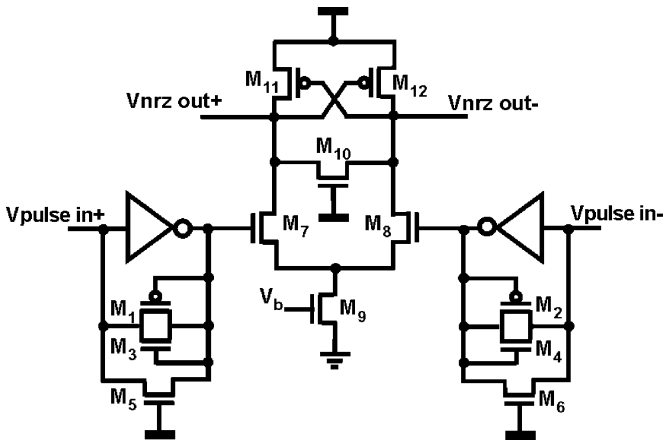


Fig. 11. Low-swing high speed pulse receiver.

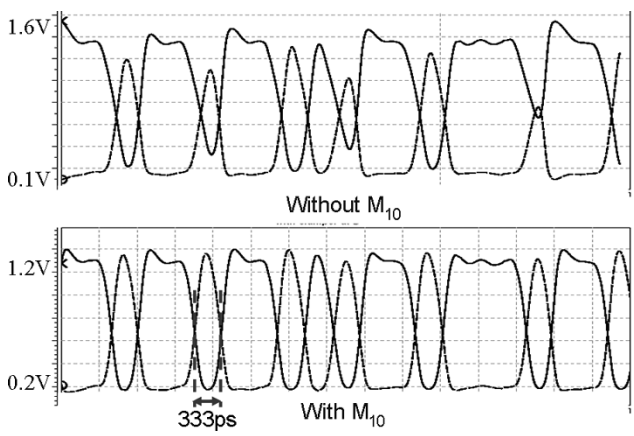


Fig. 12. Output clamping for high-speed latch operation.

D. Receiver Input Noise Margin

There are two kinds of noise margin associated with a RZ-pulse signal for a certain pulse receiver. A RZ-pulse signal, as shown in Fig. 7, can be divided into two parts in one data period, one is the pulse part, and the other is the return-to-zero part. In the pulse part, the noise margin is the difference between the pulse swing and the receiver sensitivity. For example, the sensitivity of our pulse receiver is 120 mV_{pp}, thus a 200 mV_{pp} pulse signal will have 80 mV_{pp} noise margin. In the return-to-zero part, the noise margin is the receiver sensitivity (i.e. 120 mV_{pp}) which prevents the misdetecting of noise as a valid pulse.

E. Simulated Shmoo Plot

For the voltage-mode driver and the pulse receiver discussed before, simulation shows a 0.8 unit interval (UI) opening in the recovered 3 Gb/s NRZ data with both coupling capacitors varying from 85 to 175 fF and a T-line length varying from 0 to 20 cm, as shown in Fig. 14. The transistor level parasitic capacitors at driver output and pulse receiver input are modeled by spice. Other parasitic capacitance CP shown in Fig. 5(a) are also included in the simulations. $CP0_{TX}$ and $CP1_{RX}$ are parasitic capacitance associated with the MIM capacitor size, which is estimated as 30% of the CC value. Since the test chip is not packaged in the wirebond test, $CP1_{TX}$ and $CP0_{RX}$ are estimated to be 200 fF to represent the parasitic capacitance associated with 0.025-mm diameter and 2-mm long bonding wire. The parasitic resistance and inductance associated with the bonding wires (not shown in the figure) are estimated as 0.1 Ω and 2 nH respectively. We assume the transistor layout is symmetrical and close enough so transistor mismatch is not included in this simulation. As discussed before, minimum coupling capacitance is constrained by the input pulse swing requirement of the receiver, which needs to be more than 120 mV_{ppd}. Maximum coupling capacitance is constrained by ISI in neighboring pulses, which requires pulse width to be less than the 330 ps bit period for 3 Gb/s operation. Maximum T-line length is constrained by either swing (in lower right area) or ISI limit (in upper right area). The valid operating range, for variation in both or one of the coupling capacitors, allows a ± 35 tolerance to capacitance value, which could come from the six degrees of misalignment [7]. The valid operating range of T-line lengths enables chip-to-chip communication over distance variations from 0 to 20 cm using the same transceiver cell, even with the ± 35 change in both or one of the coupling capacitors.

F. Test Chip

The block level layout of the test chip is shown in Fig. 15. TX is the voltage mode driver and RX is the pulse receiver. Four pseudo-random bit sequences (PRBS) with pattern lengths of $2^7 - 1$ are generated with spread seeds and multiplexed by four into a 3 Gb/s data stream based on four-phase DLL generated clocks. The driver outputs full-swing NRZ data into the ACCI channel. To reduce reflections, a 50-Ω shunt termination is used. The pulse receiver recovers the NRZ data from the low swing pulses and sends this data to a semidigital dual-edge DLL. The clock phase at the receiver is recovered and the data are deserialized by four and analyzed for BER.

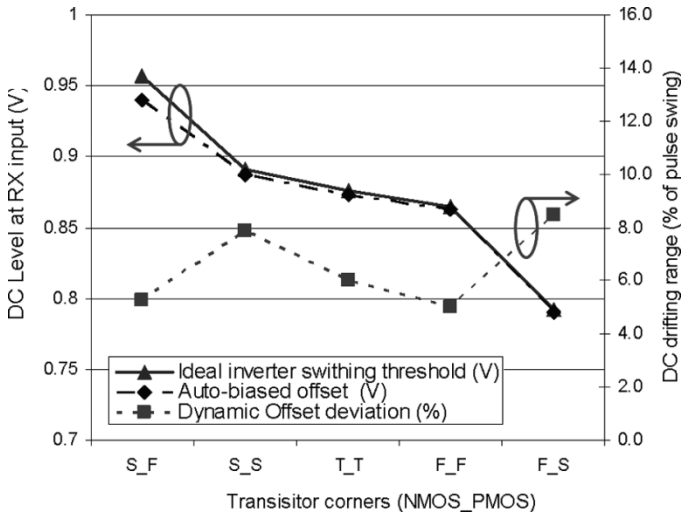


Fig. 13. RX input offset and deviation.

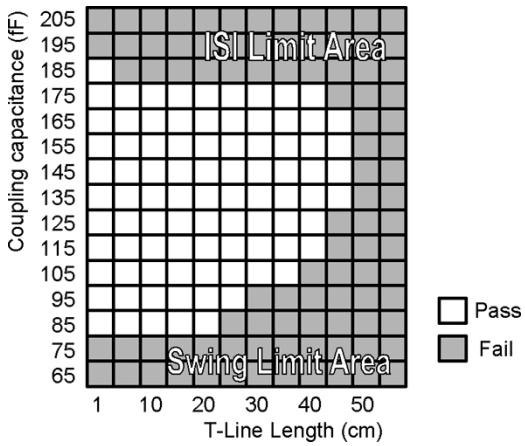


Fig. 14. Simulated shmoo plot with coupling capacitance and T-line length variations, pass criteria is a 0.8 UI time opening at the eye diagram of the recovered NRZ data.

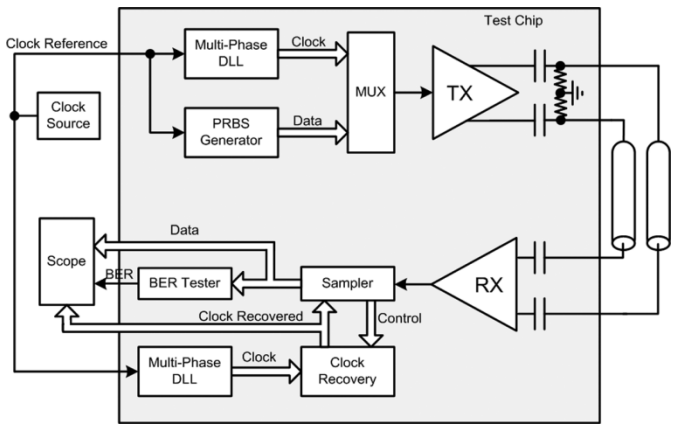


Fig. 15. Block diagram of the test chip.

G. Timing Circuits

On the test-chip, there are two timing circuits. One is a phase-recovery circuit, with a design similar to the semidigital dual delay locked loop in [12] and [13] with a phase step of 16 ps.

The other timing circuit is a multiphase DLL clock generator used by the multiplexer (MUX) in the transmitter path and for clock phase recovery in the receiver path. The MUX serializes data based on combinations of multi-phase clocks; therefore, both edges of the multiphase clocks are important and will directly influence the jitter performance of the output data. Only when all the rising/falling edges are spaced by exactly a quarter of a period will the serialized data jitter be equal to the clock jitter. Otherwise, any inter-clock phase offset, on both edges, will transfer to output deterministic jitter in addition to single clock jitter.

To minimize interclock phase offset, the delay cell employs a dual-edge control mechanism [14]. Shown in Fig. 16, both the rising and falling edge are detected and controlled by the delay cell. "VCN" & "VCP" control the rising edge of the clock line and "VCN2" & "VCP2" control falling edge of the clock line, as shown in the delay cell.

To help the phase detector minimize phase errors, it is also necessary to maintain the same rise/fall time and duty cycle for Clk_ref and Clk3. To achieve this, the drive force (output impedance) and capacitive load for each node between neighboring delay cells needs to be balanced. Dummy delay cells are placed at the beginning and end of the delay loop, and additional dummy capacitive loads are carefully inserted after post-layout RC extraction. This also helps to minimize delay deviation between the delay cells.

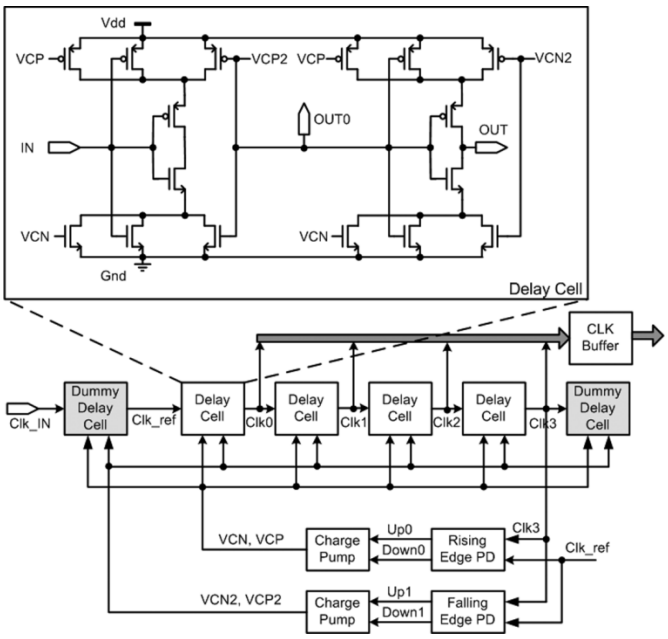


Fig. 16. Dual-edge controlled multi-phase DLL.

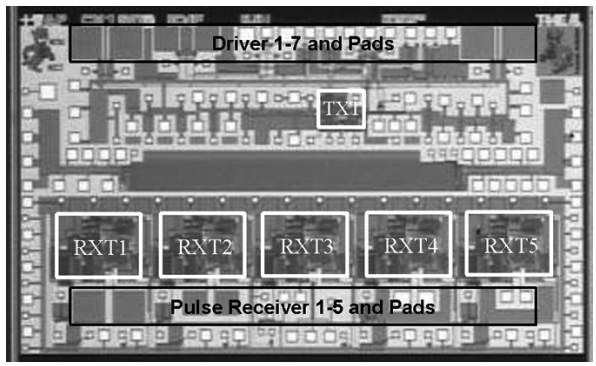


Fig. 17. Die photo of TSMC 0.18 μm CMOS test chip (2 $\times$ 3.5 mm).

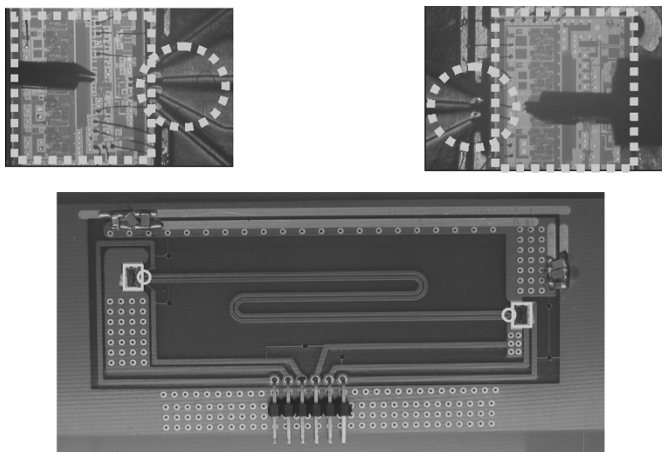


Fig. 18. Test setup on PCB.

V. Experimental Results of Wire-Bonded ACCI

A 2 $\times$ 3.5 mm test chip [16] with seven drivers and five pulse receivers was fabricated in the TSMC 0.18 μm CMOS technology (Fig. 17). Each driver and pulse receiver circuit occupies an area of 40 $\times$ 20 μm^2 and 45 $\times$ 15 μm^2, respectively. In this measurement, the AC pads at both transmitter side and receiver side are 60 $\times$60 μm^2, with 150-fF metal–insulator–metal (MIM) capacitors under it. The seven drivers share the TX test (TXT) circuitry. Each of the five pulse receivers has its individual RX test (RXT) circuitry.

The test chips are measured over an ACCI channel consisting of two 150 fF coupling capacitors and a 15-cm-long 50 Ω copper T-line on FR4, as shown in Fig. 18. Power supply and signals are wire-bonded out from the chips. A 0.75-GHz clock is generated by an HP8133A Pattern Generator and fed into the chip using a GGB Model 40A probe. Recovered clock, recovered and deserialized NRZ data, and bit error report signals are probed at the receiver chip and monitored using a Tektronix 11 801B Digital Sampling Oscilloscope.

For a 3-Gb/s data rate on each channel, the driver and pulse receiver consume 5 and 10 mW, respectively. All other test circuits in Fig. 15, except for TX and RX, consume 117 mW of power. These test circuits includes the PRBS generator, the multi-phase DLL and the 4:1 multiplexer on transmitter chip. It also includes the samplers, the multi-phase DLL, the clock recovery circuit and the BER test circuit on the receiver chip. Table I show the chip summary and measured data. BER is estimated to be below 10^{-12} based on an error-free 3 Gb/s operation according to the on-chip BER checker over at least 10 min. Fig. 19(a) shows the

TABLE I
CHIP SUMMARY AND MEASURED DATA

Process		TSMC 0.18μm CMOS 1P 6M
Supply Voltage		1.8V
Data Rate		3Gb/s/channel
BER		$< 10^{-12}$
Coupling Caps		60μm × 60μm on-chip (150fF)
Link		15cm and 50 Ω micro-strip line
Jitter of recover data		7ps RMS
Power (mW)	Pre-Driver and Driver	5
	Pulse RX	10
	Clock, test circuit and buffers	117
	Total	132

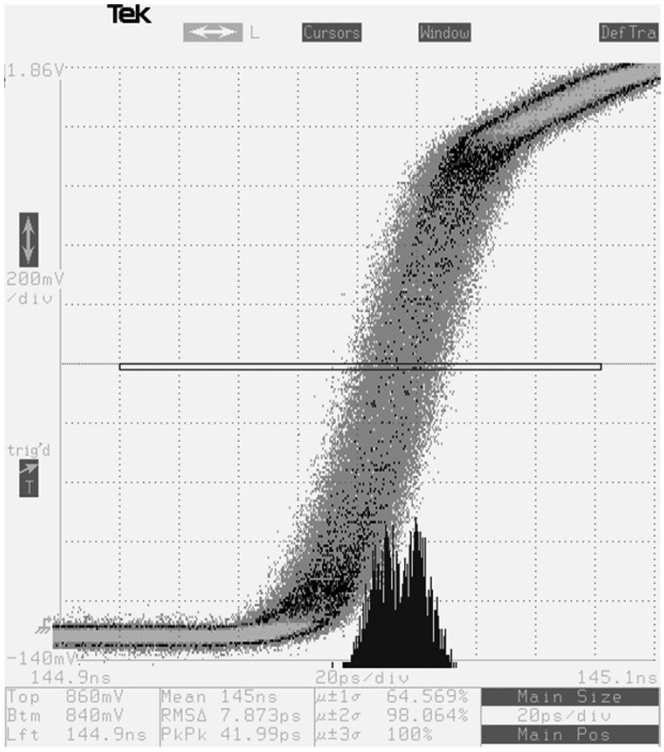
clock recovered by the semidigital dual DLL with a phase interpolation step of 16 ps. Fig. 19(b) shows the recovered and 1:4 deserialized NRZ data with 7-ps root mean squared (RMS) jitter.

VI. EXPERIMENTAL RESULTS OF FLIP-CHIP ACCI

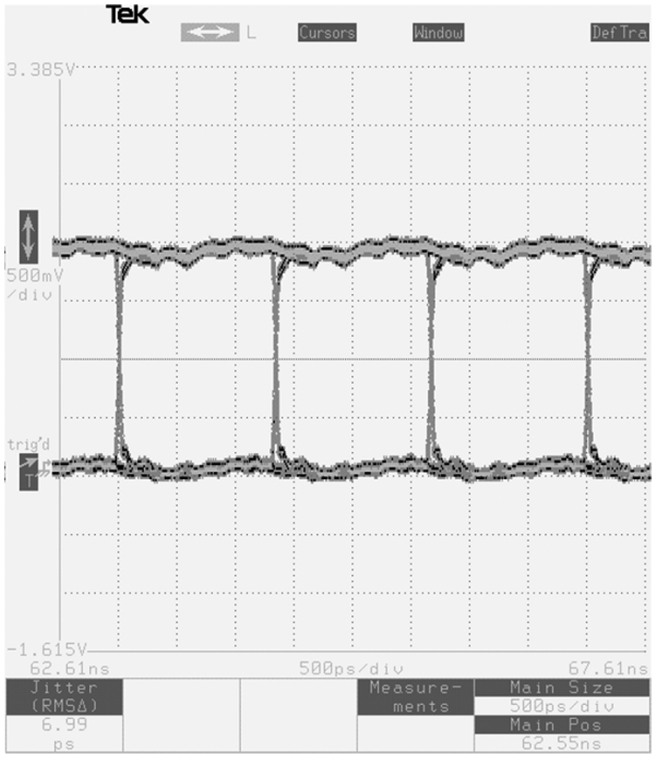
In the wire-bonded ACCI test setup, the coupling capacitor is emulated by on-chip MIM capacitors. In this section, a flip-chip ACCI demonstration proves the feasibility of creating coupling capacitors and buried bumps at the same interface between chip and MCM substrate. A 0.35 μm CMOS chip using a single-ended version of the driver and receiver was used in this flip-chip ACCI test. Shown in Fig. 20 is a photograph of an assembled MCM substrate populated with two CMOS ICs and eight decoupling capacitors. The MCM substrate has two chips mounted, but can accommodate up to four chips and includes eight sites for C4 solder ball style de-coupling capacitors (two per chip). Fig. 20 also shows a die photo of the TSMC 0.35-μm CMOS chips used in this system demonstration and a zoomed in view of a mounting site for the IC on the substrate. The mounting site contains both solder bump trenches, approximately 26 μm deep, and the plates corresponding to the capacitive AC coupling elements on the surface of the substrate. The substrate is 25 × 12.5 mm and the CMOS chip is 3.2 × 3.2 mm.

Fig. 21 shows the cross section of an assembled substrate and CMOS chip. Coupling capacitors formed by the substrate and chip interface can be seen between the buried solder balls. From the images in Fig. 21, it can be seen that there is slight misalignment in coupling elements (from 5 μm–10 μm). Misalignment in this case is due to the fact that the chips and substrates were deliberately brought into contact and friction at the interface prevented the solder bumps from self-aligning. This intimate contact resulted in a separation between the chip and MCM substrate capacitor plates of approximately 1 μm, or less, and was chosen so that the performance at minimum separation could be established. By controlling the solder ball volume and reflow parameters, any specific gap distance can be achieved.

Fig. 22 shows the measured output of the receiver chip for both a 32-bit arbitrary data pattern and PRBS $(2^7 - 1)$ data on channel 1, while channel 2 transmits and receives PRBS $(2^7 - 1)$ data. Each channel operates without error in the presence of power supply noise from the adjacent channel. The peak-to-peak jitter on the PRBS data of channel 1 is less than 120 ps.



(a)



(b)

Fig. 19. (a) Recovered clock and (b) recovered and 1:4 deserialized data.

The measured BER is less than 10^{-12}. The receiver circuit used in this flip-chip demonstration does not include the clock and data recovery circuitry used in the wire-bonded demonstration, and therefore has higher jitter at the receiver output.

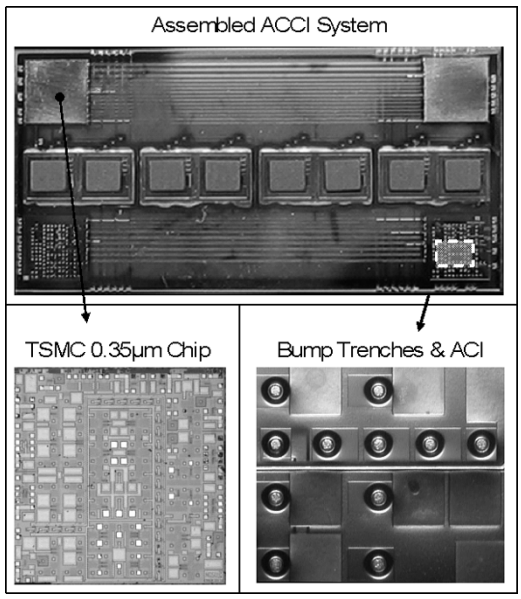


Fig. 20. Top views of assembled ACCI system, TSMC 0.35 μm CMOS chip, and solder bump trenches & AC Interconnect.

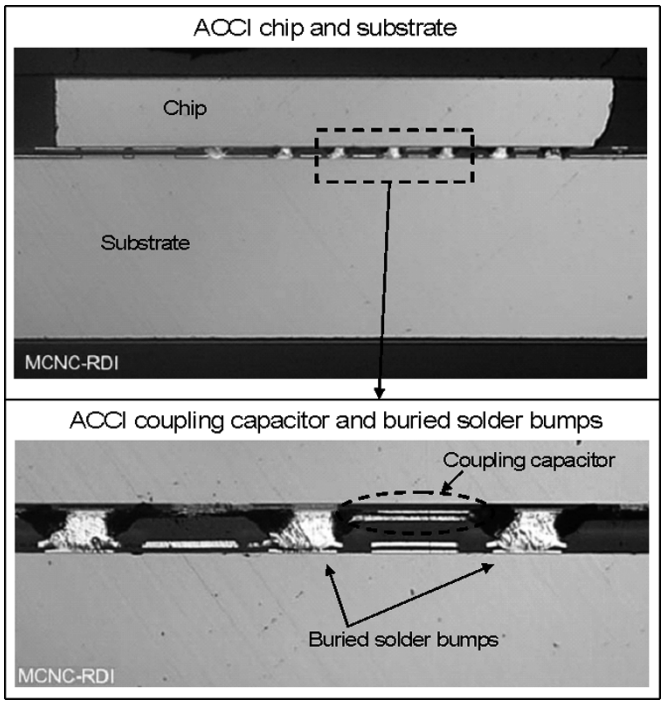


Fig. 21. Cross sectional photograph of assembled substrate and chip, with view of coupling capacitor and buried solder bumps.

VII. Conclusion

ACCI provides high-density I/O and enables communication across a 20-cm channel at 3 Gb/s/channel data rate among potentially 25 chips, assuming a five by five chip array with 2-cm chip-to-chip pitch, where the longest possible communication length is 20 cm between diagonal corners. A band-pass ACCI channel extends 3 dB bandwidth by three times and does not require active high frequency compensation techniques. Adaptive low-frequency compensation is provided by a simple pulse receiver. The inherent characteristics of an ACCI channel enables pulse signaling and the use of a voltage mode driver, which saves significant power on the interconnect and at the driver side. With a low swing pulse receiver, 3 Gb/s/channel communication is demonstrated through an wire-bonded ACCI channel with two 150-fF coupling capacitors and 15-cm-long 50 Ω copper T-line on FR4. BER is measured to be less than 10^{-12} from the on-chip BER checker.

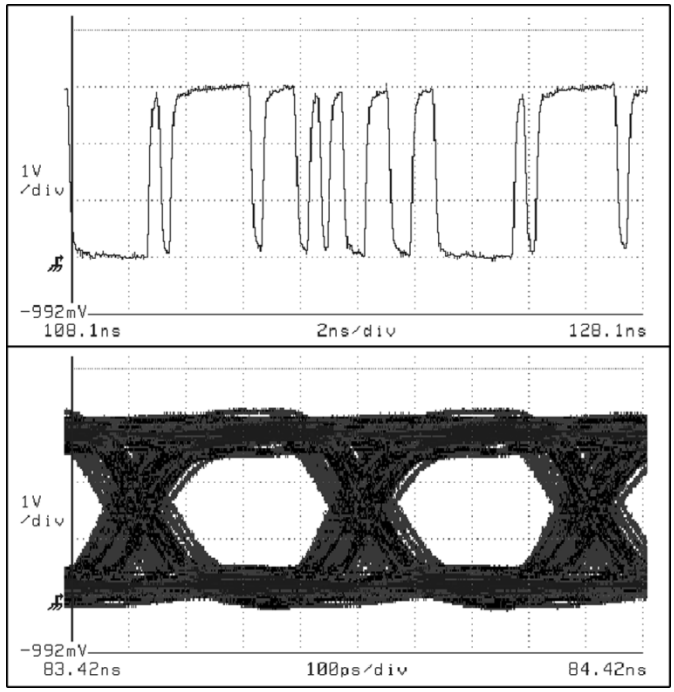


Fig. 22. Measured output for 5 Gb/s for two channels operating (2.5 Gb/s/channel): channel 1 with 32 bit arbitrary pattern and channel 1 eye with $2^7 - 1$ PRBS (channel 2 has $2^7 - 1$ PRBS for each case).

A flip-chip ACCI with buried bump technology is also demonstrated for the first time with both the AC connections (coupling capacitors) and DC connections (buried bumps) successfully integrated across the same interface between chips and MCM substrate, providing a complete solution. Over this ACCI channel, 2.5 G/s/channel communications are demonstrated with a single ended transceiver fabricated in the 0.35 μm CMOS chip, with a measured BER less than 10^{-12}.

A 150-fF on-chip coupling capacitor in wire-bonded ACCI is equivalent to a 93 $\times$ 93 μm^2 AC pad or a 110-μm pitch in flip-chip ACCI, assuming a SiO_2 gap of 2 μm. Given the density made possible by ACCI using this pulse receiver, the ITRS milestone in the year 2008 of 110 μm pad pitch can be attained in the area array flip chip application.

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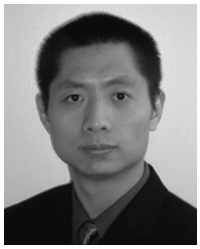
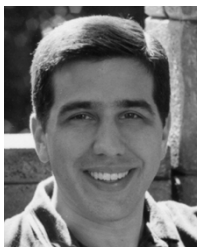


Lei Luo was born in Suzhou, China. He received the B.S. and M.S. degrees from Southeast University, Nanjing, China, in 1998 and 2001, respectively, both in radio engineering, and is currently pursuing the Ph.D. degree in electrical and computer engineering at North Carolina State University, Raleigh.

In the summer of 2004 and 2005, he was with Artisan Components (combined with ARM Holdings plc) and Rambus, Inc. designing high-speed serial link PHY IP. From 2000 to 2001, he was with Southeast Communication Inc. Nanjing, China, and worked on CDMA2000 base station signal-processing chip design. His research interests include mixed-signal circuit design for high-speed chip-to-chip communications; interchip interconnects and related signal integrity solutions, and signal processing techniques for communications.

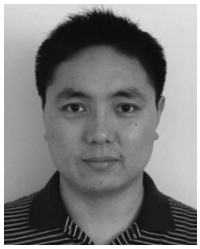
John M. Wilson received the B.S., M.S., and Ph.D. degrees in electrical engineering from North Carolina State University (NCSU), Raleigh, in 1993, 1995, and 2003, respectively. His Ph.D. research focused on the design of RF MEMS tunable capacitors.

In 1996, he was with IBM designing analog circuits for networking ICs, and in 2000, he was with a start-up company designing circuits for RFID tags. Currently, as a Research Assistant Professor at NCSU, he is leading a research effort on AC-coupled interconnect and 3D-ICs.



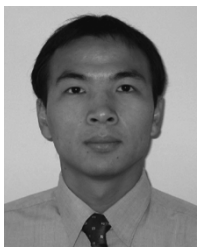
Stephen E. Mick received the B.S. degree in electrical engineering from the University of Houston, Houston, TX, in 1995, and the M.S. and Ph.D. degrees in electrical engineering from North Carolina State University, Raleigh, in 1998 and 2004, respectively.

While studying for the B.S.E.E. degree and after graduation, he worked at Texas Instruments, Dallas, TX, as an Applications Engineer, ASIC Designer, and Program Manager. His research interests include developing I/O techniques and interfaces for high-speed chip-to-chip communications and both micro- and nano-fabrication technologies.



Jian Xu received the B.S. degree in electrical engineering at Huazhong University of Science and Technology, China, in 1993. He is currently pursuing the Ph.D. degree in electrical and computer engineering at North Carolina State University, Raleigh.

He did summer internships at Motorola Laboratories and the IBM T.J. Watson Research Center in 2002 and 2005, respectively. His research interests include high-speed chip-to-chip communications, vertical signaling in 3D-IC and chip-package co-design.



Liang Zhang received the B.S. degree from Fudan University, Shanghai, China, in 1997 and the M.E. degree from the National University of Singapore in 2001, both in electrical engineering. He is currently pursuing the Ph.D. degree in electrical and computer engineering at North Carolina State University, Raleigh.

From 1997 to 1999, he was with Shanghai Belling Design Center, working on EEPROM circuits. His research interests include high-speed interconnect design and mixed-signal circuit design.

Paul D. Franzon (SM'99–F'06) received the Ph.D. degree from the University of Adelaide, Adelaide, Australia, in 1988.

He is currently a Distinguished Alumni Professor of Electrical and Computer Engineering at North Carolina State University, Raleigh. He was with AT&T Bell Laboratories, DSTO Australia, Australia Telecom, and two companies he cofounded, Communica and LightSpin Technologies. His current interests center on the technology and design of complex systems incorporating VLSI, MEMS, advanced packaging and molecular electronics. Application areas currently being explored include novel advanced packaging structures, Network Processors, SOI baseband radio circuit design for deep space, on-chip inductor and inductance issues, RF MEMS, and moleware circuits and characterization. He has lead several major efforts and published over 120 papers in these areas.

Dr. Franzon received an NSF Young Investigators Award in 1993, in 2001 was selected to join the NCSU Academy of Outstanding Teachers, and in 2003 was selected as a Distinguished Alumni Professor.