Differential Current-Mode Signaling for Robust and Power Efficient On-Chip Global Interconnects

Liang Zhang, John Wilson, Rizwan Bashirullah*, and Paul Franzon
Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC 27606
* Department of Electrical and Computer Engineering, University of Florida, Gainesville, FL 32611
Tel: (919)513-7261, Fax: (919)515-2285
Email: {lzhang3, jmwilson, paulf}@ncsu.edu, *rizwan@tec.ufl.edu

ABSTRACT
A global interconnect scheme with better current return path control is presented for accurate inductance analysis and robust interconnect design. High performance is obtained by using differential signaling, current-mode sensing, bridge termination, and driver pre-emphasis.

INTRODUCTION
On-chip global interconnects are typically routed in top-level metal layers with a large cross section to reduce resistance. With increasing signal frequency and signal edge rate, inductance is becoming an important consideration for global timing analysis and signal integrity [1]. While on-chip capacitance extraction can be restricted in a region around interested conductors without losing accuracy [2], the long-range effect of inductance makes current loops in integrated circuits unpredictable. Partial-element-equivalent-circuit (PEEC) models magnetic influence between pairs of conductor segments instead of loops [3], but it is extremely computation expensive and almost not feasible for a whole chip problem. To achieve higher modeling efficiency, loop-based inductance analysis has been proposed for clock networks with close current return paths [4].

In this work, a differential current-mode signaling scheme with drive pre-emphasis technique is proposed. It allows better return path control and loop-based inductance analysis for on-chip global buses. Diver pre-emphasis and current-mode sensing increase interconnect channel bandwidth. These techniques reduce the size of drivers and minimize the number of repeater required for global interconnects. Together with differential signaling, a current return path can be relatively well-defined and simultaneous switching noise (SSN) can be largely reduced. With a bridge resistor termination to cut the static current of current-mode signaling by half and low signal swing, this repeater-free scheme is more power-efficient than a conventional voltage mode bus scheme for data activity factors beyond 0.1. Besides, this differential scheme only requires 7.9% more bus routing area than single-ended designs for a 16-bit bus, and saves all of the repeater placement blockages.

INDUCTANCE MODEL
Magnetic interaction model as in [4, 5] is used in the inductance analysis of one pair of repeater-free differential interconnects. Fig. 1 shows current I_a flowing through interconnect $line_a$. The relationship between the time-derivative of I_a and the induced voltage V_{ind} on $line_b$ is,

$$V_{ind} = L_{ba} \frac{dI_a}{dt} \tag{1}$$

where L_{ba} is the mutual inductance of $line_a$ upon $line_b$. V_{ind} results from the integration of the induced electric field E_{ind} and E_{ind} is created by the time variation of magnetic flux Φ,

$$V_{ind} = -\int_b \vec{E}_{ind} \cdot d\vec{x} = \frac{d\Phi}{dt} \tag{2}$$

If all the current in $line_a$ is assumed to be condensed to its axis, it generates a magnetic field $B_0 = \frac{\mu_0}{2\pi Pitch} I_a$ at the center of $line_b$. μ_0 is the permeability of free space. If the magnetic field along the cross section of $line_b$ is approximated as B_0, we have,

$$\Phi = \int_{Area} \vec{B} \cdot d\vec{S} = WidthLength \frac{\mu_0}{2\pi Pitch} I_a \tag{3}$$

where S is the surface of $line_b$ on XY plane. By combining (1) - (3),

$$V_{ind} = \frac{WidthLength}{Pitch} \frac{\mu_0}{2\pi} \frac{dI_a}{dt} \tag{4}$$

From (1) and (4),

$$L_{ba} = \frac{WidthLengt}{Pitch} \frac{h}{2\pi} \mu_0 \tag{5}$$

As such, this simple closed-form calculation can be used for the inductance extraction of differential interconnects.

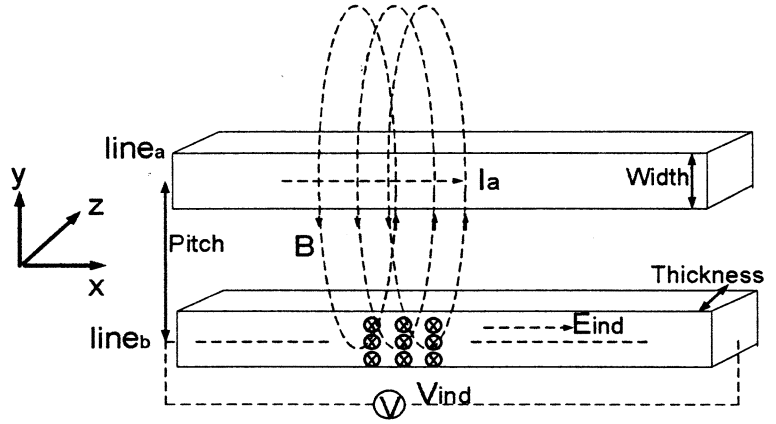

Figure 1. Magnetic field created by the time-variant current in $line_a$ induces voltage in $line_b$.

The skin effect and proximity effect are ignored in this analysis because both the skin depth and proximity depth are larger than the line width used in our interconnect scheme. For a 50pS rise time t_r, the characteristic frequency can be defined as $f = \frac{0.35}{t_r} = 7GHz$.

For an aluminum conductivity $\sigma=3.8\text{x}10^8(\Omega\text{m})^{-1}$, skin depth δ is given by [6],

$$\delta = (\pi f \mu_0 \sigma)^{-0.5} = 0.31\,\mu m \tag{6}$$

Line proximity effect can be modeled as [4],

$$R_{prox}(f) = R_{DC}\left[1 + \frac{1}{2}\left(\frac{u_0 Width^2}{R_{sheet} Pitch} f\right)^2\right] \tag{7}$$

We define the proximity depth as a width where proximity effect changes the resistance by 5% of R_{DC}. For $R_{sheet}=0.076\Omega$/square, it is roughly 5μm. Driver pre-emphasis technique and current-mode signaling allow us to use interconnects as narrow as 0.4μm for signal transmission. It is smaller than both 2δ and the proximity depth. Therefore, the skin effect and proximity effect are ignorable in this case.

INTERCONNECT SCHEME

As shown in Fig. 2, differential signaling and current-mode sensing are used to apply driver pre-emphasis technique to on-chip global interconnects [7]. A one-tap FIR filter is used to reduce driver power overhead. High frequency signal components are pre-emphasized at the driver side to improve interconnect channel bandwidth. A differential 200mV low signal swing is built on the bridge resistor R_B. This bridge termination cuts the static current of current-mode signaling by half and provides a virtual ground of $V_{DD}/2$. As a result from the driver size reduction, repeater minimization and differential signaling in this scheme, peak current is reduced by 63.8% comparing to a conventional voltage-mode bus design (Fig. 3).

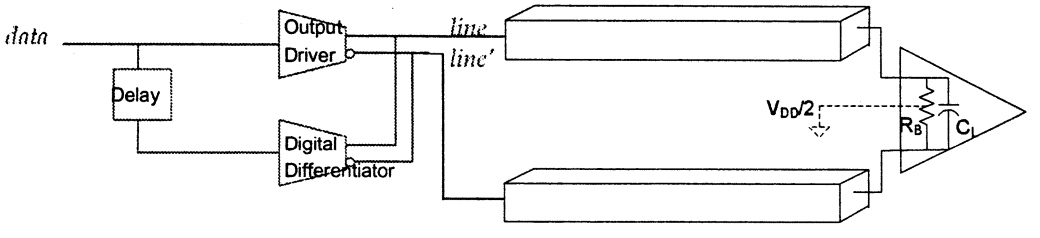

Figure 2. Interconnect scheme with driver pre-emphasis technique, differential signaling, current-mode sensing, and bridge termination.

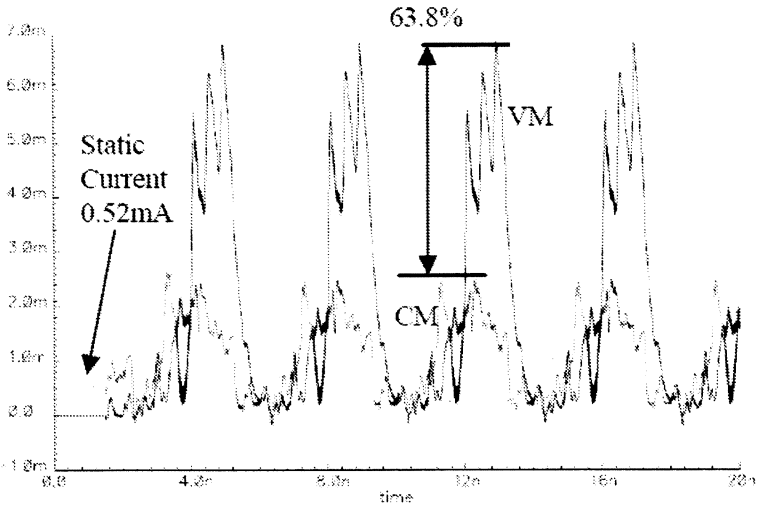

Figure 3. Peak current reduction.

Fig. 4 shows the structure implementation of a 16Gb/s differential bus and a reference bench of a single-ended full-swing bus. 10mm long metal-4 lines with 0.8μm pitch-minimum (Pmin) in TSMC 0.25μm technology are used. Every differential pair has a pitch of 3.2μm, or 2xPmin per line. The single-ended bus uses drivers with twice size of differential drivers. They still need wider wires with 3xPmin and two repeaters along each line to run signal at the same speed, plus one Vdd/Gnd shielding line for each 4-bit to provide signal return path. As such, the proposed differential bus takes only 7.9% more bus routing area than the single-ended bus and it requires none of the active area needed for repeaters. 2xPmin or 1xPmin can be used to save the routing area of the reference bench, but that requires much more repeaters to meet the delay goal.

This proposed bus architecture reduces power consumption by 26.0% to 51.2% for data activity factors above 0.2 comparing to the single-ended bus architecture and only consumes more power for data activity factors less than 0.1. Crosstalk from the same metal layer is examined by transitioning the two neighbor pairs in various directions. The coupling on the differential signal swing is always under 20% for any direction of transitions. Crosstalk of the full-swing signal from other metal layer is analyzed in Fig. 5. The worst case is that the signals on the 8-bit full-swing bus running orthogonally switch to the same direction. Their coupling on the low-swing differential bus is small due to the 1fF coupling capacitance between the two layers. As shown in the figure, it can be rejected as common-mode noise.

CONCLUSIONS

Advanced signaling methods, driver pre-emphasis, differential, and current-mode sensing, were used in this proposed interconnect scheme. The improved channel bandwidth allowed a relatively well-defined signal loop and narrow lines to be used for global communication. Therefore, this scheme is suitable for loop-based inductance analysis and robust again crosstalk noise. It generates 63.8% less peak current to help reduce SSN noise and it is more power-efficient than a conventional voltage-mode bus scheme for data activity factors beyond 0.1.

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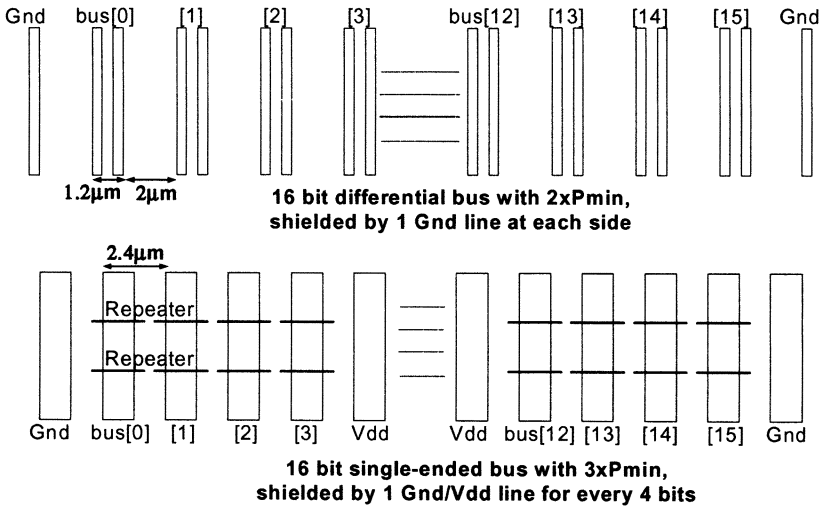

Figure 4. Differential and single-ended 16-bit bus structure.

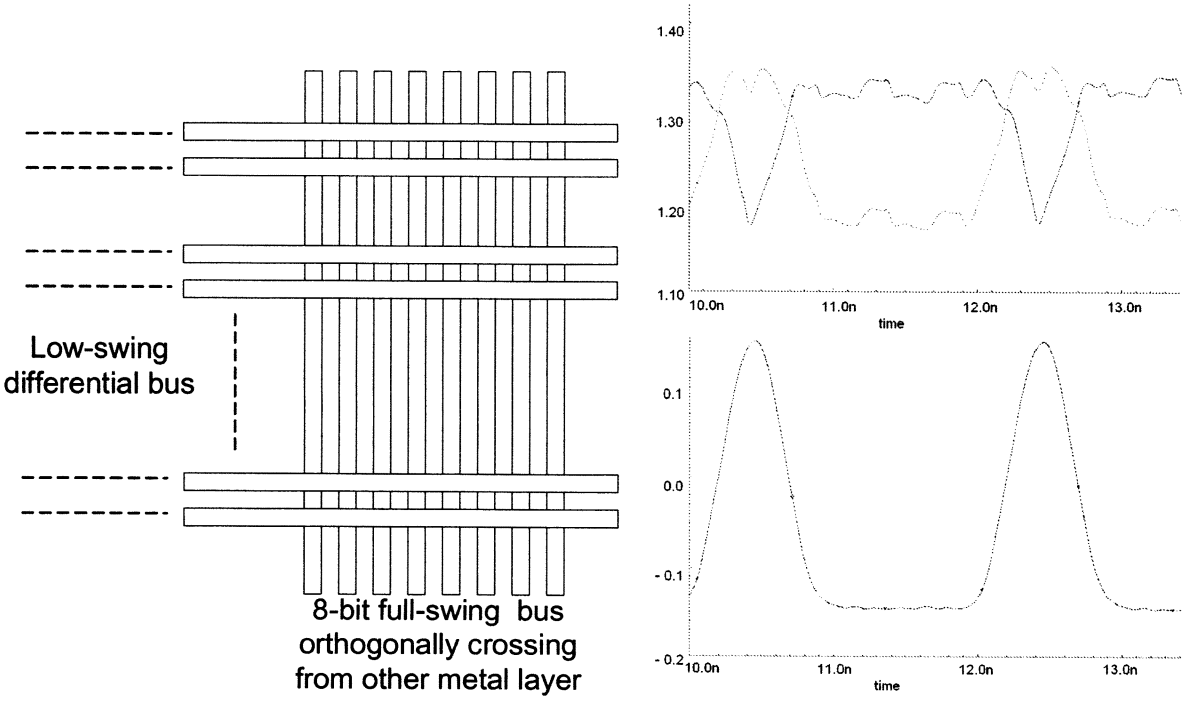

Figure 5. Crosstalk of full-swing signal from other metal layer.