2.8Gb/s Inductively Coupled Interconnect for 3-D ICs

Jian Xu, John Wilson, Stephen Mick, Lei Luo and Paul Franzon

Department of Electrical and Computer Engineering, North Carolina State University
Box 7914, Raleigh, NC 27695, USA
E-mail: {jxu6, jmwilson, semick, lluo3, paulf}@ncsu.edu

Abstract

An inductively coupled interconnect scheme for vertical signaling in 3-D ICs is demonstrated. Test chips were fabricated in TSMC 0.35µm CMOS technology, then thinned and stacked. For 90µm thick chips using 150µm inductors, the transceiver communicates NRZ signals at 2.8Gb/s, and tolerates up to 50µm misalignment. TX and RX power dissipation are 10.0mW and 37.6mW, respectively. The transceiver circuit does not require a clock to recover the data and is able to maintain less than 100ps jitter at the RX output.

Keywords: ACCI, inductive coupling, transformer, 3-D ICs, vertical signaling, transceiver.

Introduction

AC coupled interconnect (ACCI), which includes capacitive coupling and inductive coupling, can provide non-contacting signal paths between chip and substrate in a multi-chip module (MCM) [1-2]. ACCI is an attractive alternative to vertical signaling connections such as through vias or solder bumps in three-dimensional (3-D) ICs, since ACCI does not require the DC component for signaling between neighboring chips [3]. A 1.2Gb/s/pin wireless superconnect based on inductive inter-chip signaling has been reported previously [4-5].

Presented in this paper is a system operating at 2.8Gb/s per I/O using inductively coupled interconnects, also called an inter-chip transformer, for vertical signaling in a two-chip stack. The effects of chip thickness and assembly misalignment on inductive coupling were also investigated.

Characterization for Inductively Coupled Interconnect

The concept of inductively coupled interconnects for 3-D ICs is illustrated in Fig. 1, where multiple chips are thinned and stacked face-to-back. The two spiral inductors in neighboring chips overlap and form an inter-chip transformer which communicates digital signals between a TX and a RX.

The inter-chip transformer used in the inductively coupled interconnect must be modeled accurately. The magnetic coupling coefficient (k) depends strongly on the separation distance (d) between the primary and secondary inductors. In 3-D ICs, the separation distance is approximately equal to the thickness of the chips in the stack while ignoring any gap between the chips. The relationship between the coupling coefficient and the chip thickness, which was simulated using ASITIC [6], is plotted in Fig. 2. For a 90µm thick chip, the coupling coefficient is around 0.055. A lumped differential model for the inter-chip transformer was extracted from simulation results and is shown in Fig. 3.

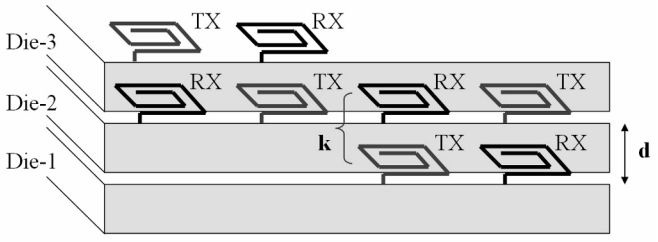

Fig. 1 Concept of inductively coupled interconnect in 3-D ICs.

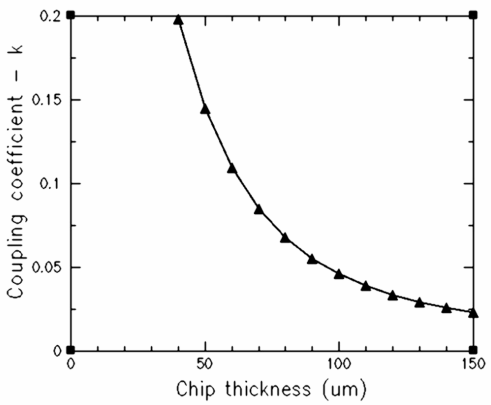

Fig. 2 Simulated (ASITIC) coupling coefficient dependence on chip thickness for a 150µm double-layer inductor with 8 turns per layer.

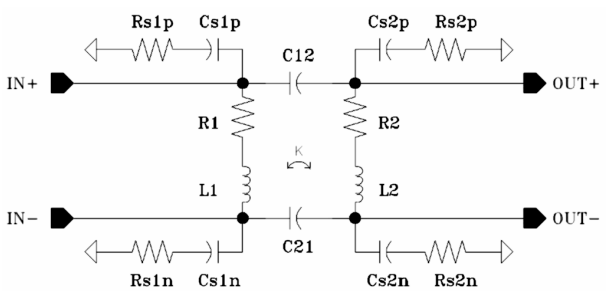

Fig. 3 Differential inter-chip transformer model: L_1 and L_2 represent the self-inductances, k represents the coupling coefficient, R_1 and R_2 represent the winding resistances, C_{12} and C_{21} represent the coupling capacitances between two overlapping inductors, R_s and C_s represent the parasitic resistances and capacitances of inductor windings.

Transceiver Circuit Design

A schematic of the current-mode transceiver circuit used for inductively coupled interconnects is shown in Fig. 4. The TX circuit is implemented using an H-bridge current steering structure. A non-return-to-zero (NRZ) input signal and its complementary signal are used to switch the H-bridge and steer the current in the primary inductor of the inter-chip

transformer. The alternating current generates an alternating magnetic field and induces current pulses in the secondary inductor.

The RX circuit can be divided into a sensing stage and a latching stage. The sensing stage of the RX, which forms a structure with low input impedance, detects current pulses from the secondary inductor and converts them into voltage pulses. The latching stage of the RX amplifies those voltage pulses and converts them into NRZ signals.

The simulation results of the transceiver system are shown in Fig. 5. The current signal in the TX inductor is a polar NRZ signal and the current signal in the RX inductor is a pulse signal, in which positive or negative pulse correspond the rising or falling edge of current swing in the TX inductor. The RX output signal is logically identical to the TX input signal except for some delay.

Demonstration System

A. Experiment Scheme

A test chip, shown in Fig. 6, for demonstrating the inductively coupled interconnect scheme was fabricated in the TSMC 0.35μm CMOS technology. A two-chip stack demonstration system is shown in Fig. 7. The bottom chip was used as the TX and was mounted on a PCB. The top chip was used as the RX and was thinned to the desired thickness, then rotated 90°, aligned and stacked on the bottom chip. The top chip was glued onto a micro-manipulator, which was used to provide precise positioning in X and Y directions. The top chip was pushed onto the bottom chip to close the gap between them.

Alignment marks were included in the layout of the chip and are visible for both top and bottom chips. By referring to the alignment marks and adjusting the micro-manipulator, it is possible to achieve perfect overlap of the coupled inductors. It also allows for arbitrary offsets of the inductors, making it possible to explore the tolerance of the transceiver system to misalignment in the 3-D assembly. Fig. 8 shows a 3-D test structure under measurement.

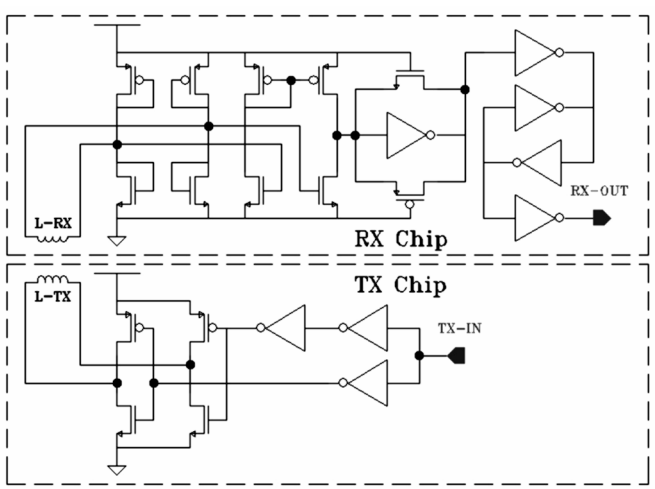

Fig. 4 Transceiver circuit for inductively coupled interconnect.

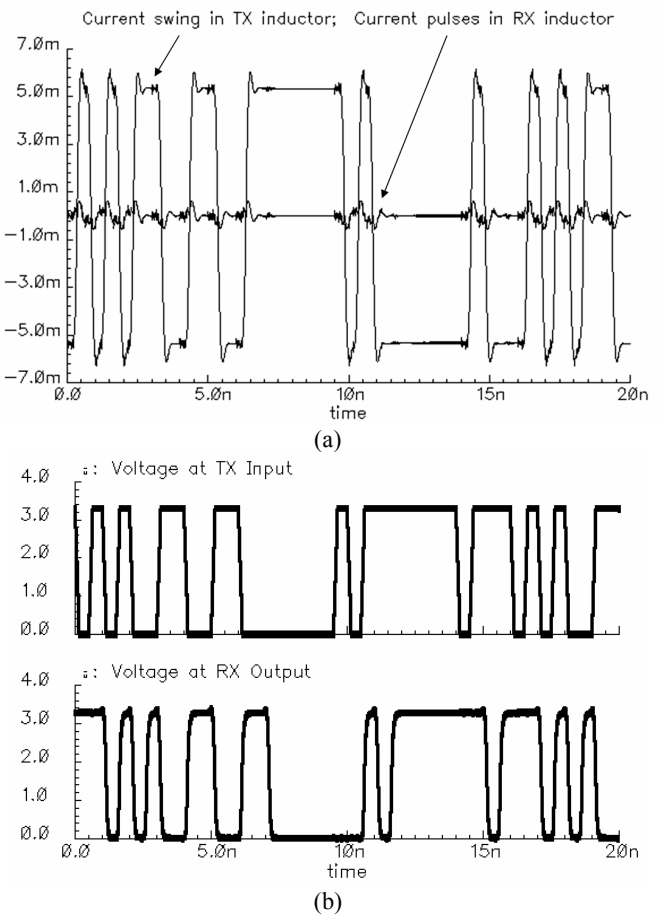

Fig. 5 Simulation results of transceiver, (a) current in the inter-chip transformer, (b) voltage at TX input and RX output.

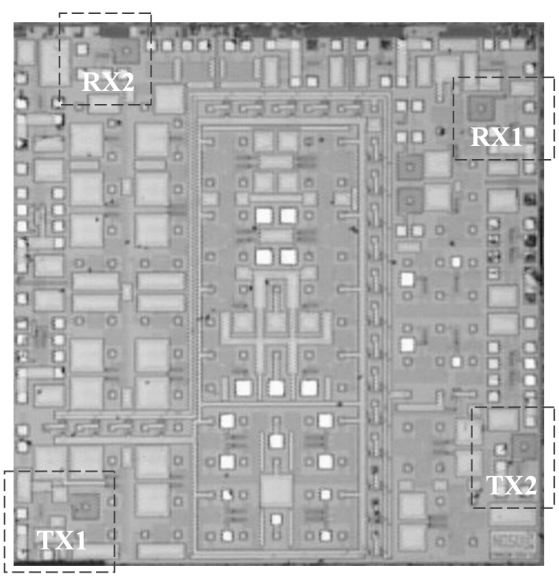

Fig. 6 Microphotograph of the test chip, 3.2mm by 3.2mm, TSMC 0.35μm CMOS process. In a two-chip stack, the top chip is rotated 90° and aligned on the bottom chip, the inductors of TX1 and RX1 on the bottom chip will overlap with the inductors of RX2 and TX2 and form two inter-chip transformers.

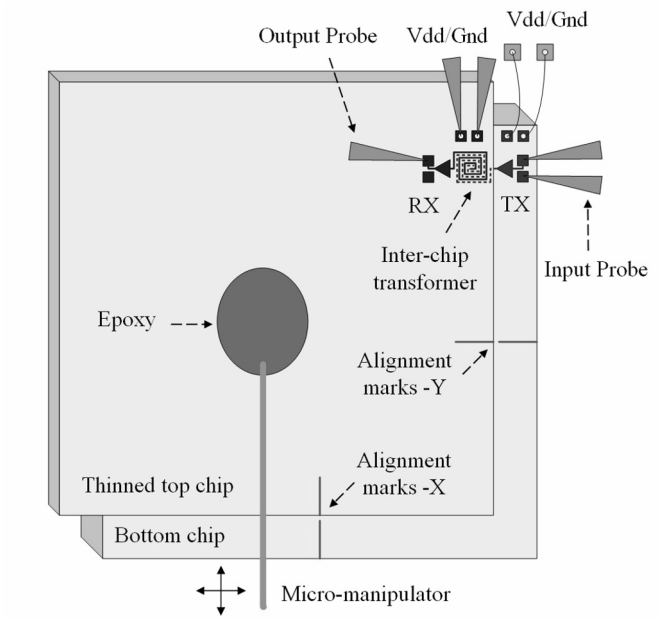

Fig. 7 A demonstration system of inductively coupled interconnect in a two-chip stack.

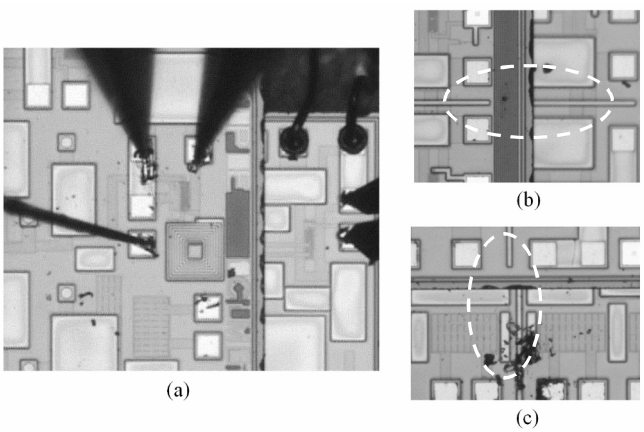

Fig. 8 Test structure for emulating 3-D ICs assembly, (a) two chips stacked, spiral inductors overlapped, (b) Alignment marks in Y direction with 0μm offset, (c) Alignment marks in X direction with 20μm offset.

B. Experiment Results

For a double layer 150μm by 150μm spiral inductor with eight turns per layer, the measured self-inductance is 27nH. An inter-chip transformer was formed by overlapping such two inductors. Measurements of this inductively coupled transceiver channel produced a maximum signaling rate of 2.8Gb/s for a 2^7-1 pseudorandom binary sequence (PRBS) when the top chip was thinned to 90μm. The accumulated eye diagram at the RX output is shown in Fig. 9. A transient waveform at the RX output for a 2.0Gb/s arbitrary data pattern is also shown in Fig. 9.

To study the dependence of the coupling coefficient on the chip thickness in 3-D ICs, the top chips were thinned to 90μm, 105μm and 120μm, and each was then stacked on the bottom chip for measurement. In the case of perfect alignment at the same data rate (2.0Gb/s), the thinner the chip, the less jitter was observed in the eye diagram at the RX output.

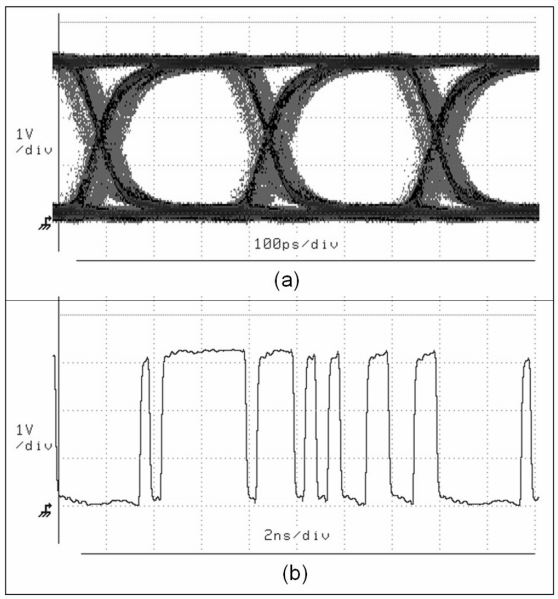

Fig. 9 Measurement results for 90μm thick test chip, (a) eye diagram at RX output, 2.8Gb/s 2^7-1 bits PRBS, (b) wave form at RX output, 2.0Gb/s arbitrary pattern.

The power dissipation for one pair of TX/RX is 47.6mW, in which the TX consumes 10.0mW and the RX consumes 37.6mW. The transceiver circuit does not require external support circuitry or a clock to recover the data and is able to maintain less than 100ps peak-to-peak jitter in the eye diagram at the RX output.

Misalignment Tolerance

The coupling coefficient determinates the strength of receiving signal at the RX input; it is not only sensitive to the vertical separation distance between two coupled inductors but it is also sensitive to the horizontal offset between them. Fig. 10 illustrates the relationship between the coupling coefficient and the horizontal offset, or misalignment, for chip thickness equal to 90μm, 105μm and 120μm, based on ASITIC simulations.

To investigate the tolerance of an inductively coupled transceiver system to the horizontal misalignment in a 3-D assembly process, measurements at arbitrary offsets between two coupled inductors in X and/or Y direction were performed. Fig. 11 shows the measured tolerance to the horizontal misalignment. To operate the transceiver system at a data rate of 2.0Gb/s with the top chip thinned to 90μm, 105μm and 120μm, the inter-chip transformer can tolerate 50μm, 20μm and 5μm misalignment in both X and Y directions, respectively.

The measurement results correlate well with the simulation results. The required minimum coupling coefficient defines a boundary between the regions of valid operation and invalid operation, for this work the minimum coupling coefficient is approximately 0.023. For instance, with 90μm chip thickness and 40μm offset, the simulated coupling coefficient is 0.028, which can be found in Fig. 10, and results in valid operation as shown in Fig. 11.

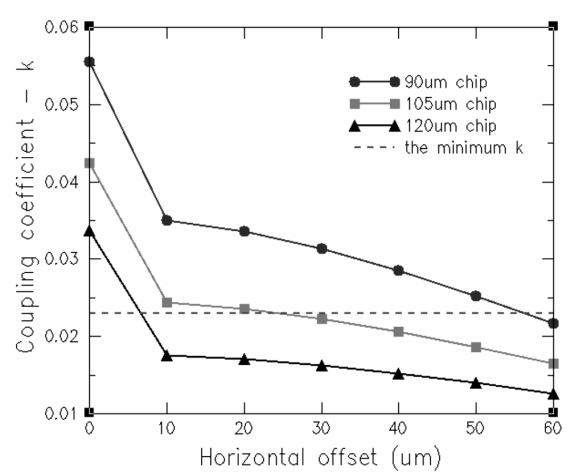

Fig. 10 Simulated (ASITIC) coupling coefficient sensitivity to horizontal offset.

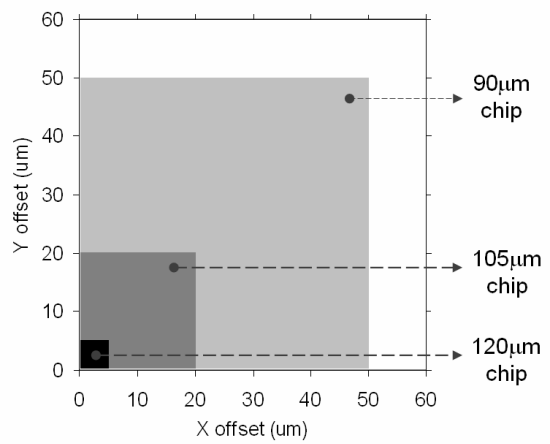

Fig. 11 Measured tolerances at 2.0Gb/s data rate, shaded regions indicate valid operation, 90μm, 105μm and 120μm represent the thickness of thinned chip.

Crosstalk

To explore the density or pitch of coupling elements, the crosstalk between neighboring inductors was measured. A crosstalk test structure is shown in Fig. 12 and the measured isolation, S_{21}, between two neighboring inductors is plotted in Fig. 13. For frequencies up to 5GHz, there is at least 40dB of isolation with 50μm of spacing between inductors, which is 1/3 of the inductor diameter.

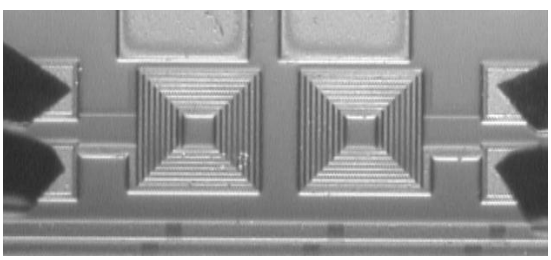

Fig. 12 Test structure to measure the crosstalk between neighboring inductors.

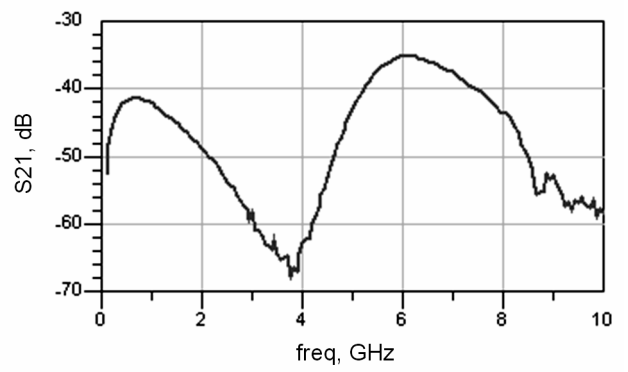

Fig. 13 Measured isolation between two neighboring inductors with a spacing of 1/3 inductor diameter, scattering parameter S_{21} represents the forward transmission coefficient.

Conclusions

A demonstration system for inductively coupled interconnects in 3-D ICs was built and tested. The inductive coupling behavior as a function of vertical separation and horizontal offset was also explored. For a 90μm thinned chip with a 150μm spiral inductor, the transceiver communicates PRBS NRZ signals at a data rate of 2.8Gb/s and tolerates up to 50μm misalignment. The transceiver circuit does not require any external support circuitry or a clock to recover the data and is able to maintain peak-to-peak jitter less than 100ps in the eye diagram at the RX output.

Acknowledgements

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