Fully Integrated AC Coupled Interconnect using Buried Bumps

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Abstract - Demonstrated is the fully integrated chip and package technology proposed in ACCI. ACCI provides power and ground distribution by using buried solder bump, and data transmission through capacitors formed between the chip and package.

INTRODUCTON

Numerous types of non-contacting, inter-chip signaling methods have been presented, such as: ACCI [1,2], proximity communication [3], and wireless superconnect (WSC) [4]. ACCI using buried solder bumps is a technology that provides a *complete solution* by integrating high-density, low inductance power and ground distribution with high-density, high-speed I/O. The mixture of solder bump technology and AC coupled I/O has the potential to improve yield during packaging and assembly since I/O channels are no longer dependent on the yield of a single solder bump. For the same reason, this technology has the potential to increase the long-term reliability of chip/carrier components of electronic systems used in harsh environments *(e.g. extreme vibration, shock, and temperature variation)*.

An illustration of the physical ACCI system with two chips mounted on a common substrate using buried solder bumps, is shown in Fig. 1. The buried solder bumps provide power and ground to the mounted chips, and are also used to self-align the AC coupling elements and control the resulting gap between the chip and substrate. The substrate uses five copper metal layers for power, ground, signal routing, and coupling element formation. Benzocyclobutene (BCB) was chosen for the dielectric layers because of its low permittivity ($\varepsilon_r \sim 2.65$) and excellent planarizing properties.

The key concept here is that DC connections are not needed to convey the high frequency content of AC signals. Instead, the information in these signals can be coupled via "AC connections", such as a series capacitor. The advantage of AC connections is that circuit design considerations can be made the limiting factor to achieving high I/O density rather than physical limitations such as the manufacturability of dense arrays of sub-100μm solder bumps. The buried solder bump has two purposes. First, the buried bumps provide DC connections (e.g. for power and ground) across the interface. Second, the buried bumps provide a means to self-align the chip and package surfaces while maintaining a close and controlled proximity between corresponding capacitor plates. This creates AC and DC paths are simultaneously created across the same interface between chip and package.

Fig. 2 shows the ACCI equivalent circuit for the system. It includes the transmitter and receiver chip, and the substrate with a 5.6cm long 50Ω microstrip line. The capacitive coupling element is formed between the top metal layer on the substrate and the top metal layer on the CMOS chip. The conformal, 1.7μm thick glass from fabrication is left as-is covering the portion of the capacitive element on the CMOS chip. The corresponding portion of the capacitive element on the substrate is not covered by a dielectric. The capacitor plate size for this work is 200μm x 200μm *(i.e. a 270fF coupling capacitance for a 1μm air gap between capacitor plates)*, and this element could be used for I/O pitches just above 200μm, because of the comparatively low lateral coupling. Scaling to a 0.18μm circuit technology allows the coupling capacitor to be reduced too less than 80μm x 80μm.

SUBSTRATE WITH BURIED BUMPS

To demonstrate ACCI with buried bumps, a multi-metal layer substrate was design and fabricated at MCNC-RDI. The substrate was manufactured using a silicon wafer with five copper interconnect layers, each 2μm thick, and four BCB dielectric layers, of varying thickness. An illustration, of the substrate stack-up showing the thickness of each dielectric layer is shown in Fig. 3. The lower two metal layers (M1 & M2) were used for power and ground distribution, as references planes, and to form the contacting layers for the buried bumps. The two metal layers (M3 & M4) embedded in dielectric were used for the routing of transmission lines (T-lines) and the top metal layer (M5) was mainly used to form the AC I/O structures. In some situations, the top metal layer was also used to create low-loss micro-strip lines for long runs across the substrate, and also as a reference plane to form a strip lines using M3. That is, when chips are flipped onto the surface of the substrate (thereby realizing a complete ACCI system), their close proximity between chip and substrate changes the impedance of embedded micro-strip lines passing below. If large die are attached to the substrate where long T-lines are routed, it is necessary to form strip lines beneath the die to maintain predictable and controlled impedance.

Fig. 4 shows the cross section of an assembled substrate and CMOS chip. Coupling capacitors formed by the substrate and chip interface can be seen between the buried bumps. From the images in the Fig. 4 it can be seen that there is slight misalignment in coupling elements (~5μm). Misalignment in this case is due to the fact that the chips and substrates were deliberately brought into contact and friction at the interface prevented the solder bumps from self-aligning. This intimate contact resulted in a separation between the chip and substrate capacitor plates of approximately 1μm and was chosen so that the performance at minimum separation could be established. By controlling the solder ball volume and re-flow parameters, any specific gap distance can be achieved. The capacitor shown in Fig. 4 is smaller than that used in this demonstration.

The ACCI system can be scaled to interconnect multiple ICs. Shown in Fig. 5 is a photograph of an assembled substrate populated with two CMOS ICs and eight decoupling capacitors. The substrate has two chips mounted, but can accommodate up to four chips and includes eight sites for C4 solder ball style de-coupling capacitors (two per chip). Fig. 5 also shows a die photo of the TSMC 0.35μm CMOS chips used in this system demonstration and a zoomed in view of a mounting site for the IC on the substrate. The zoomed in view shows solder bump trenches that are 30μm deep, and plates corresponding to the capacitive AC coupling elements on the surface of the substrate. The substrate is 25mm x 12.5mm and each chip is 3.2mm x 3.2mm.

CHANNEL RESPONSE, PULSE SIGNALING & EQUALIZATION

Instead of the low-pass response of a traditional T-line channel, in ACCI, the combination of series coupling capacitors, shunting parasitic capacitors, and transmission line create a channel, from transmitter (TX) to receiver (RX), with a band-pass response. The T-line and parasitic capacitors define the low-pass response, while the coupling capacitors define the high-pass response of the ACCI channel. To reduce reflections, one or both sides of the T-line should be terminated. Terminating at one side of the T-line instead of both produces an increase in the received signal, at the expense of reflections on the T-line.

The main difference in signaling through an ACCI channel verses a traditional T-line channel is the use of pulse signaling. The first coupling capacitor in the ACCI channel converts a binary NRZ signal into a ternary NRZ signal. This conversion comes from the differentiation that occurs due to the high-pass characteristic of the series capacitive coupling. When using ternary NRZ signaling, the intermediate state denotes a continuation of the previous full swing logic state [5]. In more detail, first consider that the full swing transmitter produces a step input to the ACCI channel. The first series coupling capacitor differentiates this edge and produces a pulse that propagates on the T -line. The T-line has a low-pass response due to the skin effect and dielectric loss, causing dispersion, which "smears" the signal into neighboring bit periods. Without equalization, this dispersion will cause ISI and reduce the timing margin at the receiver. The second coupling capacitor de-emphasizes the low frequency components by filtering the long pulse tail, thereby, reducing energy that interferes with adjacent pulses. This allows ACCI to save chip area and reduce power dissipation typically associated with active high frequency equalization.

The pulse amplitude and width, at the receiver, are determined by the coupling capacitors, T-line characteristics, and the edge rate and amplitude of the transmitted step. For a given data rate and pulse receiver input sensitivity, there is a range of coupling capacitor sizes and T-line lengths, within which a pulse receiver is able to recover the data. These limits, along with the require interconnect length and AC I/O density; determine the design space for a given chip and interconnect technology. Fig. 6 shows the differential pulse eye diagram after the second coupling capacitor (i.e. at the receiver input). The arrows show the trend resulting from increasing the coupling capacitor size. Larger coupling capacitors will increase the peak-to-peak swing and duration of the pulse. The increased swing relaxes the constraint on the receiver input sensitivity, but the increased pulse width may introduce ISI. However, a smaller coupling capacitor is more efficient at filtering the pulse signal tail and mitigating ISI, but the corresponding reduction in signal swing increases the input sensitivity requirement for the receiver. Therefore, the maximum coupling capacitance is constrained by the ISI limit, or the data period limit, while the minimum coupling capacitance is constrained by the swing limit, or receiver input sensitivity. *(From the simulation results shown in Fig. 6, it can be seen that the limiting factor in this demonstration was the 0.35μm CMOS technology. Simulations show that if a 0.18μm CMOS technology is used, then signaling rates in excess of 5Gb/s can be achieved using the same channel.)*

The band-pass characteristic of ACCI channels uses a different equalization scheme than that used with traditional T-line channels. High frequency compensation used in traditional T-line channels is not required in ACCI. However, low frequency compensation is necessary. The critical components of the system and their corresponding frequency responses are shown in Fig. 7. The receiver is essentially a latch or edge detector and is used to compensate for all low frequency attenuation. It effectively flattens the frequency response of the channel. Its response is similar to that of an integrator. The latch detects and captures pulses, and remains stable until detecting the next opposite polarity pulse in the NRZ data stream; thereby, implementing an adaptive low frequency compensator. As long as the pulse data rate is less than the latch bandwidth, the low frequency compensation dynamically adapts to changes in pulse width caused by the T-line and coupling capacitor variations. Furthermore, as long as the NRZ signal edge rate has enough energy in the pass band of the ACCI channel, any digital signal can pass the ACCI channel and be recovered by the pulse receiver. Theoretically, this corresponds to a digital signal with a data rate approaching DC. This also explains how the latch-based pulse receiver can recover long consecutive "1" or "0"s. The T-line also affects channel response and pulse shape. Longer T-lines result in more attenuation, especially high frequency attenuation. This not only extends pulse width (increasing ISI) but also limits pulse swing. Thus, the maximum T-line length is constrained by both the ISI limit and swing limit.

TRANSCEIVER CIRCUITS & MEASURED RESULTS

Elaborate circuits are not needed to demonstrate ACCI technology. Instead, as shown in Fig. 8, an inverter chain can be used for data transmission, and a self-biased inverter and latch structure can be used for the receiver circuit. The transmitter and receiver circuits used in this work do not require any clocking to transmit or receive the incoming data stream. Very similar receiver circuits have been demonstrated for single-ended capacitively coupled signaling [6], and more complex receivers have been demonstrated for differential signaling [2,7].

For testing, two CMOS chips were mounted to a substrate, as shown previously in Fig. 5, and to facilitate measurements this system was then mounted to a PCB. Although both CMOS ICs are identical, only the transmitter circuits were used on one IC to drive data through the channel, and only the receiver circuits on the other IC were used to recover data from the channel. Input data was provided by a PRBS source and output data was measured using a digital sampling oscilloscope using a high-impedance active probe. Two transmitters on the TX chip were driven by separate channels from the PRBS source at 2.5Gb/s/channel for a total throughput of 5Gb/s, across two 5.6cm long meandering 50Ω microstrip lines on the substrate. At 3.3V Vdd, the transmitter consumed 10.3mW and the receiver consumed 15.0mW, for a total power of 25.3mW, at 2.5Gb/s/channel. Table I summarizes system specifications and performance.

Fig. 9 shows the measured output of the RX chip for both a 32-bit arbitrary data pattern and PRBS (2^7-1) data on channel-1, while channel-2 transmits and receives PRBS (2^7-1) data. Each channel operates without error in the presence of power supply noise from the adjacent channel. The peak-to-peak jitter on the PRBS data of channel-1 is less than 120ps. Bit error rate (BER) measurements of the system at 2.5Gb/s/channel are better than 10^{-12}.

CONLUSION

Though similar "capacitively coupled interconnect" schemes have been presented, they lack a solution for providing robust power and ground distribution that is also compatible with current manufacturing methods [2,3]. This technology demonstrates a complete solution for high-density, high-speed I/O and high-density, low inductance power and ground distribution by using buried solder bumps and ACCI. It also has the potential to improve yield during packaging and assembly since I/O channels are no longer dependent on the yield of a single solder bump. Measurements and simulation results show that the limiting factor for this demonstration was the 0.35µm CMOS technology, not the AC coupled interconnect. Simulations show that if a 0.18µm CMOS technology is used, then signaling rates in excess of 5Gb/s can be achieved.

ACKNOWLEDGEMENT

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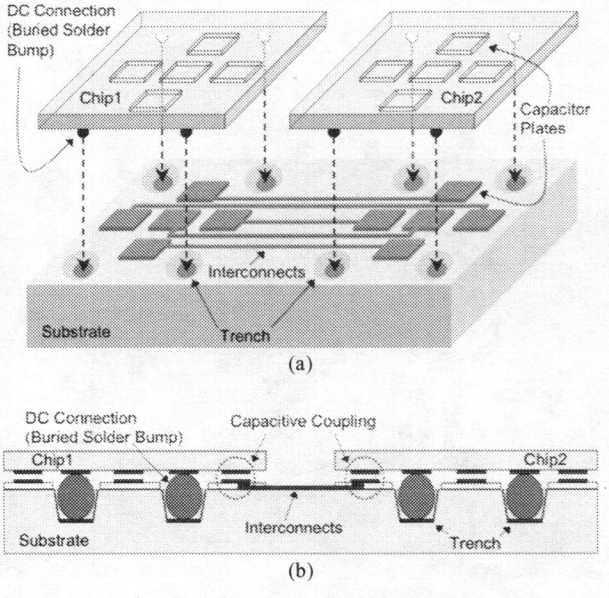

Fig. 1. ACCI Physical Structure: (a) "3-D" view, (b) cross sectional view

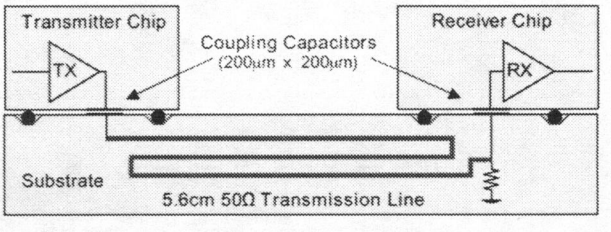

Fig. 2. ACCI Demonstration System

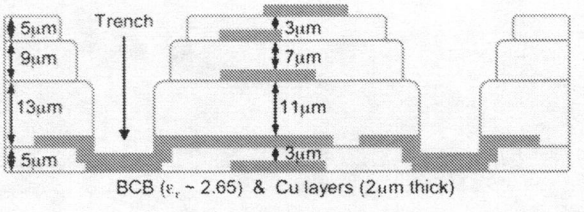

Fig. 3. Five metal layer substrate stack-up with trenches for buried bumps

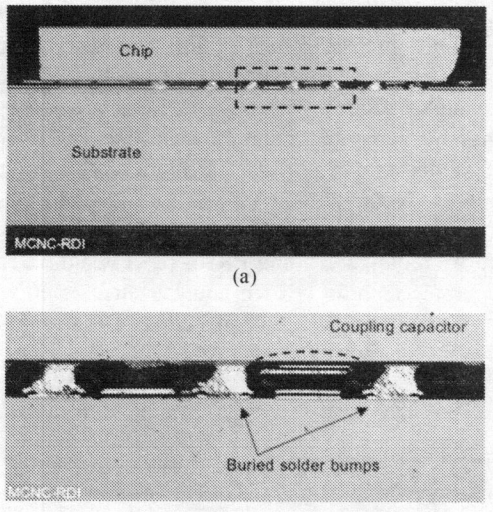

Fig . 4. Cross sectional views: (a) substrate & chip, (b) buried bumps & coupling capacitor

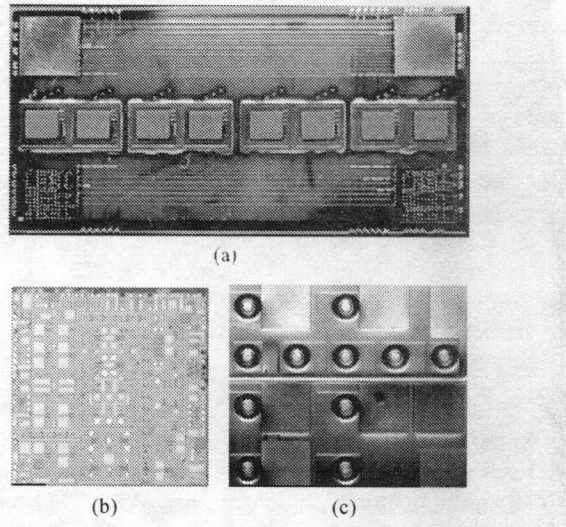

Fig. 5. ACCI system: (a) assembled MCM, (b) chip, (c) trenches & AC I/O

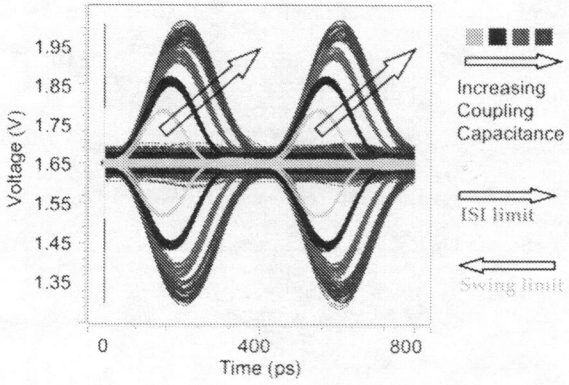

Fig. 6. Pulse eye diagram for increasing coupling capacitance

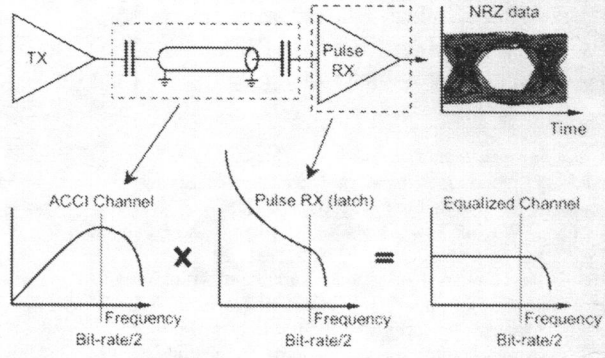

Fig. 7. Frequency domain equalization scheme for pulse signaling in ACCI

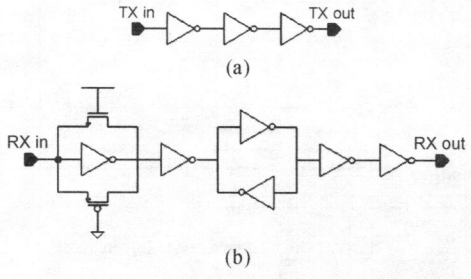

Fig. 8. Circuits for ACCI system demonstration: (a) transmitter, (b)

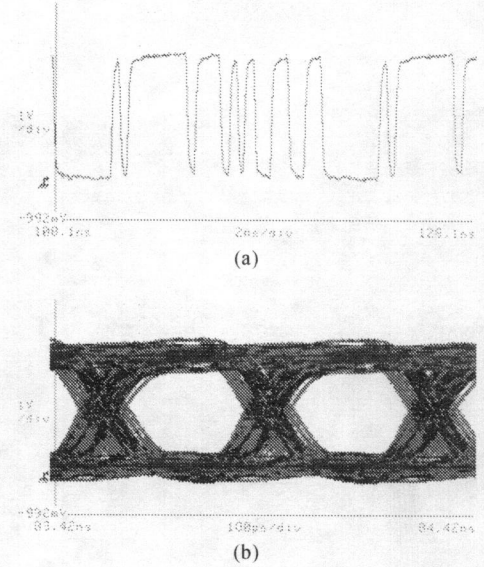

Fig. 9. Measured output for two channels operating at 2.5Gb/s/channel: (a) 32 bit arbitrary pattern, (b) PRBS eye diagram (2^7-1)

Table I
Performance Summary

Supply Voltage	3.3V
Technology	0.35μm CMOS & MCM-D
Data Rate	2.5Gb/s/channel
Interconnect Length	5.6cm
Power Dissipation (TX)	10.3mW
Power Dissipation (RX)	15.0mW
Bit Error Rate (BER)	Better than 10^{-12}