A New Method to Achieve Improved Accuracy with IBIS Models

Ambrish Varma, Michael Steer, Paul Franzon
ECE, Box 7914, NCSU, Raleigh NC 27695
Ph - 919 515 7351, fax – 919 515 2285
{akvarma, mbs, paulf}@ncsu.edu

Abstract:

IBIS (Input/Output Buffer Information Specification) models are known to lack information regarding power and ground bounce [1][2] resulting in incorrect simulations. In this paper, a novel solution to the problem is proposed making it possible to simulate IBIS models with available simulators and have a realistic chance at simulating Simultaneous Switching Noise (SSN) that are present in most if not all high speed circuits. To demonstrate the solution, a CMOS voltage-mode driver circuit and a current- mode LVDS driver circuit are simulated using HSPICE and compared with equivalent circuits created with IBIS models of the same drivers. The IBIS models are created using the s2ibis tool from North Carolina State University [3].

1. Introduction

IBIS models have become popular with system and circuit designers as they are fast compared to transistor level models and do not disclose propriety information to the end user. As they gain in popularity, a thorough analysis is needed to figure out what IBIS is capable of, where it falls short and what can be done to address the issues. One such issue is the simultaneous switching noise (SSN), also known as ground bounce, or simultaneous switching output (SSO). This paper proposes a solution to adequately represent SSN without changing the method of creating an IBIS model. This is important as to propose a change in the way the model is created would mean not just effort to convince the IBIS committee on the benefits of making a change to the model, but also time as any change to the modeling methodology typically takes months before it is either accepted or rejected.

SPICE and IBIS modeled drivers are compared for simultaneous switching noise in section 2. A new method of accommodating SSN information in circuits that use IBIS models is presented in 3. Section 4 includes results of simulation of the new technique on voltage mode and current mode drivers. Section 5 discusses future direction of research and concludes the paper.

2. Comparing SPICE and IBIS

IBIS is a widely used standard in the industry (EIA standard 656 -A) to model different kinds of I/O buffers. IBIS models cater to the need for fast, accurate models of Integrated Circuit drivers and receivers for board level simulations. These models are purely behavioral i.e. they describe the behavior of the drivers from a high level and do not contain low level circuit information. This behavior of the drivers is contained in the V-I and V-T tables. IBIS models are thus fast, accurate and do not reveal any proprietary information contained in the IC.

To test how simultaneous switching noise is represented in IBIS, a test involving 4 cascaded non-inverting voltage mode drivers is setup as shown in figure 1.

These drivers use the same power – ground plane through LC circuits that models the power and ground plane parasitics as well as pin - package parasitics. The drivers are connected to 50 ohm ideal (lossless) transmission line and terminated with 50 ohms resistors. Simultaneous switching inputs were applied on 3 drivers and the fourth driver is connected to ground to simulate a quite line.

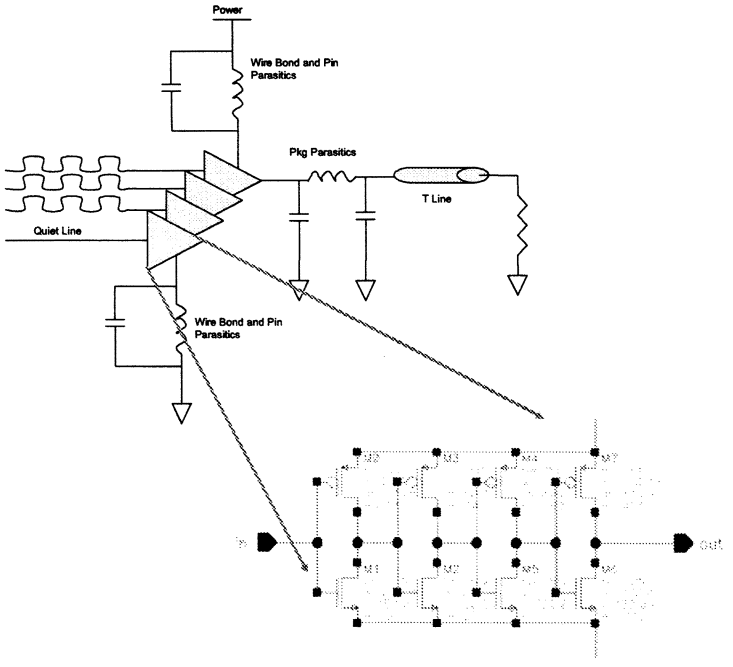
One of the four identical drivers is now converted to an IBIS model using SPICE to IBIS (S2IBIS3[1]). This model is then read back in SPICE using the B element in HSPICE.

HSPICE has provisions to distribute the silicon die capacitance (C_Comp) into all the nodes of the model. This is usually done to simulate power and ground bounce more accurately but is not implemented in this test as it is tool dependant and not available in all IBIS simulators. An identical circuit is constructed using the model as the driver and simultaneously switching signals are applied to three drivers while the fourth driver is grounded.

SPICE simulation show that while the first three driver show expected non-inverting output, the fourth driver has noise. This noise is di/dt noise that is present in the plane due to multiple drivers switching simultaneously. Due to this switching, V_{ss} rises and V_{dd} droops resulting in changed I/V characteristics [4].

[1] S2IBIS is a tool that uses a SPICE netlist of an I/O buffer and generates its IBIS model [3].

In the circuit with IBIS driver, similar results are observed on the 3 drivers with signals, the quiet line does show significant noise.



It should be pointed out that the representation of SSN/SSO noise is not accurate as IBIS overestimates the noise when compared to SPICE simulations. This result is not surprising as IBIS does not model the well known "feedback effect," in which the collapsing voltage rails reduce driver di/dt. An IBIS model has V-I table that is extracted for a single gate voltage inside the driver. With varying power/ground voltages due to noise, the gate voltage varies as well, hence producing a different characteristic curve for the device in the driver. While this effect is captured in HSPICE simulation of the driver netlist, the IBIS simulation solely depends on the one V-I table that is provided in the model. The consequences of this worst case scenario representation could severely restrict a designer's options when designing with IBIS models.

Figure 1: Test setup to compare IBIS and SPICE. 3 buffers are given simultaneously switching inputs and the 4th input is grounded.

3. A Solution for better SSN Representation

With the knowledge of why SSN is not represented properly while using IBIS models, a new method is proposed that would help the designer include SSN information in the circuit with IBIS models representing the drivers and receivers. This method does not involve modifying the IBIS modeling methodology nor is it a part of S2IBIS tool, but complements the IBIS driver as a separate subcircuit that users would add in conjunction to the B element in their circuit. The subcircuit consists of three separate Voltage Controlled Capacitances (VCCAPs) that are placed between the power and ground rails, the output and the power rail and the output and the ground rail (figure 2). These VCCAPs are a function of the power and ground voltages and the output voltage respectively. Capacitance across nodes varies linearly between a desired range depending upon the voltage across the control nodes [5]. By providing voltage controlled capacitances, more coupling is achieved between the power and ground power voltage levels with the output voltage level. Depending upon the circuit, the designer can choose to base the capacitances on one of three available nodes. An ideal situation would be to compile a library of drivers and the best combination of VCCAPs that would work with that circuit. This way, the designer would not have to play around with various permutations and combinations to arrive at the best result.

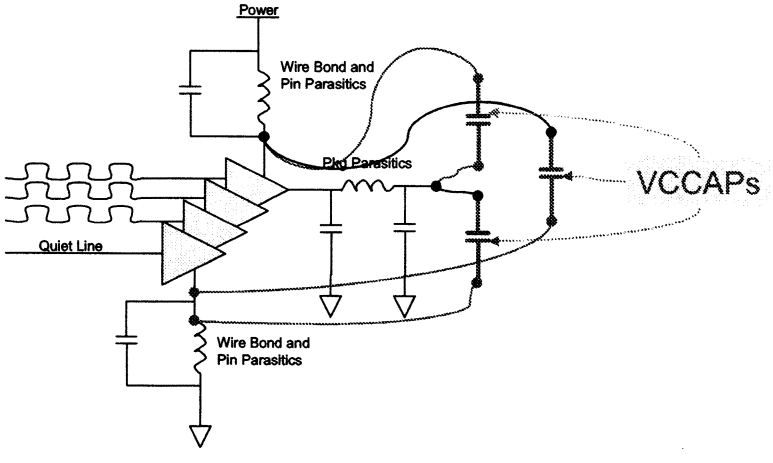


Figure 2: VCCAP Circuit that is attached to IBIS circuit.

4. Simulation Results

Figures 3 and 4 show the simulation result for the voltage mode cascaded CMOS drivers. Figure 3 shows the ground and power signals of the HSPICE simulations and the plain IBIS model (Top) and the same HSPICE simulations and the enhanced circuit of VCCAPs that complements the IBIS model. Figure 4 shows output from a switching driver (left) and a quiet driver (right). The values of the VCCAPs used are in the range of 0.5 pF to 5pF.

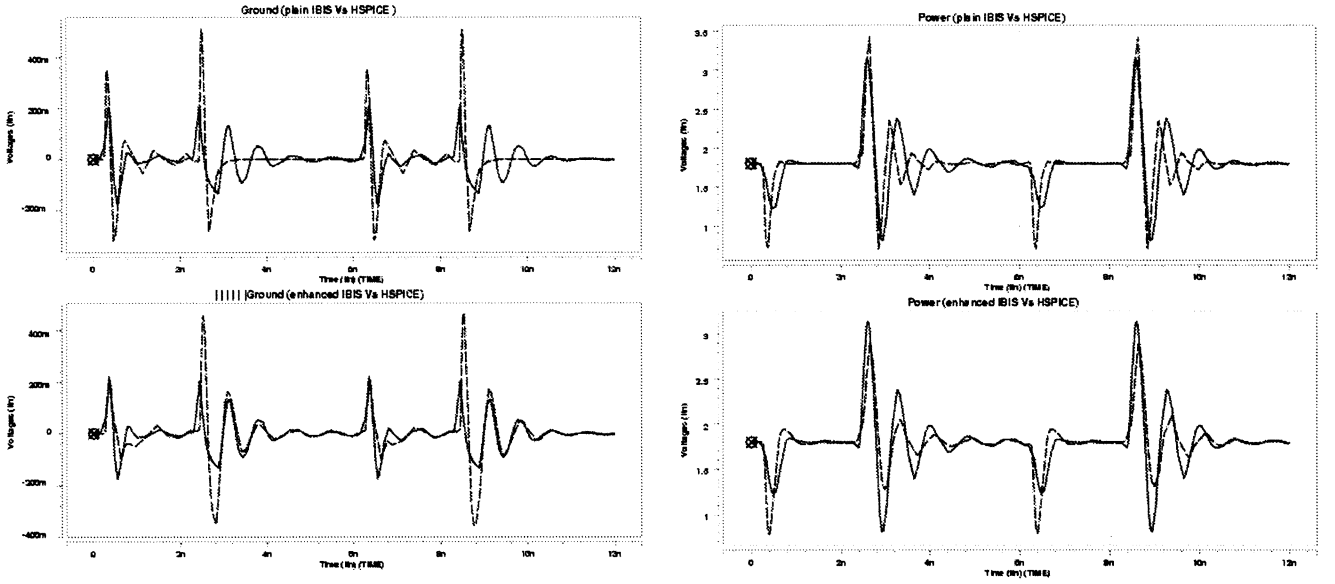


Figure 3: Ground (left) and Power (right) for IBIS without enhancements (top) and with enhancements (bottom). HSPICE signal is solid while IBIS signals are dotted.

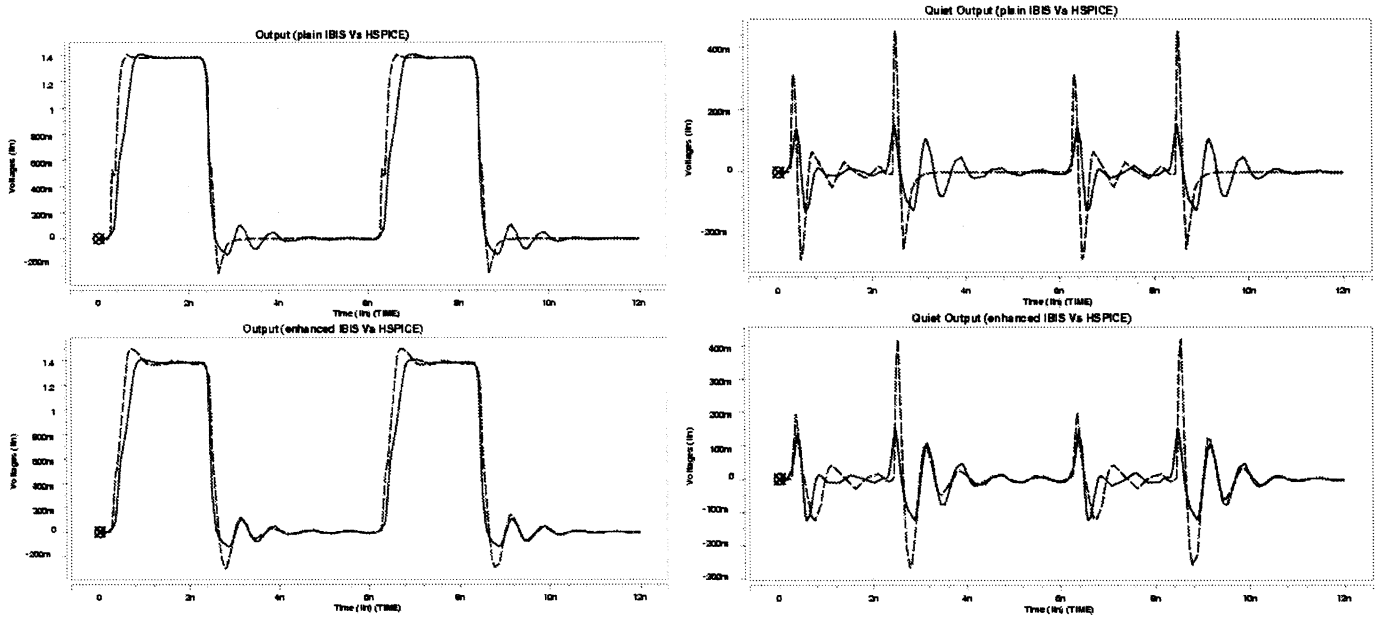


Figure 4: Switching (left) and Quiet Output (right) for IBIS without enhancements (top) and with enhancements (bottom). HSPICE signal is solid while IBIS signals are dotted.

Similar results were obtained with a Low Voltage Differential Signal (LVDS) driver. The LVDS driver was designed as described in [6] with a simplified compensation and closed loop controlled circuit. IBIS models of the LVDS drivers were obtained using the method described in [7]. Figure 5 shows the ground signal (left) and the output from one of the differential pins (right). The top portion of the figure compares the plain IBIS Vs HSPICE while the bottom portion compares the enhanced version of IBIS compared with HSPICE. Adjusting voltage controlled capacitances in this case is slightly more difficult and accurate results harder to achieve because current mode drivers are differential and have a limited tail current,

hence instead of having a spike of current when the drivers switch, the current stays relatively constant throughout. Even though SSN is low in general, simulations have shown improvements in model performances.

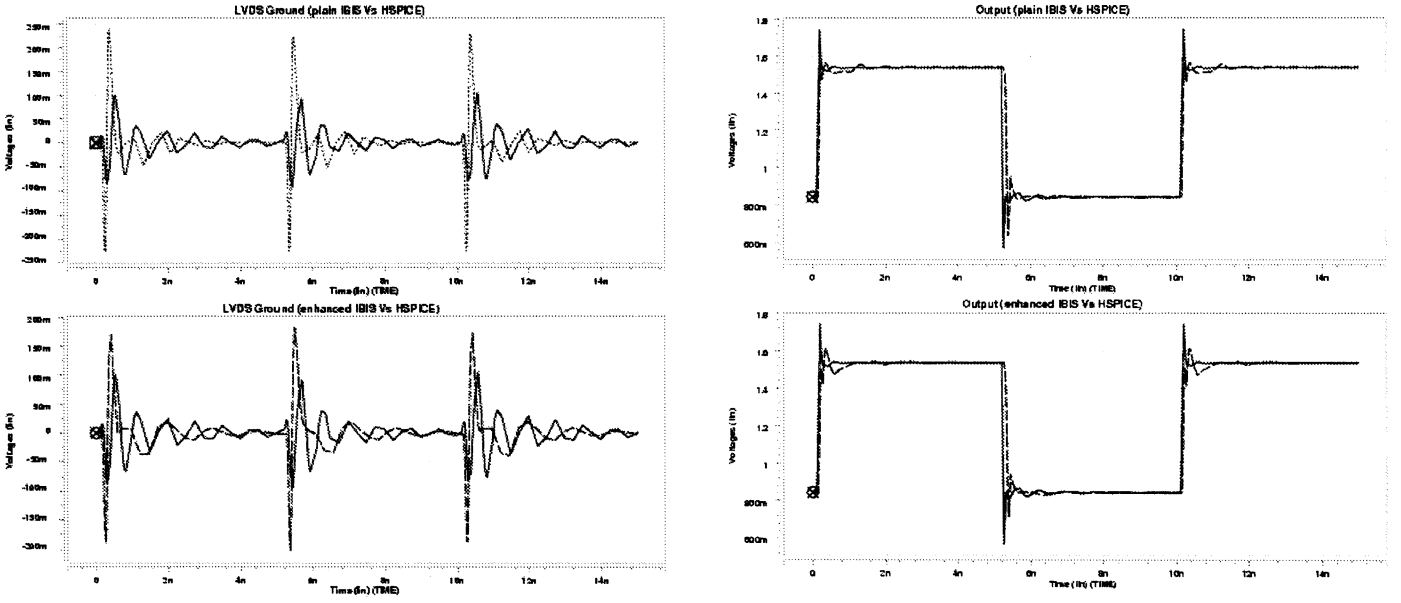


Figure 5: Ground signal (left) and Output signal (right) from one of the differential pins of an LVDS driver. The top compared plain IBIS Vs HSPICE and the bottom compares the the enhanced IBIS Vs HSPICE. HSPICE signal is solid while IBIS signals are dotted.

5. Future Work and Conclusion

As shown in this paper, an IBIS model can be complemented to produce more accurate results by providing SSN information that is present in high speed simulations. On an average, circuits with VCCAPS have a mean square error that is 15 to 20% lower when compared with hspice circuits than circuits without VCCAPS. The difference is slightly lower when comparing current mode drivers because of reason discussed above.

The authors consider this to be a first step and a stepping stone to a more versatile and better defined black box type approach that could be fitted to any driver structure and any kind of model. By tweaking certain parameters, the black box could be molded for any given model.

Acknowledgments:

The authors would like to thank engineers at Cadence Design Systems, Inc at Chelmsford, MA and Paul Fernando of NCSU for valuable discussions.

References

[1] "SSN issues with IBIS models" *Varma, A.; Steer, M.; Franzon, P.*; Electrical Performance of Electronic Packaging, 25-27 Oct. 2004.

[2] Adding On-Chip Capacitance in IBIS Format for SSO Simulations. *Raymond Y. Chen* DesignCon 2004 - IBIS Summit.

[3] "The Development of a Macro-modeling Tool to Develop IBIS Models," *Ambrish Varma, Alan Glaser, Steve Lipa, Michael Steer, Paul Franzon*, 12th Tropical Meeting on Electrical Performance of Electronic Packaging (EPEP 2003), Princeton, New Jersey, pp. 277-280, October, 2003.

[4] Simultaneous Switching Noise of CMOS Devices and Systems. *Ramesh Senthinathan and John L. Prince.* Kluwer Academic Publishers, 1994.

[5] Avanti, Star-HSpice manual Release 2001.2.

[6] "LVDS I/O Interface for Gb/s-per-Pin Operation in 0.35-_m CMOS". *Andrea Boni, Andrea Pierazzi, and Davide Vecchi*, IEEE Journal Of Solid-State Circuits, Vol. 36, No. 4, April 2001

[7] "Details on True Differential Buffer Characterization Revisited". *Arpad Muranyi*, IBIS Summit at PCB Conference East Westford, MA October 21, 2003.