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Fabrication of wafer scale, aligned sub-25 nm nanowire and nanowire templates using planar edge defined alternate layer process

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Abstract

We have demonstrated a new planar edge defined alternate layer (PEDAL) process to make sub-25 nm nanowires across the whole wafer. The PEDAL process is useful in the fabrication of metal nanowires directly onto the wafer by shadow metallization and has the ability to fabricate sub-10 nm nanowires with 20 nm pitch. The process can also be used to make templates for the nano-imprinting with which the crossbar structures can be fabricated. The process involves defining the edge by etching a trench patterned by conventional i-line lithography, followed by deposition of alternating layers of silicon nitride and crystallized a-Si. The thickness of these layers determines the width and spacing of the nanowires. Later the stack is planarized to the edge of the trench by spinning polymer Shipley 1813 and then dry etching the polymer, nitride and polysilicon stack with non-selective RIE etch recipe. Selective wet etch of either nitride or polysilicon gives us the array of an aligned nanowires template. After shadow metallization of the required metal, we get metal nanowires on the wafer. The process has the flexibility of routing the nanowires around the logic and memory modules all across the wafer. The fabrication facilities required for the process are readily available and this process provides the great alternative to existing slow and/or costly nanowire patterning techniques.
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I. Introduction

In microelectronics where the critical dimensions of interconnects shrink with the continuous trend to downscale the size of semiconductor devices such as IC and memory cells, nanowires present an important application. There are various methods for fabricating patterned nanowires, but organizing these wires into highly ordered arrays with predetermined spacing and registry has been extremely challenging [1,2]. The methods to fabricate nanowires are (1) lithography with photons in UV, DUV, EUV and X-ray spectrum; (2) lithography using electron particles, ions and neutral atoms; (3) machining using AFM, STM, NSOM; (4) replication against masters (or molds) via physical contact printing, molding and embossing; (5) self-assembly by using surfactant systems, block copolymers, crystallization of proteins and colloids; (6) spacer formation, controlled deposition and size reduction, which involves deposition on cleaved edges, or oxidation, followed by anisotropic etching forming spacers. These processes also include techniques like shadowed/oblique evaporation on surface through a mask; (7) isotropic deformation processes by the compression of elastomeric masters or molds; (8) SNAP process involving multiple epitaxial growth of alternate material and using the cross-section of such a stack as a nanowire template. Then the metal layer deposited on the template is transferred on the wafer by adhesives. Each of these methods has some basic intrinsic limitations. In recent years, much research has been done to overcome the limitations of these processes, to achieve sub-50 nm features. In photon and particle-based lithography, by using nonlinear resists, near-field phase shifting or topographically directed technology, it has been possible to achieve sub-50 nm feature. For example, EBL has demonstrated the ability to achieve 20 nm width nanowires with 60 nm pitch [3]. Pitch is often limited by the lift-off process. Extreme ultraviolet light (EUV) lithography has generated 38 nm patterns [4], and recently with the use of a Leica e-beam, it was possible to fabricate 20 nm features [5]. High cost, limited availability, low throughput and uniformity are still major issues with this serial nanowire patterning technology. In microcontact printing [6], micromolding [7,8], embossing and nano-imprinting techniques [9,10], issues limited by van der Waals forces, speed of capillary filling and adhesion of mold and replica are overcome by using low-viscosity solutions and surface modification. Step and Flash technology has demonstrated the ability to imprint sub-20 nm features [11]. Although such methods may translate the serial method of EBL/EUV into a parallel patterning process, the mold formation still depends on EBL/EUV and its use restricted by the high cost of molds. In self-assembly techniques, defect density and control over order of block copolymers, proteins and colloids are major limitations. Dip-pen lithography has demonstrated 50 nm nanowires functionalized with oligonucleotides [12]. However, the pitch and length is limited by mechanical movement of the pen or the wafer. Ability to fabricate only one wafer at time and slow processing speed of this technology has limited its usability for batch manufacturing. Although size-reduction lithography has demonstrated 7 nm wide wires, its pitch is usually >100 nm [13–15]. Low flexibility of patterning and low reproducibility has seriously restricted the use of this process. The SNAP process, which is similar to nano-imprinting but without lift-off, has demonstrated 8 nm nanowires with 16 nm pitch [16]. However, the template is formed on the edge of the wafer and its usability for the wafer scale nanowire structure and the alignment with previous layers of processing is yet to be demonstrated. This process can only make crossbar circuits and routability of nanowires is not possible. We have demonstrated in our current effort a challenging “planar edge defined alternate layer (PEDAL)” process, which can be developed into more reliable technology to be used for wafer scale batch manufacturing of sub-10 nm nanowire templates. These templates can be used for wafer scale nano-imprinting or for shadow metallization of the required metal directly onto the wafer.

2. Overview of concept

The PEDAL process involves defining the path and location of nanowires by etching a trench

directly in the silicon wafer, or in the layer deposited on the silicon wafer. As shown in Fig. 1(a), 5000 Å polysilicon is deposited, and a trench is etched into it by anisotropic dry etch. After defining the trench, alternate layers of silicon nitride and crystallized amorphous silicon are deposited conformally on the wafer as shown in Fig. 1(b). As discussed later in the paper, the step angle and conformality of the LPCVD process is critical in defining the shape of the nanowires. The

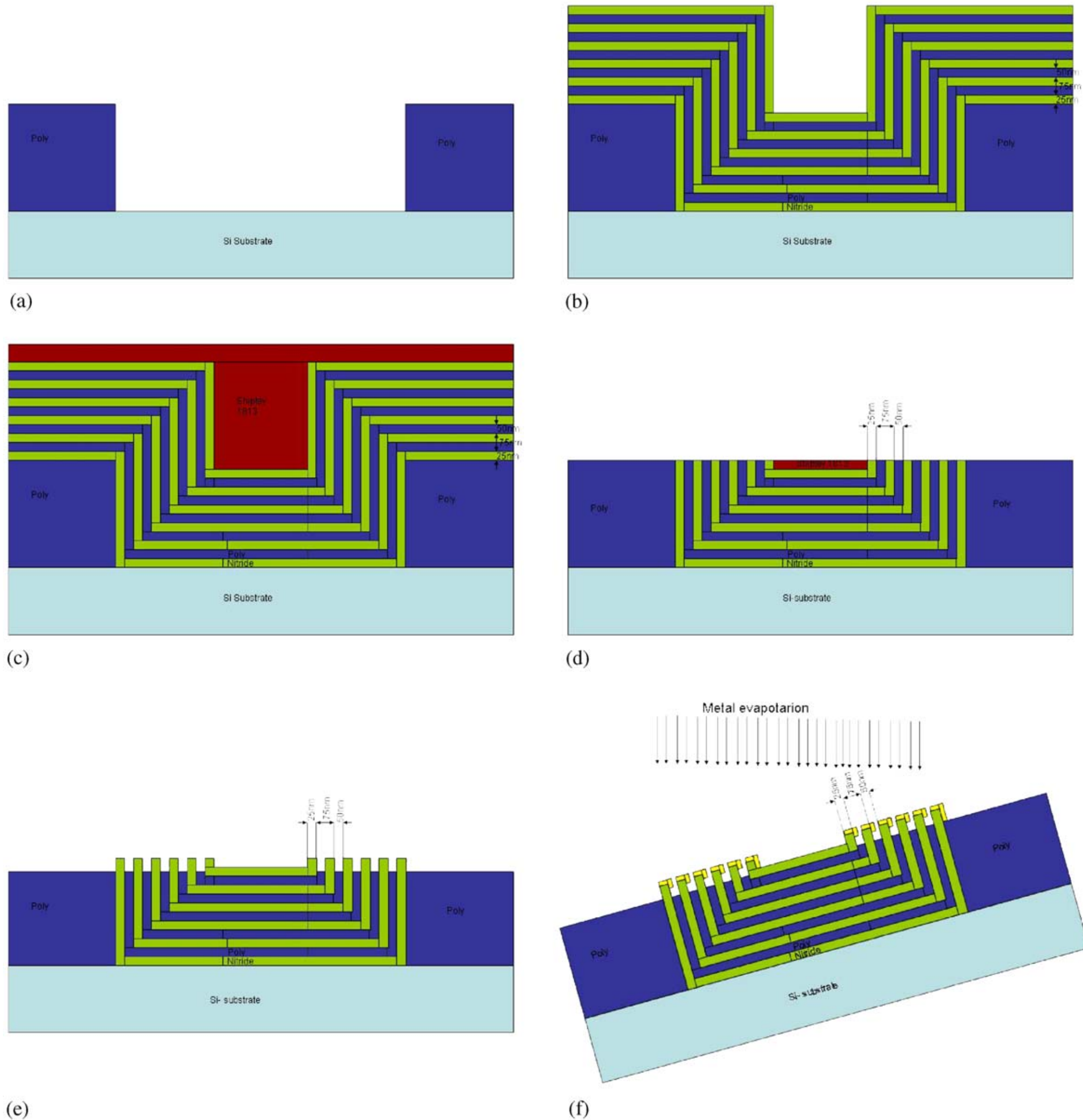

Fig. 1. Process diagram for fabrication of nanowire template using PEDAL process: (a) trench of dimensions varying from 1 to 3 μm is etched in polysilicon, (b) alternate layers of silicon nitride and a-Si are deposited by LPCVD, (c) Shipley 1813 organic polymer is spun on wafer, (d) planarization of polymer, silicon nitride and polysilicon stack by RIE, (e) polymer strip and selective wet etch of polysilicon layer, (f) oblique metallization on the nanowire template.

wafer is spin coated with polymer as shown in Fig. 1(c). The etch process which is nonselective over silicon nitride, crystallized amorphous silicon and polymer is used to planarize the wafer surface to the edge of the trench as shown in Fig. 1(d). The nanowires are defined by a etching either of the deposited material by highly selective etch recipe over the other deposited material as shown in Fig. 1(e). This gives the template which can be used for nano-imprinting. To define nanowires directly on the wafer, shadow metallization of required metal is done on the wafer as shown in Fig. 1(f).

3. Experiment

All the fabrication was done on p-type ⟨1 0 0⟩ silicon wafer. The wafers were precleaned by soaking in acetone and methanol solution for 10 min each. The wafers were then cleaned with JTB-111 solution for 10 min followed by DI water rinse. Thermal oxide 30 Å thick was grown on the wafer at 800 °C. Some of the SiO_2 layer so prepared was slightly etched back in 1% HF solution for 20 s. This breaks the Si–O bonds to create Si–OH bonds on the surface [17]. The increased density of nuclei in our process therefore achieves the deposition of continuous and smoother amorphous silicon film. The LPCVD 5000 Å amorphous silicon film was deposited in a standard, horizontal hot wall LPCVD. The deposition was carried out at 130 mTorr and 550 °C with a silane pressure of 60 sccm.

Solid phase crystallization of a-Si was done by annealing the wafers at 775 °C in nitrogen ambient for 5 h. To prevent silicon atom diffusion on a-Si surface during annealing, the wafers were soaked in DI water for 10 min and blown dry. This helps in growing native oxide thick enough to prevent the diffusion. To define the initial edges for the subsequent depositions, trenches of widths varying from 1 to 3 μm were etched completely into the polysilicon layer. Lithography was carried out on a Karl-suss MA6 aligner in which wafers are exposed by the ultraviolet light monitored on i-line. Trenches were etched in the polysilicon in a Semigroup 1000 parallel plate reactive ion etcher, at an RF power (frequency 13.56 MHz) of 100 W and 20 mTorr pressure using CHF_3 (40 sccm), O_2 (10 sccm) and SF_6 (10 sccm). The polymer Shipley 1813 was stripped in Nanostrip solution and the wafers were soaked in acetone and methanol for 10 min followed by 10 min cleaning in JTB-111 solution and DI water rinse. Silicon nitride (25 nm) was deposited on the wafers in a horizontal hot-wall LPCVD system at 300 mTorr and 775 °C. The initial ramp-up time of 5 h has been shown to help in the SPC of the silicon layer. The pressures of dichlorosilane and ammonia were maintained at 40 and 120 sccm. The deposition was done for 7 min to get a film thickness of 25 nm. The wafers were later put in a-Si LPCVD furnace for 8 min to deposit 50 nm of a-Si film. The wafers were then left in ambient conditions in order to grow native oxide, which prevents silicon atom diffusion on the a-Si surface. After this, the wafers were put in nitride LPCVD furnace where the initial ramp-up time causes the SPC of the a-Si layer. A silicon nitride film of 25 nm thickness is deposited and then wafers are put back in the a-Si LPCVD. The process is repeated a number of times depending on the number of nanowires.

After depositing the alternate layers of silicon nitride and a-Si, the trench is planarized. Planarization is done by spinning organic polymer and etching the polymer, silicon nitride and a-Si in the RIE system by a non-selective etch recipe. For this purpose, Shipley 1813 was spun over the wafer at 4000 rpm for 40 s. The RIE was done in Semigroup 1000 system at 10 mTorr pressure and an RF power of 100 W using 40 sccm CHF_3, 5 sccm O_2 and 5 sccm SF_6. This etches away the top 12 000 Å of polymer. Later the non-selective etching is carried out till the stack is planarized with the edge of trenches etched in polysilicon. The non-selective etch process is done at 30 sccm with an RF power of 100 W. The gases used for non-selective etch are 5 sccm SF_6, 88 sccm Ar and 10 sccm CHF_3. After planarization the remaining PR is removed using Nanostrip. The wafers were then soaked in acetone and methanol solution for 10 min each. The nanowires were created by selectively wet etching either polysilicon or silicon nitride. By selectively etching silicon nitride layer we created the polysilicon nanowire template. The width of the structure thus obtained is 50 nm with

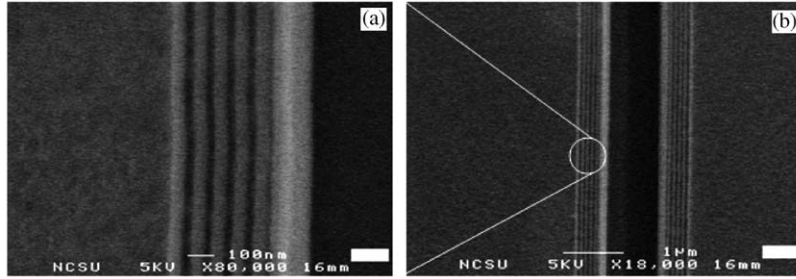

Fig. 2. (a) and (b) SEM of the nanowires formed by the PEDAL process after etching away silicon nitride layer. The width of the nanowires is 50 nm and the spaces are 25 nm.

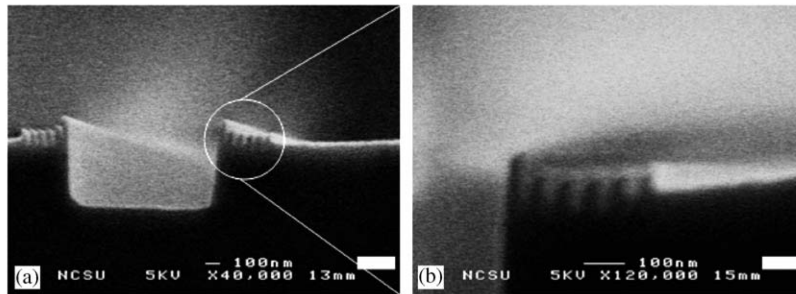

Fig. 3. (a) SEM of the cross-section of the nanowires formed by the PEDAL process after etching away polysilicon layer. (b) SEM showing nanowires along both edges of trench. The width of the nanowires is 25 and the spaces are 50 nm. Nanowires are inclined because of the non-vertical trench walls.

a spacing of 25 nm as confirmed by the SEM, Fig. 2. The silicon nitride nanowire template is created by selectively wet etching polysilicon. The linewidth obtained is 25 nm with spacing of 50 nm as shown in the SEM of the cross-section Fig. 3.

4. Results and discussion

The fabrication was carried out on a batch of five wafers, all of which showed good uniformity all across the wafer as shown in Fig. 4. It was possible to fabricate nanowires with widths as small as 25 nm using PEDAL process. The process allows the flexibility of routing the nanowires, directly on the wafers, around the logic or memory modules of the circuit. The template can also be used in conjunction with oblique metal evaporation and pattern transfer, or as the mold in nano-imprinting to fabricate the wafer scale crossbar structures.

We start with a pattern that is produced by photolithography and has spatial definition of the wavelength of the order of visible light (~600 nm). The process depends on the i-line lithography to define the initial trench structures. These trenches in turn define the position of the array of nanowires as well as the length of nanowires. The depth of the trench, as well as width of the trenches are decided after choosing the number of nanowires, the required width of nanowires to be fabricated along the edge, and the spacing between these nanowires. The relation between the depth of the trench d, width of the trench w, number of nanowires n, width of nanowires w_{n} and spacing s is given by a simple formula shown below:

$$d \geqslant n(w_{\mathrm{n}} + s),$$

$$w > 2n(w_{\mathrm{n}} + s).$$

The above formula holds, assuming the step angle of the trench is 90 and conformality of the

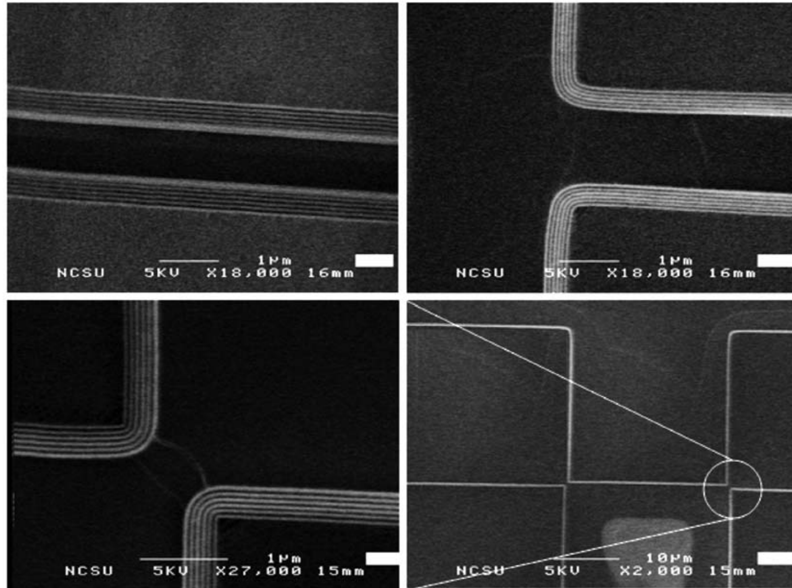

Fig. 4. SEM of various nanowire structures fabricated by the PEDAL process at different locations on wafers.

deposited materials is 100%. A modification in design is needed in order to incorporate deviation from ideal behavior. The fundamental limitation on the minimum width of nanowires is the minimum thickness and conformality of the deposited materials as well as the step angle of the trench. Judicious choices of material and deposition process can help in getting nanowire widths <10 nm. LPCVD has been proved successful over MBE, PECVD, APCVD, PVD [18,19] for getting better conformality of deposited films. The DRIE and ICP RIE systems have shown remarkable results in achieving highly anisotropic etches with step angles as good as 89.5° [15,20]. The LPCVD process used for depositing silicon nitride is a slow process with a deposition rate of 32 A/min at 775 °C and hence it is possible to grow thin films of thickness <15 nm with great uniformity and repeatability. By reducing the temperature, it is possible to get an even lower deposition rate and hence an even lower nanowire width. Amorphous silicon LPCVD is used instead of polysilicon because the LPCVD of polysilicon is a fast process as it is carried out at a higher temperature of 635 °C. The deposition rate affects the surface recovery of the film. When deposition rate increases, the thickness needed to fully recover the surface tends to be higher. Consequently, no continuous polysilicon film can be obtained with a deposited thickness lower than 200 Å. Depositing a-Si on top of silicon nitride has provided smoother films with great uniformity. The a-Si solid phase crystallization process is not performed in situ. There is a need to leave the wafer in ambient condition, in order to grow a native oxide which prevents silicon atom diffusion on an a-Si surface. The SPC is done during the temperature ramp-up while the wafers are in silicon nitride LPCVD furnace. It is also possible to do RTA and crystallize the film. (It was found that a-Si deposition at 500 °C followed by 10 min RTA at 700 °C provides a thickness value <10 nm [17] which can give 10 nm wide nanowires.)

The planarization process decides the uniformity of the height of nanowires across the wafer. We were able to demonstrate the planarization of stack of silicon nitride, polysilicon and Shipley 1813 using the non-selective RIE process with 2.1% uniformity. The etch selectivity observed was 1:1:0.95 for silicon nitride, polysilicon and PR.

The selective wet etch process is very important as it not only defines the height of nanowires but

also the contour of nanowires. The highly selective etch recipe will give sharp nanowire top edges. Etching the polysilicon in KOH solution at 80 °C is a suitable process as it is highly selective over silicon nitride. The contour of the nanowire is important while doing shadow metallization as a smooth contour may cause broadening of the metal nanowires and eventually shorting of adjacent wires. Similarly, round edges may cause an increase in the width of nanowires imprinted onto the wafer when the template is used as a mold.

The SEM of the structure obtained after etching a silicon nitride layer is shown in Fig. 2. The SEM shows several micrometer long nanowires at the edge of trenches. The width of the nanowires is around 50 nm and spaced at around 25 nm. The SEM of the cross-section of structure obtained after etching a polysilicon layer is shown in Fig. 3. The SEM shows the nanowires 25 nm wide with 50 nm spaces. The nanowires are inclined because of non-vertical trench walls. Fig. 4 shows the uniformity of nanowires at different locations on the wafer surface and various structures of nanowires that can be easily made using the PEDAL process.

5. Conclusions

The new PEDAL process is useful in wafer scale fabrication of aligned nanowires directly on the wafer. Nanowires with 25 nm width spaced at 50 nm have been demonstrated. Although the nanowire templates shown in this paper are inclined and less usable as such, with improved vertical trenches and slower CVD process, PEDAL has the potential to fabricate sub-10 nm nanowires with 20 nm pitch. The fabrication facilities required for the process are readily available. The process can also be used to make templates for the nano-imprinting with which the crossbar structures can be fabricated. Also by doing shadow metallization directly onto a wafer, it is possible to make nanowires of different metals directly onto the wafer. The process has the flexibility of routing nanowires around the logic and memory modules all across the wafer without resorting to multiple alignments. For technological applications, it is necessary to have nanowires into a highly ordered array with predetermined spacing and registry and also to know the location and registry between wires precisely. Otherwise, every time electrical contact to the nanowires is to be made, the beginning and end locations of every single nanowire must be determined and the contacts patterned specifically for each wire. The PEDAL process gives wires with precise beginning and ending location depending on the definition of edges of trench, allowing contacts to the wire in predetermined manner.

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