

Molecular Electronic Latches and Memories

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Abstract — Many two terminal molecular devices functioning as diodes have been synthesized with responses similar to solid state devices such as rectifying and resonant tunneling diodes. In this paper, the feasibility of integrating these molecular diodes into current circuit architectures is explored. A bistable latch and memory architecture are simulated using IV data from the 2'-amino-4-ethynylphenyl-4'-ethynylphenyl-5'-nitro-1-benzenethiolate molecule previously published by the Reed group at Yale University. HSPICE simulation results are used to illustrate the performance of a bistable latch and a memory array.

Index Terms — circuits, nanotechnology, architecture, logic, memories, molecular electronics.

I. INTRODUCTION

Over a quarter of a century ago [1], molecules were proposed as building blocks for logic functions and families. Molecular electronic devices have the potential to offer many advantages over their silicon counterparts, including integration into much smaller areas and faster response times [2]. Although these advantages are substantial, additional factors such as interconnect performance, ease of fabrication and defect tolerance must also be quantified to accurately compare a molecular electronic system's response with other solid-state technologies. Although it is clear that several types of two terminal non-linear molecular elements can be chemically synthesized today [3]-[5], it is unclear as to whether they can be integrated into larger circuits and systems based upon current architectures.

Although it is difficult to imagine assembling molecules to anywhere near the same degree of accuracy, certain electrical effects could prove useful in the development of a molecular electronics technology. This work focuses on the design and development of several molecular electronics circuits and potential applications. Simulations demonstrating a bistable latch and several memory architectures are presented. Finally, architectural implications of these circuits are discussed.

II. CIRCUIT ELEMENTS AND SYSTEMS

A majority of molecular electronic devices being synthesized and characterized today contain two terminals and function predominately as diodes. Molecular

electronic devices displaying both rectifying diode and Resonant Tunneling Diode (RTD) characteristics have been demonstrated [3]-[5]. Diode-based logic families are well understood and a large number of logic gates and digital systems based on diodes have been designed and fabricated since their conception. Logic gates such as the AND and OR functions have been constructed using only rectifying diodes connected to the input terminals and a resistor connected to either a power rail or ground [6]. RTDs have proven useful in the design and fabrication of logic families, memories, oscillators and other devices [7]-[10]. Although the usefulness and scalability of these diodes fabricated in current solid-state technology is proven in many applications, the scalability of molecular devices exhibiting similar current-voltage responses is not well understood. In addition, impact of parasitic effects such as interconnect wire capacitance and how they might affect the performance of these systems is equally not well understood and likely will depend on the properties of each molecular device.

A useful characteristic of the IV curve measured from a cluster of 2'-amino-4-ethynylphenyl-4'-ethynylphenyl-5'-nitro-1-benzenethiolate molecules² is the negative differential resistance region. Negative differential resistance is exploited in applications such as oscillators, memories and digital logic elements [8]-[10]. When a device exhibiting NDR is placed in series with a resistor and voltage source, a bistable latch can be created. Although loading with a resistor is the simplest method for creating a bistable latch, previous research has shown that an RTD can be loaded with a depletion-mode FET or another RTD to form bistable latches. Area and performance improvements have been demonstrated through the integration of these latches into CMOS technologies [11].

As shown in Figure 1, the IV data from 2'-amino-4-ethynylphenyl-4'-ethynylphenyl-5'-nitro-1-benzenethiolate is superimposed with various load resistances. The molecular device has a peak current of approximately 1nA, a valley current of approximately 1pA and a peak-to-valley current ratio of 1030:1 [3]. The peak current for this device occurs at 2.12V as measured by Chen and Reed. In the region from 0 to 1.5V, the device conducts only the valley current, or 1pA.

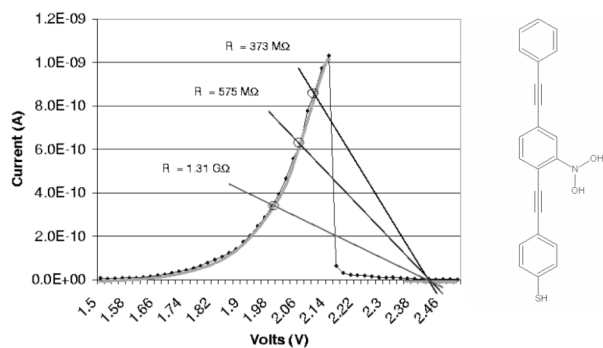


Fig. 1. Load line for mononitro dithiol molecule using 1.31GΩ, 575MΩ and 373MΩ resistors.

A. Bistable Latches

In simulation, a resistor was chosen to load the NDR device and form a bistable latch for three reasons. First, the I-V characteristics and area of the molecular devices do not lend themselves to simple integration with FETs. A peak current of 1nA is several orders of magnitude lower than what would be required to intersect the load line of a depletion mode FET. In addition, the feasibility of an all-molecular device solution is of principal interest. Second, loading the NDR device with another molecular NDR device exhibiting a similar I-V characteristic would not necessarily result in two distinct stable operating points. If two of these devices were placed in series with a bias voltage as previously shown [11], the resulting load lines would intersect at a large number of points. This is due to the long, flat conducting regions of the I-V curve from 0V to 1.5V and above 2.4V. A trait common to RTDs that makes this type of loading possible is the continual increase in conductivity at voltages above the NDR region of the device. Finally, it has been demonstrated that molecules exhibiting a large linear resistance can be synthesized and possibly integrated with the molecular NDRs [12,13].

As previously mentioned, the value of the load resistor will determine the slope of the load line. This will impact the location of the two stable points of intersection with the molecular NDR, determining the high and low voltages for each of the two states of the bistable latch. In the high voltage state, the molecular device will operate in the low conduction region. In the low voltage state, the molecular device will operate in the high conduction region. The x-intercept of each load line shown in Figure 1 is set by the voltage source, Vdd. The y-intercept of the load line is set by the voltage source divided by the load resistor, or V_{dd}/R . In Figure 2, the impact of several load

resistance values on the bistable points is illustrated. For these three load lines, the voltage source (Vdd) and resistances (R) are 2.41V and 373MΩ, 575MΩ and 1.31GΩ respectively. If the load resistor is much below 373MΩ, there is a risk the latch will not set in the low voltage state.

Avant! STAR-HSPICE 98.2 was used to simulate the performance of the latch circuit shown in Figure 2. A model was created using a voltage-controlled current source defined as a “G” element in HSPICE. The schematic in Figure 2 displays the input and output terminals on the latch. Figure 2 illustrates the input and output waveforms of a latch loaded in series with a 373MΩ resistor and a 2.41V source. Toggling between the two stable points is achieved by pulsing the voltage source, V_{bias} , above and below the 2.41V steady state value. As shown in Figure 2, this latch results in two stable points of operation separated by 0.32V. Transitions from the low voltage state to the high voltage state require a smaller V_{bias} pulse than from high to low. This is because the low voltage stable point of operation is closer to the NDR region than the high voltage stable point. With larger resistor values, the two stable points could be placed equidistant from the NDR segment, resulting in the same V_{bias} pulse magnitudes required to transition between the states.

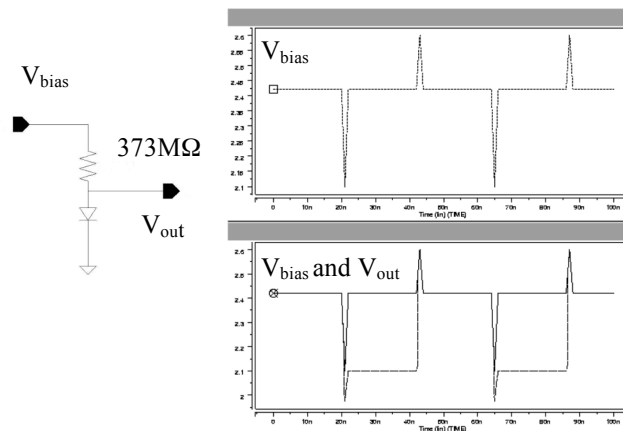


Fig. 2. Bistable latch for mononitro dithiol molecule loaded with a 373MΩ resistor. The two memory states are separated by 0.32 volts.

B. Memories

Memory element architectures are promising candidates for molecular integration due to their regular structure. Regularity, or repeating structures, lend themselves to nanofabrication techniques and also to random self-assembly of molecular components.

One challenge in building memory cells is to design the circuits in a manner that allows them to be scaled to a large functional array. Shown in Figure 3 is an example of a memory that uses the NDR as both a memory storage device. As before, all resistor values are $373M\Omega$, while the capacitors were replaced with an NDR device and a near-ideal diode respectively, allowing for DC operation. A reset is performed by pulling the selected wordline high, to 2.7V, which forces all memory latches on that wordline into the low-conductivity state. Subsequently, the selected wordline can be written by lowering it to 2.27V while raising the write bitlines where a logic '0' is to be stored. Only the combined effect of these bias conditions will cause the NDR bias to drop below the threshold, changing the state of the latch to the high-conductive state; cells in other wordlines remain above the threshold due to the slightly higher wordline bias, while '1' cells in the selected wordline remain above the threshold due to the lower bitline bias.

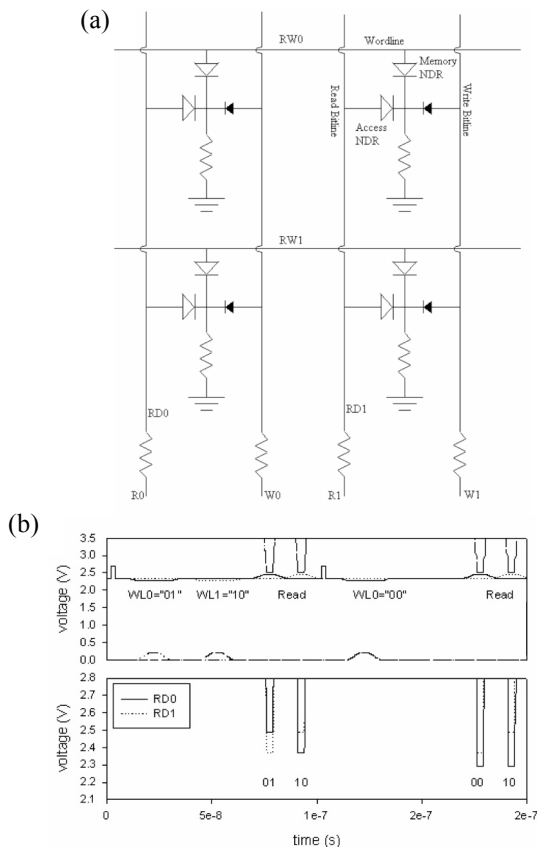


Fig. 3. 2x2 Memory array approach (a) with no isolation capacitors and (b) the corresponding waveforms.

A read is performed by raising the wordline voltage to 2.46V, a value low enough not to cross the threshold and causing a reset. In memory cells storing a logic '0', this causes a significant increase in the voltage at the center node. At the same time, the bitline bias, with the load resistor connected, is lowered, which acts in combination with the raised center node voltage in memory cells storing a logic '0', decreasing the voltage across the access NDR far enough to cause the "access latch" formed by the access NDR and the resistor in the cell to cross the threshold and switch to the high-conductivity state. This causes increased current draw through the external bitline load resistor, thus lowering the read-out voltage. A cell storing a logic '1' would have a low center voltage due to the memory latch being in the low-conductivity state, and would thus not allow the access NDR to become conductive.

The noise margin will be limited by the voltage difference between the normal wordline bias and the raised wordline bias, which cannot exceed the difference between the two threshold voltages of the latch. Assuming reasonable values for the load resistor in the cell, this value is limited to a few tenths of a volt. There are actually three noise margins: the noise margin from the normal bias to the low threshold voltage ("set margin"), the margin from the raised to normal bias ("access margin"), and from the high threshold voltage to the raised bias ("reset margin"). None of these are higher than a few tenths of a volt. Furthermore, scaling of the memory is limited by the isolation characteristics of the NDR device.

Isolation is provided by the low conductivity of the NDR device beyond the NDR peak, as well as the reverse-biased rectifying write diode. NDR devices with peak-to-valley ratios of better than 1000:1 have been presented [3], which would limit the number of words in the memory on the O(100). It is interesting to note that this isolation does not have to be absolute. If the cell being accessed contains a logic '0', it will draw current through the access latch (the external load resistor and the access NDR). This will result in a reduced read bitline voltage, which can trigger access NDRs in other wordlines to turn on, amplifying the read-out swing.

Although these noise margins should be improved upon to allow the maximum scaling potential of this memory in its present form, large improvements could result from different NDR I-V characteristics, larger load resistors and/or more conductive NDR devices.

III. FUTURE APPROACHES

Memory architectures, which tend to be constructed from more ordered arrays of logic, may be a suitable

application for two-terminal molecular devices. The highly resistive loading elements could possibly be replaced with other molecular diodes if their IV characteristics more closely resemble that of conventional resonant tunneling diodes. If molecular memories can be chemically synthesized, an option exists to realize logical functions within these memories by implementing them as lookup tables. Theoretical architectures based upon molecular memories and reconfigurable logic are currently under investigation [14]-[17] and the potential density advantages molecular devices offer could make extremely large-scale implementations of entire systems within molecular memory and latches possible. In addition, the regular arrays of interconnect wiring might also allow for a less demanding fabrication and molecular assembly processes, and be less susceptible to defects which will likely be quite high.

Other fabrication techniques based on molecular self-assembly have been proposed which lessen the demand for nanometer-scale lithographic capabilities [18]. These techniques rely on post-fabrication training of the logic block. The benefit of such an approach is that it allows for organized logic to be fabricated out of disordered, self-assembled chemical structures with a method that is defect tolerant [19]. Although it is likely that some form of nanometer-scale lithographic steps will be required to route clock and interconnect wires, this approach greatly lessens the burden for fabrication and attempts to address the organization of high-density logic through post-fabrication methods.

III. CONCLUSIONS

In conclusion, the feasibility of integrating molecular diodes into current circuit architectures has been explored. A series of logic gates and a 4x4 memory array were simulated based on the voltage-controlled current flow method using the 2'-amino-4-ethynylphenyl-4'-ethynylphenyl-5'-nitro-1-benzenethiolate molecular diode IV sweep data [3]. A 4x4 memory was designed and simulated using a bistable latch configuration for each memory bit, and read/write operations were demonstrated.

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REFERENCES

- [1] A. Aviram, M. A. Ratner, "Molecular Rectifiers," *Chem. Phys. Lett.* 29, pp.277-283, 1974.
- [2] J. Tour, M. Kozaki, J. M. Seminario, "Molecular Scale Electronics: A Synthetic/Computational Approach to Digital Computing," *J. Am. Chem. Soc.* 120, pp. 8486-8493, 1998.
- [3] J. Chen, M. A. Reed, A. M. Rawlett, J. M. Tour, "Large On-Off Ratios and Negative Differential Resistance in a Molecular Electronic Device," *Science* 286, pp. 1550-1552, 1999.
- [4] R. M. Metzger et al., "Unimolecular electrical rectification in hexadecylquinolinium tricyanoquinodimethanide," *J. Am. Chem. Soc.* 119, pp. 10455-10466, 1997.
- [5] C. Zhou, M. R. Deshpande, M. A. Reed, L. Jones II, J. M. Tour, "Nanoscale metal/self-assembled monolayer/metal heterostructures," *Appl. Phys. Lett.* 71, pp.611-613, 1997.
- [6] Wakerly, *Digital Design Principles and Practices*, pp. 59-62, Prentice-Hall Inc., New Jersey, 1990.
- [7] J. L. Huber et al., "An RTD/Transistor Switching Block and Its Possible Application in Binary and Ternary Adders," *IEEE Trans. Electron. Devices* 44, pp. 2149-2153, 1997.
- [8] W. F. Chow, *Principles of Tunnel Diode Circuits*, Chapters 8 and 11, John Wiley & Sons Inc., New York, 1964.
- [9] Kern K. N. Chang, *Parametric and Tunnel Diodes*, Chapters 11 and 12, Prentice-Hall Inc., New Jersey, 1964.
- [10] J. M. Carroll, *Tunnel-Diode and Semiconductor Circuit*, Chapters 5-7, McGraw-Hill Inc., New York, 1963.
- [11] R. H. Matthews et al., "A New RTD-FET Logic Family," *Proc. IEEE* 87, pp. 596-605, 1999.
- [12] P. S. Weiss et al., "Probing electronic properties of conjugated and saturated molecules in self-assembled monolayers," *Ann. NY Acad. Sci.* 852, pp.145-168, 1998.
- [13] J. C. Ellenbogen, J. C. Love, "Architectures for Molecular Electronic Computers: 1. Logic Structures and an Adder Designed from Molecular Electronic Diodes," *Proc. IEEE* 88, pp. 386-426, 2000.
- [14] S. C. Goldstein, "Electronics Nanotechnology and Reconfigurable Computing," *Proc. IEEE. Computer Soc. Workshop on VLSI*, pp. 10-15, 2001.
- [15] S. C. Goldstein, M. Budiu, "NanoFabrics: Spatial Computing Using Molecular Electronics," *Proc. 28th Annual Int. Sym. On Comp. Architecture*, pp. 178-189, 2001.
- [16] R. StanleyWilliams, P. J. Kuekes, "Molecular Nanoelectronics," *IEEE Int. Sym. On Circuits and Systems*, pp. 5-7, 2000.
- [17] Philip J. Kuekes, Duncan R. Stewart, R. Stanley Williams, "The crossbar latch: Logic value storage, restoration, and inversion in crossbar circuits," *J. App. Phys.* 97 (2005).
- [18] J. M. Tour, W. L. V. Zandt, C. P. Husband, L. S. Wilson, P. D. Franzon, and D. P. Nackashi, "Nanocell Logic Gates for Molecular Computing," *IEEE Transactions on Nanotechnology*, 2002.
- [19] James R. Heath, Philip J. Kuekes, Gregory S. Snider, R. Stanley Williams, "A Defect-Tolerant Computer Architecture: Opportunities for Nanotechnology," *Science* 280, pp. 1716-1721.