28.7 3Gb/s AC-Coupled Chip-to-Chip Communication using a Low-Swing Pulse Receiver

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Recently, several technologies have been reported using capacitive coupling to replace physical pin/solder bumps for high-density low-power chip-to-chip communications. In contrast to most of the recent results focusing on stacked ICs [3-5], the work presented here is optimized for lossy board-level capacitively coupled interconnect, and is built upon the work described in [1] and [2]. Previous single-ended or differential pulse receivers [1, 3, 4, 5, 6] require more than 200mV single-ended peak-to-peak (SEPP) input swing when scaled to 0.18μm CMOS/1.8V_{DD}, as shown in Fig. 28.7.1. In this work, a differential pulse receiver is proposed that requires 60mV SEPP input swing, thus enabling 5-times smaller coupling capacitors (and therefore, higher I/O density) and longer transmission lines (TL), comparing with previous work [1]. A 3Gb/s chip-to-chip error-free communication is demonstrated through two 150fF coupling capacitors and a 15cm FR4 microstrip line. On the test chip, a semi-digital dual DLL successfully recovers RX clock phase from the recovered NRZ data. An on-chip BER test circuit confirmed error-free data communication up to 3Gb/s.

Figure 28.7.2 shows the physical cross-section and circuit view of an AC-coupled interconnect (ACCI) system [1, 7], and the waveforms at TX output, RX input and RX output. The buried bump structure enables simultaneous creation of DC- and AC-coupled paths between a chip and a package (although an MCM is shown, it can be used for conventional packaging) and it also provides self-alignment [7]. The combination of serial coupling capacitors, parasitic capacitors and the TL creates a channel from the TX to the RX with a band-pass response. A pseudo-differential TX outputs full-swing, high edge rate NRZ data. The serial capacitors convert the data into pulses at the data transitions, and RX recovers the low-swing incoming pulses to NRZ data. ACCI promises low power, high I/O density, low cost, high bandwidth and removal of ESD protection for board-level interconnect.

In ACCI, since the coupling capacitors block the DC signal, the RX needs to self-bias, then amplify and convert the pulse signal into NRZ data. Figure 28.7.3 illustrates the low-swing pulse receiver. An inverter with negative feedback (M_1-M_6) self-biases and amplifies the pulse signal at the RX input. The feedback structure not only sets up the bias level but also continuously clamps the inverter into the high gain region. There are two feedback mechanisms employed here to achieve both adaptive swing control and stable bias level to accommodate variations of coupling capacitor size and TL length. The diode-connected feedback (M_1-M_4) limits the swing at the output of the inverter by adaptively controlling the feedback strength. It also sets up a coarse bias voltage, which is sensitive to the data pattern and both the width and swing of the incoming pulses. To mitigate this problem, the pass gate (M_5 and M_6) tied to Vdd, provides a weak but constant feedback to stabilize the bias voltage, making it less sensitive to the input pulses. The source-coupled logic (M_7-M_9) further amplifies the pulses, while the cross-coupled PMOS load (M_{11} and M_{12}) serves as a latch to recover NRZ data. A clamping NMOS device (M_{10}) limits the swing of long 1s or 0s and enables latch operation for short pulses which improves operating bandwidth. Careful layout is necessary to minimize the mismatch, especially for the bias stage. Most of the noise coupled from the transmission line is common-mode noise, that can be rejected by this differential receiver. Simulation shows a 0.8UI opening in the recovered NRZ data with coupling capacitors variation from 80fF to 180fF, combined with TL length variation from 0 up to 20cm. The recovered NRZ is then fed to the clock and data recovery circuit on the test chip.

No active equalization is used at the TX or RX, since the coupling capacitors provide passive equalization for ACCI. A step input to the channel results in a pulse signal on the TL and at the RX input (Fig. 28.7.4). The TL has a low-pass effect due to the skin effect and dielectric loss, resulting in a long tail on the pulse signal. Without equalization, this tail would cause ISI and would reduce the timing margin at the RX. However, the coupling capacitor performs equalization by filtering the long pulse tail, thereby, reducing energy that interferes with adjacent pulses. This inherent behavior allows ACCI to save the chip area and power dissipation typically associated with circuit-based equalization implementations.

The configuration of the test chip is shown in Fig. 28.7.5. Four PRBS with pattern lengths of 2^7-1 are generated with spread seeds and multiplexed by 4 into a 3Gb/s data stream. The TX outputs full-swing NRZ data into the ACCI channel. To reduce reflections, a shunt termination is used. The RX circuit recovers the NRZ data from the low-swing pulses and sends this data to a semidigital dual DLL. The clock phase at the RX is recovered and the data are demultiplexed by 4 and analyzed for BER.

A 2mm×3.5mm test chip with seven TXs and five RXs is fabricated at MOSIS in the TSMC 0.18μm CMOS technology (Fig. 28.7.7). Each TX and RX circuit occupies an area of 40μm×20μm and 45μm×15μm, respectively. The seven TXs share the TX test (TXT) circuitry. Each of the five RX circuits has an individual RX test (RXT) circuitry. Figure 28.7.6 shows the clock recovered by the semidigital dual DLL with a phase interpolation step of 16ps and the recovered and demultiplexed NRZ data, which is error free and only has 7ps rms jitter. For each channel, the TX and RX consume 5mW and 10mW, respectively at 3Gb/s data rate. An additional 110mW of power is dissipated by all other circuits including test and measurement (Fig. 28.7.4) and output buffers to measurements pads.

References:
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[2] T. Knight, "Capacitive Chip to Chip Interconnections," Polychip Inc and M.I.T. Artificial Intelligence Laboratory, 1990.
[3] K. Kanda et al., "1.27Gb/s/pin 3mW/pin Wireless Superconnect (WSC) Interface Scheme," *ISSCC Dig. Tech. Papers*, pp. 186-187, Feb., 2003.
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[7] S. Mick, L. Luo, J. Wilson and P. Franzon, "Buried Bump and AC Coupled Interconnection Technology," *IEEE Trans. on Advanced Packaging*, vol. 27, pp. 121-125, Feb., 2004.
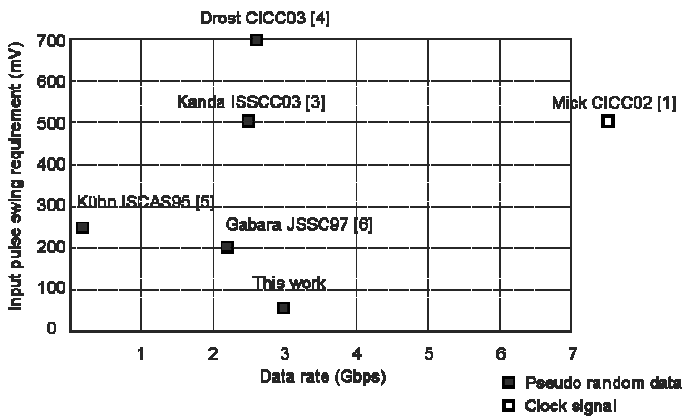
Figure 28.7.1: Comparison with previous CMOS high-speed pulse receivers. (All scaled to 0.18μm/1.8V single ended peak-to-peak input swing).
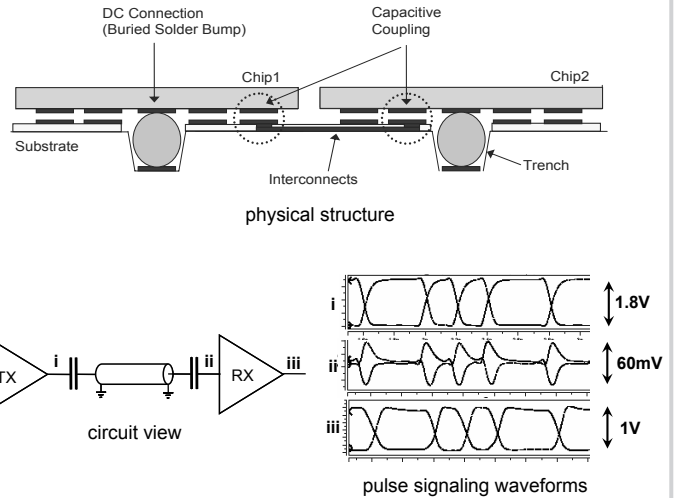

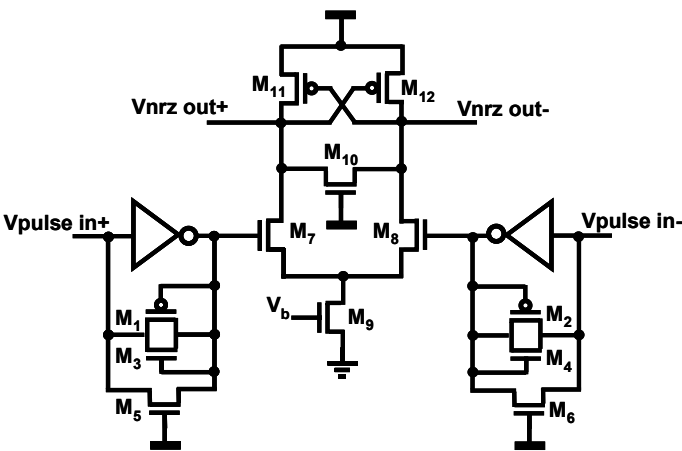**Figure 28.7.2: AC-coupled interconnect.**

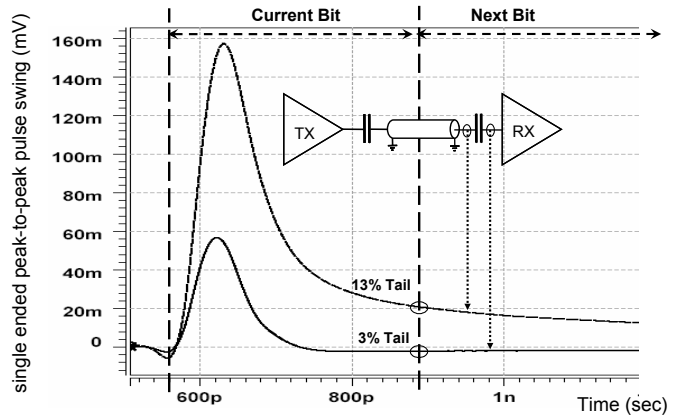**Figure 28.7.3: Proposed low-swing high-speed pulse receiver.**

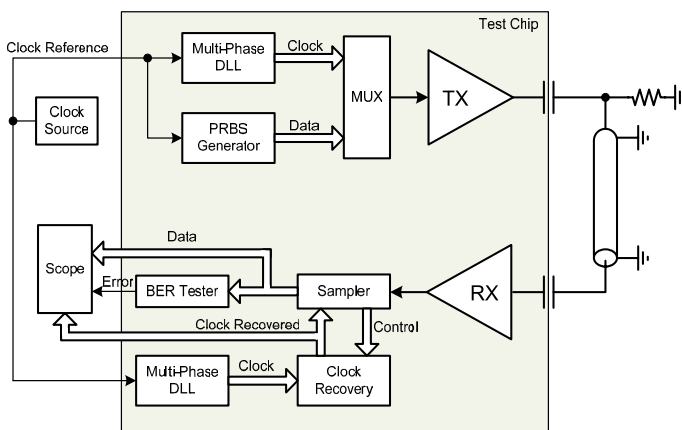**Figure 28.7.4: Coupling capacitors provide passive equalization.**

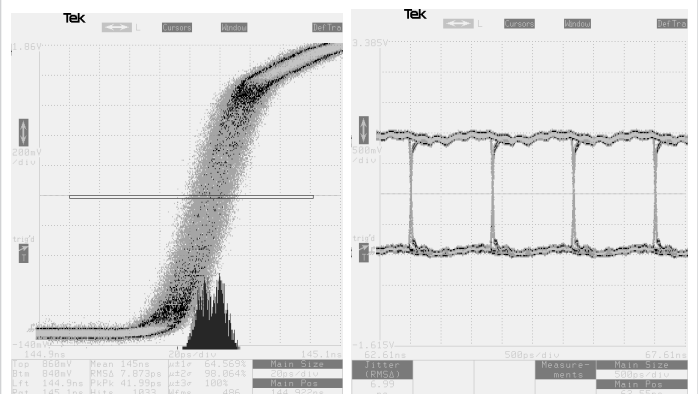**Figure 28.7.5: Block diagram of the test chip.**
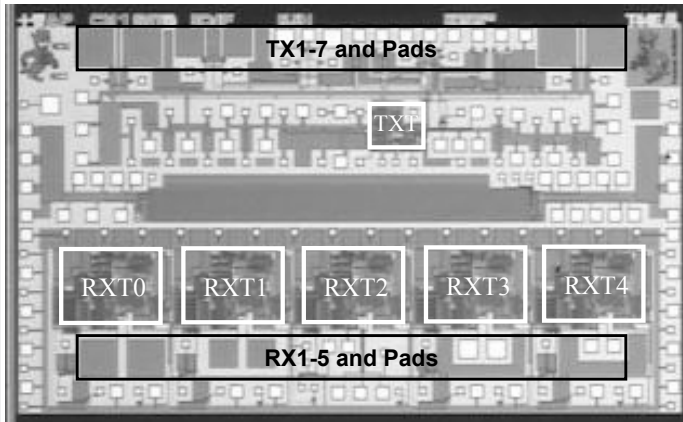

Figure 28.7.6: Recovered clock and data.

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Figure 28.7.7: Die micrograph of TSMC 0.18μm CMOS test chip (2mm$\times$3.5mm).