Signal Integrity and Robustness of ACCI packaged systems

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ABSTRACT- AC coupled interconnects (ACCI) enable reliable multi-Giga-b/s/channel communication with less than 100um pin pitch, and with BER less than 10^{-12}. This paper discusses the potential for switching noise, crosstalk and ISI control in ACCI system.

I. Introduction

Capacitive coupling has been demonstrated as a means to enable high data rate interconnection between ICs [1]. Buried solder bump technology provides DC connections across the same interface as the AC connections, thereby, providing a systematic approach for high speed, high density and low power chip to chip communication. A low swing pulse receiver was reported [4], which enabled greater interconnect length and higher AC pad density. Figure 1 shows the physical structure, circuit view and signaling waveforms of a typical ACCI system. Potential switching noise, crosstalk and ISI associated with ACCI and its Return-to-zero (RZ) pulse signaling have not been reported. This paper will focus on these signal integrity aspects and robustness of ACCI packaged systems.

Section II discusses how to reduce self-generated switching noise. Section III describes crosstalk noise in ACCI systems. Section IV investigates the effects of process variation on ACCI systems and gives design rules on coupling capacitance and T-line.

II. Switching Noise

The effects of power supply switching noise on signal integrity limit the level of system integration. In ACCI systems, it is important to reduce the self-generated switching noise at the transmitter side, and improve noise immunity at the receiver side.

Due to its high input impedance, ACCI channel allows the use and also requires a voltage mode driver. Voltage mode drivers save significant power (Figure 2) but also generates more switching noise than traditional current mode drivers, as show in Figure 3, where SN1 and SN2 are the switching noise generated by a complementary voltage mode driver use in ACCI, and a differential mode current mode driver for traditional channel, respectively. The complementary voltage mode driver with capacitive loading generates five times of switching noise on the power supply than the current-mode driver.

This self-generated switching noise can be reduced in several ways. Sufficient use of on-chip and off-chip bypass capacitors and large numbers of low inductance power supply pins are preferred, which is actually available in ACCI systems. AC signal pins are built with very high density so that most of the chip surface area is available for power supply pins. In addition, slew control can be used at transmitter side to slow down the signal edge rate and thus reduce the switching noise. This is feasible for lower signaling rates or for shorter link length communication.

Another more efficient and low cost way, proposed here, is to spread the transition edges among all I/Os. Since the switching noise only happens at data transition edge for all the channels, it is possible to average the di_n/dt (n is the number of channels associated with edge spreading) by spreading the transition edge of the data. Simulations show that power supply switching noise is reduced significantly by using this edge spreading method as shown in Figure 3. This method is especially efficient when the data of the channels are independent. In serial link applications, spreading of edges will not affect the timing constraint since at receiver side, each channel will be individually recovered from RZ-pulse signals to non-return-to-zero (NRZ) data by the asynchronous pulse receiver and then sent to individual clock and data recovery circuits [4].

Switching noise can also come from other parts of the chip/system. Common-mode noise coupled from transmission lines at board level or multi-chip module (MCM) level could be larger than the actual signal itself, which means a signal-to-noise ratio (SNR) less than 1. Fortunately, the noise is usually common mode and can be rejected by a differential receiver. This requires good noise rejection circuit at receiver side.

III. Crosstalk Noise

Unlike traditional NRZ signaling, RZ pulse signaling uses more bandwidth, as shown in Figure 4. These high frequency components could generate more crosstalk noise. Analysis is performed on coupled micro-strip T-lines as shown in Figure 7. The T-Line has width and coupling space of 5mil. Dielectric thickness is 4mil. Cross-coupled capacitance and mutual inductance are extracted using a field solver and then used in spice simulations for both an ACCI channel and a traditional

channel. Xtalk noise is measured when the space S2 between neighboring T-Lines is 5mil, 10mil and 20mils, as shown in Figure 5. The top two curves show the commom mode (CM) xtalk noise generated by RZ pulses and by traditional NRZ signals. The bottom two curves show the differential-mode(DM) xtalk noise generated. From the simulations, the xtalk noise generated by RZ-pulse signals and by traditional NRZ signals are similar as long as the space between two coupled lines is greater than 10mils.

The receiver can reject most of the CM noise. But the differential noise is more critical because it will directly reduce the noise margin at receiver side input. From Figure 5, as long as the neighboring T-lines are spaced more than 10mils, the differential xtalk noise will be controlled within 3% of the aggressor's swing. To get good isolation from xtalk generated by RZ-pulse signals, 20mils of space is needed, which is 5 times the dielectric thickness H.

IV. Process and application variations

The ACCI channel can vary a lot due to process and application variations, including coupling capacitance and T-line parameters. T-line parameters vary with applications. Coupling capacitance varies with the gap between the plates and the plate size. The dielectric between the two plates can be air or a high-k material. As shown in Figure 8, the two curves indicate the size of the plates needed to achieve a 150fF coupling capacitance with various gaps, for both air dielectric and a high-K dielectric. When compared with an air dielectric, a high-K dielectric enables much higher pin density even for larger gaps. Also, when using a high-K dielectric and an increased gap, the sensitivity of capacitance variation due to gap variation is greatly reduced.

The coupling capacitors and T-line parameters define the ACCI channel response and thus both the pulse swing and pulse width, which play an important role on BER. Pulse swing need to meet the swing requirement of the pulse receiver, while the pulse width need to be less than bit period to avoid inter-symbol-interference (ISI). In another word, the coupling capacitance and T-line parameters control the voltage and time margin of the RZ-pulse signal at receiver's input and thus directly affect BER. For a given data rate and pulse receiver input sensitivity, there is a range of coupling capacitor sizes and T-line lengths, within which a pulse receiver is able to recover the NRZ data.

To explain how coupling capacitance affects the RZ-pulse swing and width, Figure 6 shows the differential RZ-pulse eye diagram after the second coupling capacitance (i.e. at the input of the receiver). The arrow shows the trend resulting from increasing the coupling capacitor size. Larger coupling capacitors will increase the peak-to-peak pulse swing and overall pulse duration. The increased swing relaxes the constraint on the receiver input sensitivity, but the increased pulse width may introduce inter-symbol-interference (ISI). On the other hand, a smaller coupling capacitance is more efficient at filtering the pulse signal tail and mitigating ISI, but the corresponding reduction in signal swing increases the input sensitivity requirement for the pulse receiver. Therefore, the maximum coupling capacitance is constrained by the ISI limit, or the data period limit; while the minimum coupling capacitance is constrained by the swing limit, or pulse receiver input sensitivity. Similarly, the T-line also affects channel response and pulse shape. Longer T-lines result in more attenuation, especially high frequency attenuation. This not only extends pulse width (increasing ISI) but also limits pulse swing. Thus, the maximum T-line length is constrained by both the ISI limit and swing limit.

To investigate the robustness of the ACCI system, a shmoo plot is shown in Figure 9, where the coupling capacitors vary from 65fF to 205fF, combined with T-line length varying from 0cm to 55cm. As discussed before, minimum coupling capacitance, on the bottom of plot, is constrained by the input pulse swing requirement of the receiver. Maximum coupling capacitance, the top part of the plot, is constrained by ISI in neighboring pulses, which requires pulse width to be less than the 330ps bit period for 3Gb/s operation. Maximum T-line length is constrained by either swing (in lower right area) or ISI limit (in upper right area). The valid operating range, for variation in both or one of the coupling capacitors, allows a tolerance of capacitance value, including the six degrees of misalignment [2].

V. Conclusions

ACCI RZ-pulse signaling has the benefits of high pin density, low power and high speed. The potential issues, such as switching noise, crosstalk noise, ISI and process variations are controllable and are comparable with traditional current mode NRZ signaling. Proposed edge spreading technique can reduce the switching noise significantly for the voltage mode driver with capacitive loads. The xtalk noise generated by RZ-pulse signals and by traditional NRZ signals are similar as long as the space between two coupled lines is greater than 2.5*H, where H is the dielectric thickness. High-K material filling enables larger gap between the two capacitor plates and relieves the capacitance change due to gap variation. Measurement shows a 3Gb/s/channel communication with a BER less than 10^{-12}, through a 15cm ACCI channel with 150fF coupling capacitors. This 150fF coupling capacitor can be implemented as small as 75um pitch, with 5um thick high-K material filling between the two capacitor plates, as shown in Figure 8. Analysis including all the noise sources and processing corners shows a valid chip-to-chip communication range from 0cm to 20cm, even with a simultaneous change in one or both of the coupling capacitors from 85fF to 175fF.

Acknowledgements

This work was supported by SRC under contract 99-NJ-722 and NSF under grant EIA-9703090. The authors wish to thank MCNC for providing solder bump services.

References

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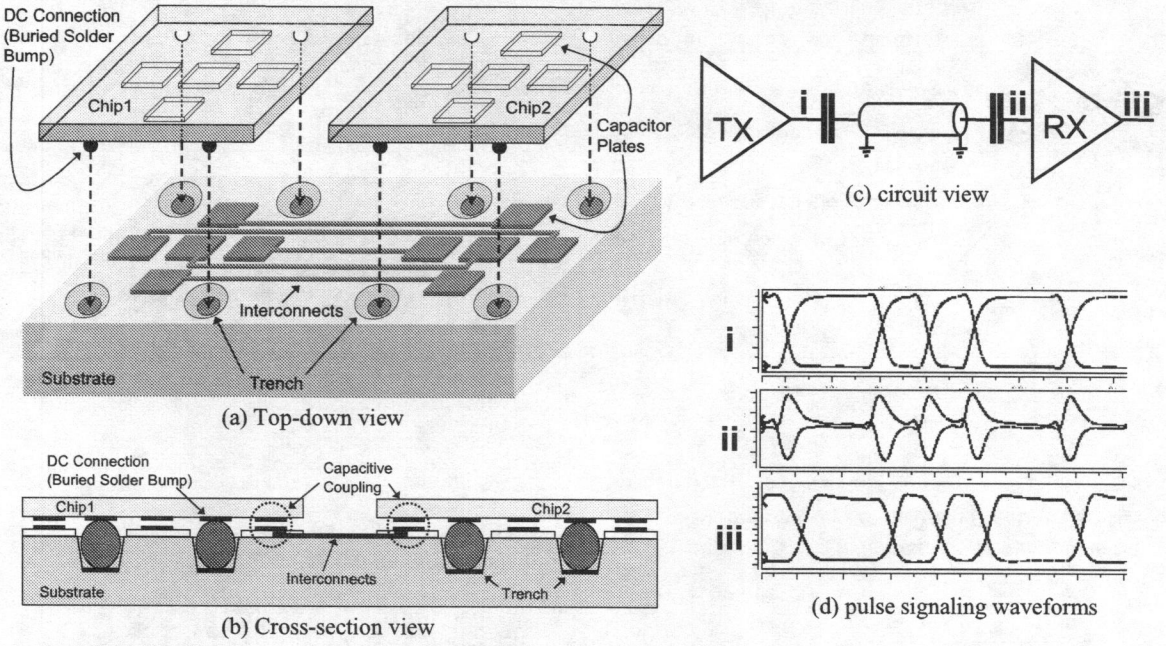

Figure 1: ACCI physical structure, ciruit view and pulse signaling waveforms

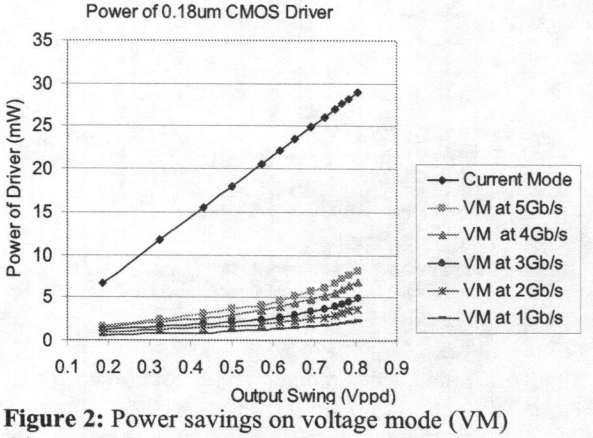

Figure 2: Power savings on voltage mode (VM) driver, with a data activity of 0.5

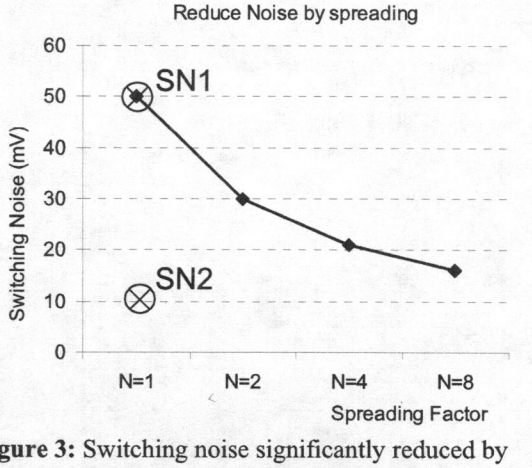

Figure 3: Switching noise significantly reduced by spreading the data transition edges across I/Os

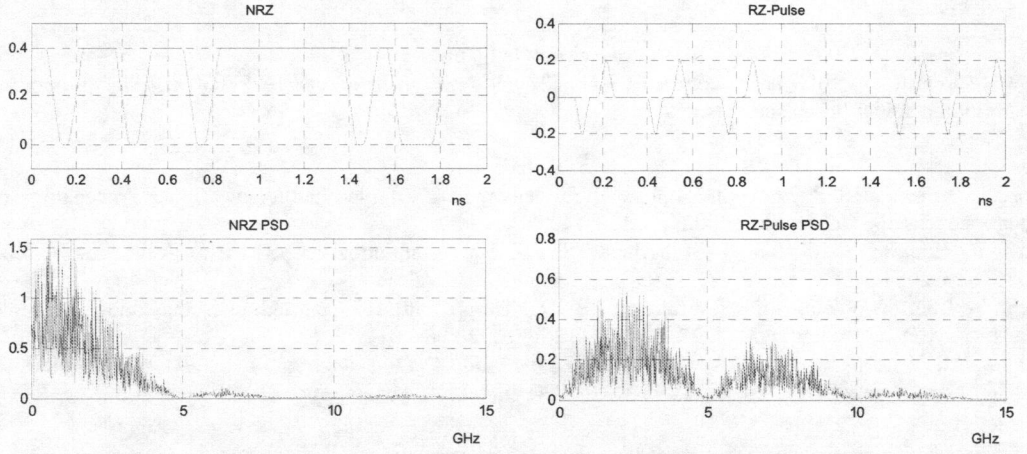

Figure 4: Transient waveform and power spectrum density (PSD) of NRZ data and RZ-pulse data

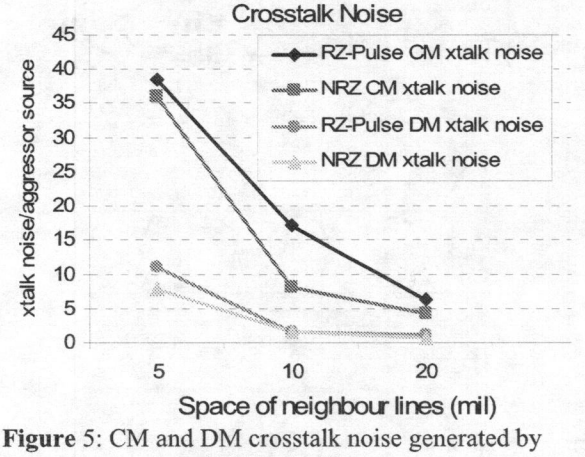

Figure 5: CM and DM crosstalk noise generated by RZ-pulse signal and NRZ signal

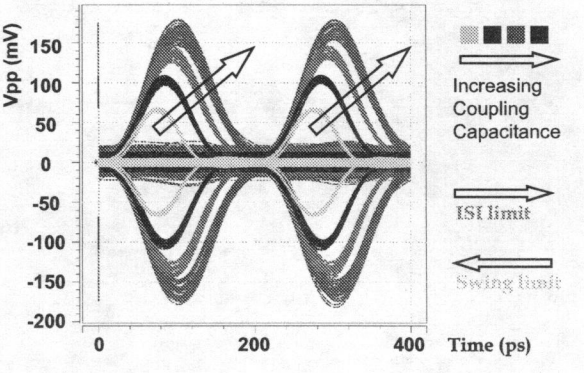

Figure 6: Differential pulse eye diagrams with increasing coupling capacitance

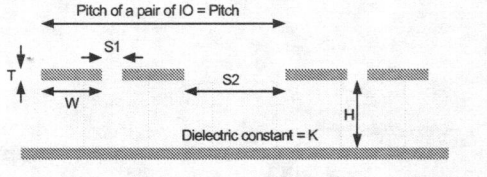

Figure 7: T-LINE Pitch for Coupled Micro-strip

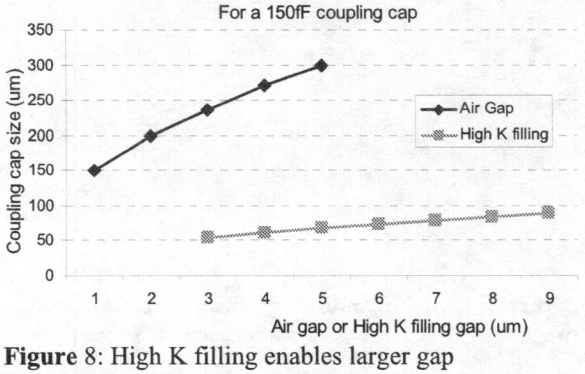

Figure 8: High K filling enables larger gap

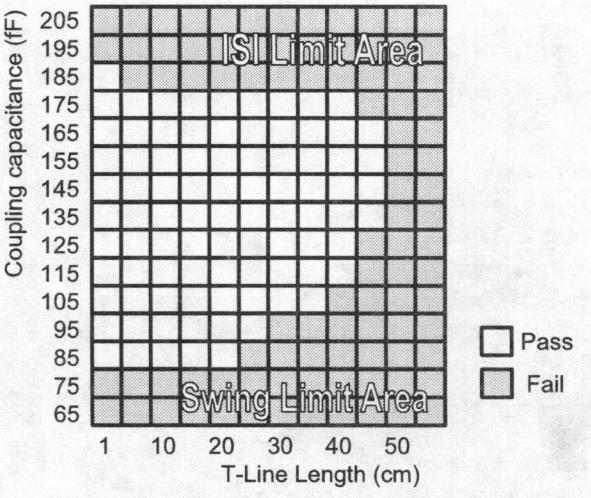

Figure 9: Simulated shmoo plot with coupling capacitance and T-line length variations, pass criteria is 0.8UI time opening at the eye diagram of the recovered NRZ data.