INSTITUTE OF PHYSICS PUBLISHING NANOTECHNOLOGY
Nanotechnology **16** (2005) 2251–2260 doi:10.1088/0957-4484/16/10/047

Scaling constraints in nanoelectronic random-access memories

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Received 30 April 2005, in final form 28 July 2005
Published 26 August 2005
Online at stacks.iop.org/Nano/16/2251

Abstract
Nanoelectronic molecular and magnetic tunnel junction (MTJ) MRAM crossbar memory systems have the potential to present significant area advantages (4 to $6F^2$) compared to CMOS-based systems. The scalability of these conductivity-switched RAM arrays is examined by establishing criteria for correct functionality based on the readout margin. Using a combined circuit theoretical modelling and simulation approach, the impact of both the device and interconnect architecture on the scalability of a conductivity-state memory system is quantified. This establishes criteria showing the conditions and on/off ratios for the large-scale integration of molecular devices, guiding molecular device design. With 10% readout margin on the resistive load, a memory device needs to have an on/off ratio of at least 7 to be integrated into a 64×64 array, while an on/off ratio of 43 is necessary to scale the memory to 512×512.

1. Introduction

Nanoelectronic memory devices have been researched in recent years as a potentially denser alternative to CMOS-based systems. One particular class of memory devices under investigation is a crossbar array of nanoelectronic devices that store the memory state as a high/low conductivity. Two particularly promising types of this conductivity-switched nanoelectronic memory are molecular electronic memory devices and magnetic tunnel junction (MTJ) magnetic RAM (MRAM). Molecular memories have significant potential to outscale silicon memories in terms of raw density [1–3]. Several candidate devices exhibiting memory behaviour have been demonstrated [1, 4–6]. In most of these, the memory effect is displayed as a change in the conductivity of the molecule, which can be used to construct architectures based on crossbar circuits to implement random-access memory [2] with a $4F^2$ cell footprint.

MTJ MRAM devices have also been demonstrated as both 1MTJ1T cell RAMs [7–10] and in a denser configuration ($6F^2$) as crosspoint (XPC) arrays [11–13]. The two questions addressed in this paper are as follows. (1) What is the scaling potential of these nanoelectronic memories based on this class of conductivity-switched devices in crossbar arrays, i.e. can they outscale CMOS in terms of density? (2) What are the requirements for molecular and MRAM memories, and the supporting interconnect technology, to be able to outscale CMOS? For a fair comparison, only the transistor-less XPC MTJ MRAM cell is evaluated, as this is also the cell with the smallest footprint.

The promise of nanoscale electronics to deliver ultradense memory systems using novel device characteristics, especially in crossbar arrays without transistors integrated into the memory cells, requires novel approaches not only to circuit design, but also to circuit and system simulations [14, 15].

In this work, an approach to examine the scalability of nanoelectronic conductivity-switched random access memories will be described. In section 2, criteria for correct functionality will be established based on the readout margin. The RAM circuit model is described in section 3, from which a parametrized circuit template is developed for the case of an idealized interconnect. This template is then used in section 4 to evaluate scaling constraints from a device perspective. Finally, in section 5, circuit simulations on a full

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molecular RAM system are performed in order to examine the impact of a non-idealized interconnect on RAM scalability. Combining the results from the theoretical and the simulation approaches enables us to draw quantitative conclusions about the scalability of molecular-electronics-based RAM from both a device and an interconnect perspective.

2. Memory requirements

In order for memory to function correctly, it must be able to store and retrieve binary data with a low probability of corruption. Furthermore, there are several performance requirements on memory, such as density, size, power dissipation, retention time, speed, cost of production, yield etc. Each of these has different degrees of importance in different types of memory technologies, such as capacitor DRAM, six-transistor SRAM, FLASH, FeRAM etc. The two technologies investigated in this work, molecular RAM and XPC MTJ MRAM, share the basic properties of high density and nonvolatility. In addition, the characteristics of molecular memory effects include relatively large operating voltages [4], likely limited speed due to the large resistances involved [4, 5], long retention times [4], potential for ultrahigh density [1, 2] and low cost/bit [3]. These suggest that molecular memories would be most suitable for FLASH-type and other high density/low operating speed applications. MTJ MRAM technology, especially XPC-type MRAM, has been under development primarily as an embedded memory technology [10] due to relatively straightforward integration, compared to molecular memories, both in terms of processing and operational voltage, with CMOS processing and the combination of nonvolatility, high density and low access time. However, while specific performance requirements are demanded by these specific applications, the basic store–retrieve reliability remains fundamental. Thus, the scalability analysis will be based on the probability of bit errors, both static and dynamic, which translates into a readout margin.

In order to evaluate these memories fairly, comparisons should be made between these nanoelectronic type memories and the forecasts in the International Technology Roadmap for Semiconductors (ITRS) [16]. Although bit error rates for the primary semiconductor type of nonvolatile memories, FLASH technology, are not contained in the ITRS, a minimum of reliability for an order-of-magnitude comparison that should probably be met would be the DRAM error rate. DRAM-type systems are generally much more prone to single-event upsets than FLASH-type memories [17] and have higher error rates, but ECC could be used to improve on this upper bound, as has been shown for static faults in nanoelectronic memories [18], compensating for the discrepancy.

DRAM-type memory systems are predicted to maintain a soft error rate of 1000 fits (fits = failures in one billion operating hours) and an access time of 60 ns. This implies a probability of incorrect bits of

$$\frac{1000\ \text{fits}}{10^9\ \text{h}\frac{3600\ \text{s h}^{-1}}{60\times10^{-9}\ \text{s/cycle}}} = 1.667\times10^{-17}\ \frac{\text{failures}}{\text{cycle}}.$$

This probability of a bit error for DRAMs is used in this paper as a reliability target for molecular-based memory systems. The probability of an error depends on both the statistical distribution of noise and upset sources, as well as the statistical distribution of device characteristics. The latter variability is twofold—(1) the transient variability in device characteristics during continuous operation of a single device (i.e. the characteristics change over time); (2) the statistical distribution of device characteristics when comparing all molecular devices in the system.

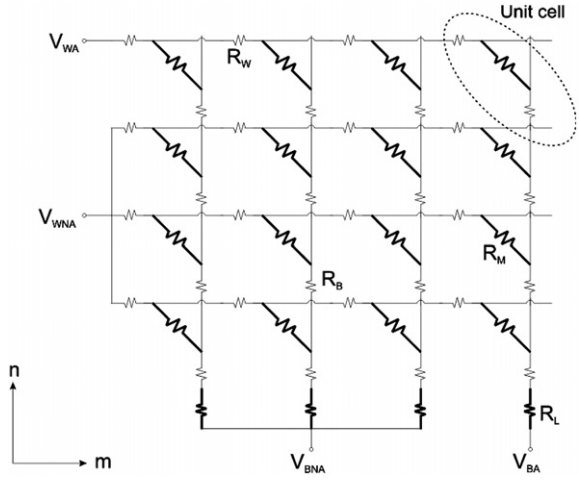

Figure 1. Memory array circuit ($m = n = 4$) modelled. Molecular memory devices at crosspoints have resistance R_M, load resistors R_L connected to bitlines, interconnect resistance of wordlines and bitlines is R_W and R_B, respectively.

In order for a memory to function properly with a given probability of a bit error, p, the probability of correctly interpreting the state of a particular memory cell must be larger than the probability of $1 - p$. A simple, commonly used method for determining the state of a memory cell in conductivity-based memories, which store the state of the cell as a conductivity state [1, 4–6], is to use a load (in the simplest case, a resistor) attached to the bitlines to construct a voltage divider, as shown in figure 1. Actual implementations utilize much more sophisticated types of loads, but the resistor serves as a useful abstraction. In this case the voltage across the load would serve as the input for a comparator circuit (see [19], for example). Under an applied voltage at the wordline, the voltage across the load resistor depends on the conductivity of the molecular element in the cell, and its state is detected using a sense amplifier, by comparing that voltage to a reference voltage.

Given a molecular device characteristic with two different states, with resistances R_{ON} for the high conductivity state and R_{OFF} for the low conductivity state, the value of the load resistance needs to be optimized for the maximum possible readout margin.

A general resistive m by n crossbar is shown in figure 1. The horizontal (word) lines have resistance mR_W; the vertical (bit) lines have resistance nR_B. These represent the interconnect resistance. A load resistor R_L is connected to the bitlines, and the resistors at the crosspoints, R_M, represent the molecular memory device. The value of R_M is either R_{ON} or R_{OFF}, depending on the state of the device.

The accessed memory cell is at the crosspoint of the accessed wordline, with voltage V_{WA} applied, and the accessed

bitline, which is biased to V_{BA}. V_{WNA} and V_{BNA} are applied at the remaining non-accessed wordlines and bitlines, respectively.

Ignoring interconnect resistance, the voltage across the load resistor is always determined by the voltage divider formed between the load resistance and the device resistance. Under these idealized circumstances of negligible interconnect resistance, V_{WNA} and V_{BNA} have no effect on the device, and a device in the array can be considered independently of the other cells in the array. Thus, the difference between the voltages across the load resistor in the two states is given as:

$$\Delta V_{OUT} = \mathrm{RM} = (V_{WA} - V_{BA})\left[\frac{R_L}{R_L + R_{ON}} - \frac{R_L}{R_L + R_{OFF}}\right]. \quad (1)$$

Taking the derivative with respect to R_L and setting it equal to zero,

$$\left.\frac{\partial(\Delta V_{OUT})}{\partial R_L}\right|_{R_L = R_{L\_Optimal}} = 0$$

$$0 = (V_{WA} - V_{BA})\left[\frac{1}{R_{L\_Optimal} + R_{ON}} - \frac{1}{R_{L\_Optimal} + R_{OFF}} - \frac{1}{(R_{L\_Optimal} + R_{ON})^2} + \frac{1}{(R_{L\_Optimal} + R_{OFF})^2}\right].$$

Solving for R_L yields

$$R_{L\_Optimal} = \sqrt{R_{ON} R_{OFF}}. \quad (2)$$

Therefore, assuming negligible interconnect parasitics, the maximum difference between the voltages, which is the readout margin, is achieved with a load resistor equal to the geometric mean of the two resistances of the memory device.

The assumption of negligible interconnect resistance is likely to be accurate for molecular memories in the case where the architecture relies on lithographically defined metal wires, such as in [1, 2]. Even nanoscale metallic wires have impedances that should be negligible compared to the device resistance. Most metals have bulk resistivity on the order of at least 10^{-6} Ω m, so lithographically defined nanowires (pitch ≅ 133 nm, width = 40 nm, height = 8 nm [2]) should have unit length resistance (R_W) on the order of 100–1000 Ω. This is still several orders of magnitude lower than the resistance of molecular devices [4, 5, 20, 21]. This, however, is not necessarily the case in architectures employing molecules as part of the interconnect structure, and a clear difference must be made between analysing these two cases. Similarly, MTJ devices have much lower resistances, so the interconnect impedance can become significant [12]. In either case, capacitive and inductive parasitic effects are neglected, since operating speed performance is not examined in this work.

The probability of correctly reading the memory state of the device depends on the sensitivity of the sense amplifier, as well as both the statistical distribution of the noise sources in the circuit and the statistical distribution of the device characteristics.

The latter two factors will cause the actual voltage across the load resistor in the two states to be a statistical distribution rather than a fixed value. A simple readout margin analysis can be performed for a statistical distribution of the on and off readout voltages around their respective nominal values, $V_{ON\mu}$ and $V_{OFF\mu}$, as illustrated in figure 2(A), where $\tilde{V}_{ON\mu}$ and $\tilde{V}_{OFF\mu}$ are modelled as a normal distribution.

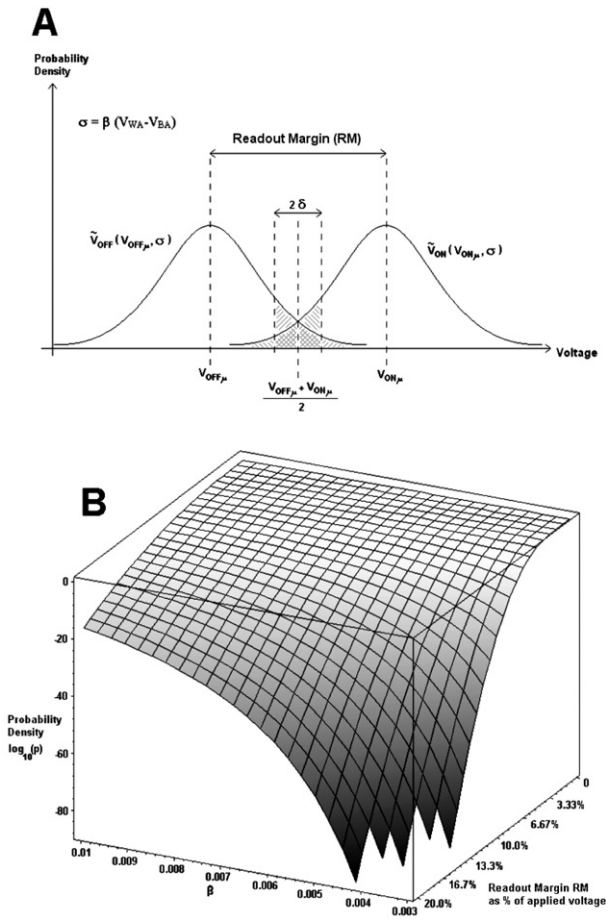

Figure 2. (A) Relationship between readout margin, device characteristic variability and probability of bit errors (shaded region). (B) Probability of bit error versus architecture variability parameter β and readout margin.

The magnitude of variability in the readout voltage is a function of the applied voltage. The switching noise in the circuit is an increasing function of the voltage applied. Also, for a given spread in device on and off resistances, increasing the applied voltage will translate linearly into an increased spread in the readout voltages. Thus, it is assumed that the standard deviation σ is approximately a linear function of the applied voltage, i.e.

$$\sigma = \beta(V_{WA} - V_{BA}).$$

The probability of a bit error, p, as indicated by the two shaded regions in figure 2(A), is the sum of the area under the V_{OFF} distribution that is greater than the maximum voltage that the sense amplifier reliably detects as a logic '0', and the area under the V_{ON} distribution that is smaller than the minimum voltage that the sense amplifier reliable detects as a logic '1'. Assuming that the sense amplifier has sensitivity 2δ around $(V_{OFF\mu} + V_{ON\mu})/2$, the resulting expression for readout margin, $V_{ON\mu} - V_{OFF\mu}$, with sense amplifier sensitivity 2δ, and the standard deviation of the V_{ON} and V_{OFF} distributions,

$\sigma = \beta(V_{WA} - V_{BA})$, is

$$p = P\left[\tilde{V}_{OFF} > \frac{V_{OFF\mu} + V_{ON\mu}}{2} - \delta\right] + P\left[\tilde{V}_{ON} < \frac{V_{OFF\mu} + V_{ON\mu}}{2} + \delta\right]$$

$$p = P\left[z > \frac{V_{OFF\mu} + V_{ON\mu}}{2\sigma} - \frac{\delta}{\sigma} - \frac{V_{OFF\mu}}{\sigma}\right] + P\left[z < \frac{V_{OFF\mu} + V_{ON\mu}}{2\sigma} + \frac{\delta}{\sigma} - \frac{V_{ON\mu}}{\sigma}\right].$$

These two terms are equal due to symmetry, so

$$p = 2P\left[z > \frac{V_{OFF\mu} + V_{ON\mu}}{2\sigma} - \frac{\delta}{\sigma} - \frac{V_{OFF\mu}}{\sigma}\right]$$

$$p = 2P\left[z > \frac{RM}{2\sigma} - \frac{\delta}{\sigma}\right]$$

$$p = 2P\left[z > \frac{RM - 2\delta}{2\beta(V_{WA} - V_{BA})}\right].$$

The readout margin, $RM = V_{ON\mu} - V_{OFF\mu}$, is related to the resistance on/off ratio by $RM = \Delta V = V_{ON\mu} - V_{OFF\mu}$, and since $R_L = \sqrt{R_{ON} R_{OFF}}$ the readout margin can be written as

$$RM = (V_{WA} - V_{BA})\left(\frac{R_L}{R_L + R_{ON}} - \frac{R_L}{R_L + R_{OFF}}\right) = (V_{WA} - V_{BA})\frac{1 - \frac{R_{ON}}{R_{OFF}}}{\left(\sqrt{\frac{R_{ON}}{R_{OFF}}} + 1\right)^2}. \quad (3)$$

Therefore, an MTJ MRAM TMR ratio of 45%, corresponding to an on/off ratio of 1.45, as reported in [7], results in a readout margin of 9.3% of the applied voltage in this load–resistor architecture. MTJ MRAM device variability has been demonstrated to be below 5% (one σ in resistance distribution) across a whole wafer. Working MRAM memories (albeit with unspecified yield/error rates) have been demonstrated using these devices [7], thus a 10% readout margin will be assumed for the purposes of quantitative values reported in this paper.

Unfortunately, there are very few data available on the device variations in molecular circuit elements, and the impact of noise sources in the circuit would heavily depend on the physical architecture of the RAM itself. Since these heavily influence the shape of this curve assumed for the V_{ON} and V_{OFF} distributions, the derived readout margin requirement of 10% should only be taken as a rough estimate, and the figures show trends for a range of readout margin requirements.

Thus, different molecular memory architectures could have widely varying values of the system-dependent parameter β, resulting in very system-specific, and widely varying, values for the required readout margin that achieves the desired error probability, as shown in figure 2(B) (assumed $\delta = 50$ mV, $V_{WA} - V_{BA} = 3$ V). A readout margin equal to 10% of the applied voltage $V_{WA} - V_{BA}$ for $p = 1.667 \times 10^{-17}$ implies $\beta = 3.952 \times 10^{-3}$. In terms of device design, this illustrates a key trade-off: large on/off ratios result in greater readout margins, and thus reduced constraints on the device variability. In either case, the constraint implied by this value can be relaxed somewhat by using approaches combining spare memory cells and ECC to alleviate those problems with the devices falling into the shaded tail areas in figure 2(A): this method was shown to be effective for repairing CMOL arrays with up to 2% of nanoelectronic devices falling outside specifications, i.e. defective [18].

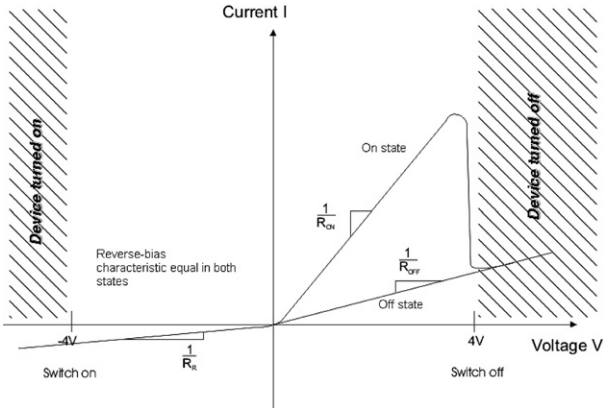

Figure 3. Current–voltage (I–V) characteristic of the modelled memory device. Voltages exceeding the negative threshold turn the device 'on'; voltages larger than the positive threshold turn it 'off'. The state is maintained so long as neither threshold is exceeded.

3. Memory equivalent circuit models

A memory is built from memory cells arranged in 2D arrays, as shown in figure 1 (a 4×4 array). A memory cell consists of the memory device as well as the wordline and bitline 'unit cell' resistance. The equivalent circuit for these 2D arrays, as shown in figure 1, consists of the distributed wire resistances in the wordlines (mR_W) and bitlines (nR_B), and devices (R_M) at the crosspoints between the wires. R_M can take on different values corresponding to the two conductivity states of the device, R_{ON}/R_{OFF}, if the device is positively biased, i.e. the wordline voltage exceeds the bitline voltage. In the case of negative (reverse) bias, it is assumed that the device resistance in both states is the same, R_R, for simplicity. This allows for the model to easily incorporate a rectifying (isolating) characteristic by setting $R_R \neq R_{ON}/R_{OFF}$. Leaving R_R an independent variable allows this model to be used both for MRAM XPC-type circuits as well as those employing rectifying 1R1D cells, if the series diode I–V is approximated as an ideal diode. Figure 3 shows the type of current–voltage (I–V) characteristic used for the purposes of this work. Load resistors, R_L, are present at the end of the bitlines for readout.

The performance evaluation of a particular set of parameters (n, m, R_W, R_B, R_{ON}, R_{OFF}, R_R) was based on a switching characteristic in which a molecular device changes its conductivity state from on to off and vice versa. The case for XPC MRAMs is analogous, only the parameter values change significantly [8]. The molecular device model used in this paper is based on the type of I–V characteristic demonstrated in [4], showing voltage-controlled switching between two stable conductivity states (see also [5, 6]). The model used in this paper assumes the state changes from on to off at +4 V and from off to on at −4 V.

The memory state of a particular word in the array can be written by first performing a reset on the wordline, by applying a large forward bias between the accessed wordline

Table 1. Driving voltages for different memory operations.

Parameter (V)	Reset	Write	Read
V_{WA}	6	−3	3
V_{WNA}	−1	−1	−1
V_{BA}	0	2	0
V_{BNA}	0	0	0

and all bitlines. This forces all the molecules on that accessed wordline into the nonconductive state. By then applying a reverse bias between the wordline and selected bitlines, a write operation is performed by forcing targeted molecules into the conductive state while leaving the rest unchanged. Examining the memory states of cells on a wordline is accomplished by forward-biasing the accessed wordline while reverse-biasing all other wordlines, and reading the voltage drop across the load resistor. The operational parameters assumed for the purposes of this paper are summarized in table 1.

The two critical parameters are the voltage drop across the molecule, and the difference in the voltage drop across the load resistor for the two molecular conductivity states, both relative to the voltage applied between wordline and bitline at the edge of the array. The first value pertains to the reset and write operations, while the second, more critical, value pertains to the read operation. The actual voltage appearing across memory cells is influenced not only by the location of the cell in the array—cells located near the edge of the array, near the wordline and bitline drivers, suffer much less voltage degradation than those located far from the drivers—but also by the state of other cells in the array. The appropriate worst-case scenario has to be examined, in order to evaluate the critical parameters correctly. The voltage across the load resistor depends on the amount of current flowing through the bitline. As soon as a slight parasitic interconnect resistance R_W is present, current division occurs at each crosspoint along the wordline, between the path continuing through the rest of the wordline and the path through the molecular device into the bitline. An analogous effect occurs on the bitline [13]. This is why the interconnect resistance cannot be assumed to be negligible for the purpose of this analysis. The magnitude of current on the wordline that is divided away depends on the ratio of the input resistance of the rest of the wordline and the input resistance of the bitline, which depends largely on the state of the molecular device. Thus, the state of the other devices on the wordline affects the amount of current flowing through the one under consideration. Therefore, in the case of a read, the readout margin between reading a '1' and a '0' has to be taken as the difference between reading the conductive cell with the worst degradation, farthest from the drivers, when all other cells on this worst-case wordline are also conductive, and reading a nonconductive cell with the least degradation, closest to the drivers, when all other cells on that best-case wordline are also nonconductive.

It is important to note that the allowable probability of a bit error imposes a significant constraint on the allowable range of device variability in this architecture. Even in the idealized case without any noise sources, and assuming a reasonable sense-amp sensitivity at the readout (100 mV for a single-ended architecture), the variability of the on and off state resistances of the molecular device would have to be small. As discussed above, a spread in device resistance would result in a spread in the readout voltages. This can lead to situations where a given device may have an on-resistance high enough that it is interpreted by the sense-amp as an off, and vice versa, leading to static stuck-at type faults. For a read operation, if both on and off state resistance of a device varies as it operates, and that variability is distributed normally with a standard deviation larger than just 8% of the mean values (the nominal on/off ratio is assumed to be 10/1), the resulting spread in the readout voltage would cause faults at a rate worse than the CMOS target of 1.667×10^{-17} cited above. This necessitates high on/off ratios and/or smart circuit design for the readout circuits; the illustrative resistive load will not be adequate. Improved nominal on/off ratios obviously have a large positive impact on the allowable variability, but in general a device needs to have a well characterized, stable resistance in both states over its lifetime.

The remainder of this paper focuses on the relationship between readout margin and the device and array characteristics.

4. Scalability analysis

Circuit simulations using commercial HSPICE circuit simulation software[4] of the RAM circuits up to 128 × 128 arrays were performed. Molecular devices were modelled as resistive elements with values depending on their bias and conductivity state. Default values for the parameters were chosen based on experimental data for the memory molecule [4], as well as molecular interconnect 'wires' [21] or, alternatively, lithographically defined nanoscale metal wires. For the purpose of this study of voltage-switched molecular devices, the absolute value of these parameters is immaterial; only their relative ratios matter. The study was performed using parameters estimated for a molecular memory; a similar study can be performed for XPC MRAM using this approach with different values for the parameters. In general, MTJ MRAM devices have much higher conductivity than molecular devices, so the higher interconnect-device impedance ratio makes the interconnect resistance a much larger factor [12], compared to molecular memory with lithographic interconnects. Also, their lower on/off ratios present formidable design challenges for large-scale XPC readout circuitry. In a demonstrated [13] 4 kbit array, 97% of the readout current was due to parasitic leakage paths.

By varying a single parameter at a time, the impact of each parameter on the scalability of the memory is determined. This approach was chosen over a full combinatorial analysis, where all sets of parameters within a range are evaluated, due to the large size of the combinatorial space that would have to be explored. Also, due to the increasing computation time, simulations were not extended beyond 128 × 128 arrays (16 kbit). In order to overcome the practical limitations imposed by the computational complexity, a theoretical model was used to evaluate the scalability of molecular memories of practical sizes. In order to develop this model, negligible interconnect resistance had to be assumed. This means that it is only valid for structures using low resistance, lithographically defined interconnects, as explained above.

[4] Avant! Corporation: Star-HSPICE 2001.2 and AvanWaves 2001.2.

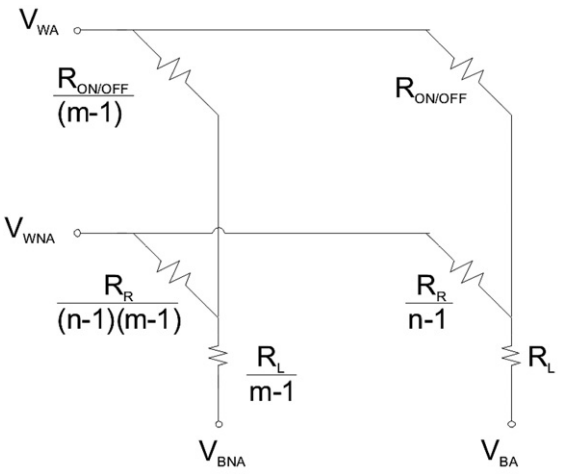

Figure 4. Parametrized RAM circuit model for evaluating array scalability.

Using various circuit transformations, this assumption leads to a simple equivalent circuit template for the RAM circuit, as shown in figure 4, that is parametrized by the RAM dimensions. The driving voltages for (non-)accessed wordlines/bitlines are labelled $V_{\mathrm{W/B(N)A}}$. The single device in the top right corner labelled $R_{\mathrm{ON/OFF}}$ represents the worst-case cell farthest from the word- and bitline drivers. This derived circuit template was used to perform scalability evaluations for the case of negligible interconnect resistance, as it allows evaluation of large arrays with reasonable computational complexity. A number of technological factors can limit the scalability of the array.

4.1. Limitations imposed by device on/off ratio

Given their nanoscale nature, molecular devices are unlikely to achieve the on/off ratios of larger silicon devices, due to the presence of tunnelling currents that are unavoidable at the nanometre-scale dimensions (e.g. as evidenced in nanometre-scale gate dielectrics [22]). Thus it is important to establish the limits on scalability presented by this ratio. MTJ MRAM devices currently have on/off ratios around 1.3 to 1.5 [7], albeit with good reproducibility, which is not necessarily expected of molecular devices.

Using the circuit template shown in figure 4, analytical solutions were obtained for the readout margin for given device parameters and voltage biases. Simulations generally showed the read operation to be the most critical in terms of operational margin. The readout margin can be derived based on circuit theory. Using the superposition principle and summing up the contributions of the three voltage sources yields the readout voltage across R_{L} in the V_{BA} branch:

$$V_{\mathrm{OUT}} = \frac{R_{\mathrm{L}} R_{\mathrm{R}} V_{\mathrm{WA}}}{(n-1)\left(R_{\mathrm{L}} + \frac{R_{\mathrm{R}}}{n-1}\right)\left(\frac{R_{\mathrm{L}} R_{\mathrm{R}}}{(n-1)\left(R_{\mathrm{L}} + \frac{R_{\mathrm{R}}}{n-1}\right)} + R_{\mathrm{M}}\right)} + \frac{R_{\mathrm{L}} R_{\mathrm{M}} V_{\mathrm{WNA}}}{(R_{\mathrm{L}} + R_{\mathrm{M}})\left(\frac{R_{\mathrm{L}} R_{\mathrm{M}}}{R_{\mathrm{L}} + R_{\mathrm{M}}} + \frac{R_{\mathrm{R}}}{n-1}\right)} - \frac{R_{\mathrm{L}} V_{\mathrm{BA}}}{R_{\mathrm{L}} + \frac{R_{\mathrm{M}} R_{\mathrm{R}}}{(n-1)\left(R_{\mathrm{M}} + \frac{R_{\mathrm{R}}}{n-1}\right)}}. \quad (4)$$

Notice that due to the ideal interconnect, V_{BNA} does not enter this equation, as all paths from V_{BNA} to R_{L} go through nodes tied directly to a voltage source, and thus the number of bits per word, m, has no impact on scalability if interconnect is ideal. Given an on/off ratio of k and assuming that the molecular negative-bias resistance is the same as the off-state resistance, i.e. $R_{\mathrm{OFF}} = R_{\mathrm{R}}$, and that $R_{\mathrm{L}} = R_{\mathrm{L\_optimal}}$, the readout voltage if the molecule is conductive, i.e. has resistance equal to R_{ON}, is

$$V_{\mathrm{OUTon}} = \frac{\sqrt{k}(kV_{\mathrm{WA}} + V_{\mathrm{WNA}}n - V_{\mathrm{WNA}} - V_{\mathrm{BA}}n + V_{\mathrm{BA}} - kV_{\mathrm{BA}})}{k^{\frac{3}{2}} + \sqrt{k}n - \sqrt{k} + k}. \quad (5)$$

Similarly, the readout voltage for a nonconductive molecule is

$$V_{\mathrm{OUToff}} = \frac{\sqrt{k}(kV_{\mathrm{WA}} + kV_{\mathrm{WNA}}n - kV_{\mathrm{WNA}} - kV_{\mathrm{BA}}n)}{k^{\frac{3}{2}}n + k^2}. \quad (6)$$

The difference of the V_{OUT}s between a conductive and a nonconductive molecule, given as R_{ON} and R_{OFF} respectively, then yields the readout margin as

$$\mathrm{RM} = \{(k-1)(n-1)(V_{\mathrm{WA}} - V_{\mathrm{WNA}}) + (k^{\frac{3}{2}} - \sqrt{k})(V_{\mathrm{WA}} - V_{\mathrm{BA}})\} \{(k - 1 + \sqrt{k} + n)(\sqrt{k} + n)\}^{-1}. \quad (7)$$

Figure 5 shows the relationships between the achievable memory size, the device on/off ratio and the readout margin defined by (7) for the read operation as specified in table 1.

For a 64 × 64 memory, if interconnect resistance is negligible, an on/off ratio of $R_{\mathrm{OFF}}/R_{\mathrm{ON}} = 7/1$ is sufficient to achieve a 10% readout margin, while a 43/1 ratio is needed for 512 × 512. Thus, even allowing for significant device variation, it is likely that the on/off ratios of current molecular devices will be large enough that it will not be the most critical limitation to the scalability of molecular memory circuits. For the case of MTJ MRAM circuits, the low on/off ratios require very sensitive readout circuitry, and although the uniformity of MTJ junctions has been improved to mitigate the probability of defects/errors, improving the TMR remains one of the most critical factors in building large-scale arrays.

4.2. Limitations imposed by word and bit line resistance

When the total wire resistance (along a word or bit line) starts becoming comparable with the load resistance (geometric mean of the on and off resistances), the wire resistance becomes a significant limit on the scalability of the array. In the case of molecular electronics, this is the likely case when the RAM architecture of a system relies on molecular-based interconnect, as stated above.

The fraction of the applied voltage that is dropped across the load resistor cannot exceed that formed by a voltage divider with nR_{B}, mR_{W}, and the molecular device. Thus, if the total wire resistance becomes a significant factor, that fraction quickly diminishes. Simulations also showed that modelling the interconnect as a single lumped resistor did not yield the

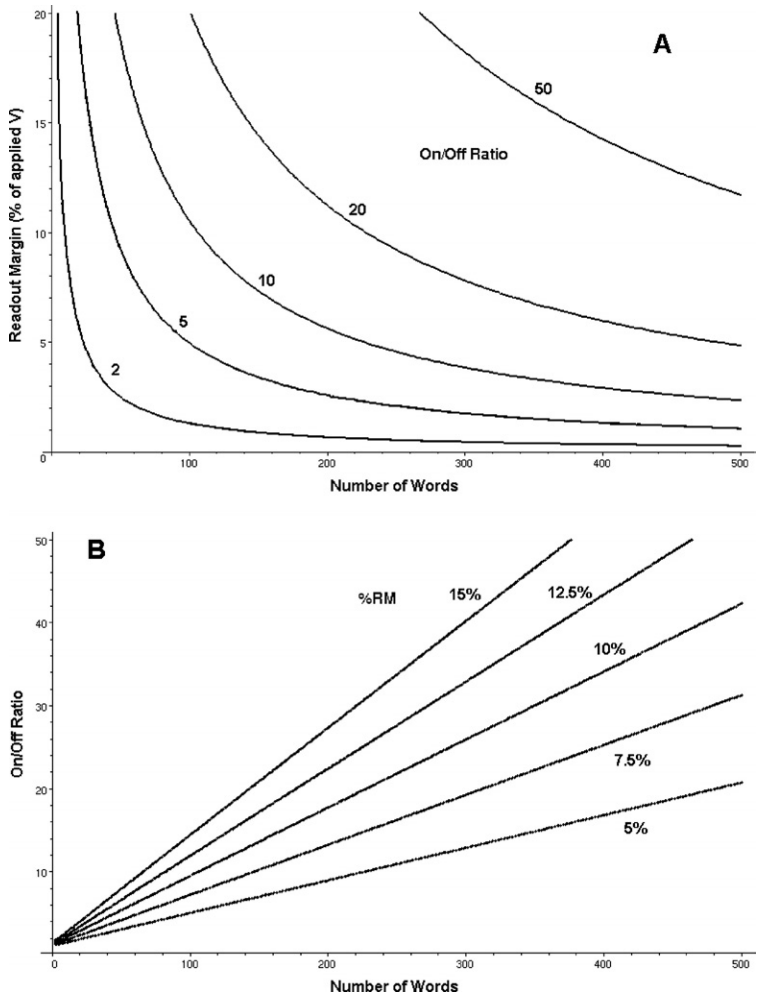

Figure 5. Relationship between memory size (in number of memory words), device on/off ratio, and readout margin (as a percentage of the applied wordline bias). (A) Readout margin versus number of words for different on/off ratios, (B) on/off ratio versus number of words for different readout margins.

necessary accuracy, and that the accuracy of such a lumped model decreased with increasing size of the memory. Under those conditions, a simple lumped model does not accurately model the input resistance of the word- or bitline, which look more like ladder circuits. Thus, it is neither possible to use the simplified circuit template, nor to use a lumped model for the word- and bitline resistance. Thus, numerical simulations were performed for the case of significant word-/bitline resistance, where the interconnect resistance was distributed over the entire length of the wordline, as shown in figure 1.

Table 2. Default parameters for the simulated memory system.

Parameter	Value
R_{ON}	10 MΩ
R_{OFF}	100 MΩ
R_R	1 GΩ
R_W	100 kΩ
R_B	100 kΩ
n	16
m	16

5. Simulation results

The readout margin dependence on the different resistance parameters is shown in figure 6 for the default 16 × 16 RAM. The different curves show how the readout margin (given as a percentage of the applied wordline bias) changes, as a single resistance parameter in table 2 is varied at a time, while all others are held at their default values. The curves are then normalized by the default value of the parameter varied, so they can all be plotted on the same x-axis, which represents the factor by which the parameters differ from their default values. Given a system with the default parameters, the readout margin is 32% of the applied wordline bias. Parameters with the largest impact on readout margin can be easily distinguished, as they exhibit the largest derivatives around the origin, which corresponds to the default ratio of 1 (corresponding to the default values). Curves that remain flat show that there is little dependence of the readout margin on this parameter; it does not change as the parameter is varied, thus the steepest slopes represent the parameters with the greatest influence on the readout margin.

Similar graphs were obtained for the reset and write operations, but functionality does not degrade as fast for these two operations.

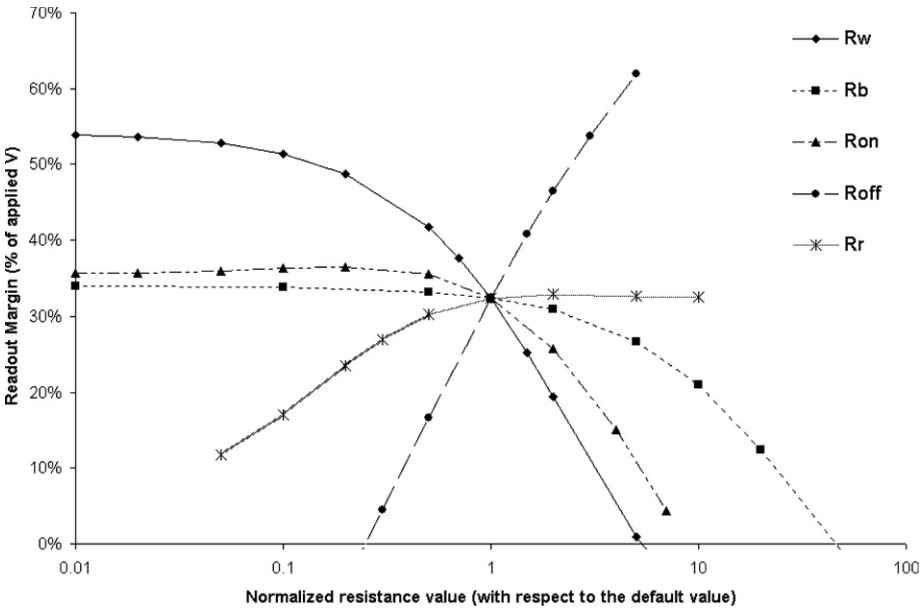

Figure 6. Readout margin dependence on resistance parameters when varied one at a time, all others being kept at their default values (the 16 × 16 memory described in table 2).

For the chosen set of default parameters, the wordline resistance R_W and the device off resistance R_{OFF} have the largest impact on the readout margin.

In general, R_W has a larger impact on the readout margin than the bitline resistance, R_B. This is due to the fact that the reverse-bias resistance of the devices is assumed to be larger than the forward-bias resistance, showing quantitatively that it is advantageous to have a cell with an isolating characteristic. The current division that occurs at each cell along the wordline is much more unfavourable than that which occurs along the bitline. In terms of current division, considering the current path from the wordline driver, through the wordline, through the device being read, through the bitline, through the load resistor into ground, relatively more current is diverted into different bitlines along the wordline than vice versa. This is because the input resistance of the bitline at each step progressing along the wordline is related to the forward-bias resistance of the device, whereas the input resistance of the wordline at each step along the bitline is related to the reverse-bias resistance of the device. Due to the smaller device forward-bias resistance, the current will tend to divert through the other devices into the bitlines, leading to 'current starvation' and a lower readout margin at the worst-case cell at the end of the wordline. For the chosen parameters, R_W starts becoming a significant factor when it is about one order of magnitude less than its nominal value, corresponding to mR_W about two orders of magnitude less than R_L. Thus, in a completely molecular-electronics-based architecture using molecular (i.e. significantly resistive) interconnect, the word- and bitline resistivity would quickly become a limiting factor, as some experimental measurements of the conductance of molecular wires relative to the switching molecules have shown one to two orders of magnitude difference in conductivity [21].

Figure 7 shows this behaviour, as the relative readout margin (as a percentage of applied wordline bias) plotted against the number of words in a square RAM (#wordlines = #bitlines). The solid line represents the RAM with the default resistance parameters, with a 100:1 ratio of device on resistance, R_{ON} to wordline resistance, R_W, which is assumed to be equal to the bitline resistance R_B. The 10% readout margin is not met for a 32 × 32 RAM. Only improved interconnects could yield large-scale memories, as shown for interconnects that are three to five orders of magnitude as conductive as the device in its on state. Based on the graphs above, a rule of thumb could be constructed, that the number of bits in the memory should not exceed the interconnect-to-device conductivity ratio R_W/R_{ON} by more than a factor of four to five.

6. Conclusions

In this paper, the scalability of nanoelectronic based random access memory systems was examined. To this end, a relationship for the memory readout margin separating the '0' and '1' bits and the allowable probability of an error was analysed and compared to CMOS-based RAM circuits. Several properties were identified that would potentially allow molecular-based RAM and MTJ MRAM to compete with CMOS under certain assumptions, such as the large on/off ratios of molecular-based RAM, and the high density of nanoelectronic memory that mitigate the likely need to insert ECC logic to compensate for faults. Assuming idealized interconnect, the maximum readout margin was derived as a function of the load resistance. A novel simplified equivalent circuit model was developed which allowed one to investigate the relationship of on/off ratio (or its MRAM equivalent TMR) to scaling. Using this equivalent circuit in a model of a sample nanoelectronic architecture, it was shown that a memory device with a reliable and repeatable 7/1 on/off ratio could be scaled up to a 64 × 64 array in a low parasitic architecture, while a 43/1 on/off ratio could be scaled to 512 × 512.

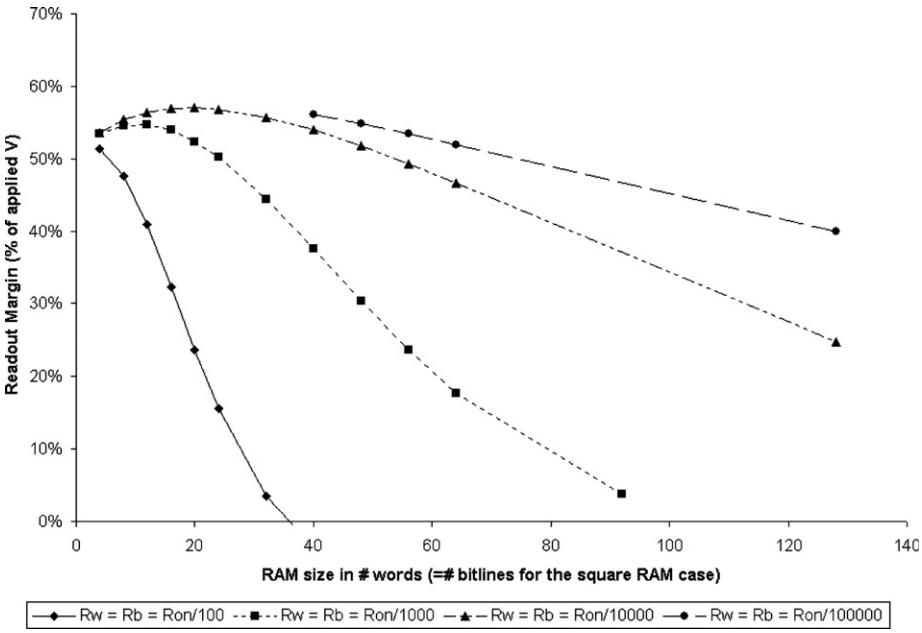

Figure 7. Readout margin dependence on memory size when parasitic interconnect resistance is significant.

Numerical calculations on a sample system using interconnect with significant resistance showed that the wordline resistance, more so than bitline resistance, and the device off resistance had the largest impact on the readout margin. Under these assumptions, establishing an equivalent circuit model is nontrivial as lumping the interconnect resistivity can give inaccurate results. Overall a case study of a sample molecular memory system was presented, from which design guidelines were extracted. This case study shows that it is very important for a molecule to have a very low conductivity off state compared to the other parameters in the system, and for architectures to use the best interconnect possible. In this model, the scalability of the number of bits in the memory system was generally limited to the device–interconnect resistivity ratio multiplied by a factor of four to five. The effect of this interconnect resistance was investigated further; the results of which showed similar trends that only improved interconnect could yield large-scale memories. Thus, the feasibility of scaling nanoelectronic random access memories was shown both in terms of device design and interconnect requirements.

Acknowledgments

This work was supported in part by the US Department of Defense under DARPA grants N00014-01-1-0657 and F29601-00-D-0244.

References

[1] Chen Y, Ohlberg D A A, Li X, Stewart D R, Williams R S, Jeppesen J O, Nielsen K A, Stoddart J F, Olynick D L and Anderson E 2003 Nanoscale molecular-switch devices fabricated by imprint lithography *Appl. Phys. Lett.* **82** 1610–2

[2] Chen Y, Jung H-Y, Ohlberg D A A, Li X, Stewart D R, Jeppesen J O, Nielsen K A, Stoddart J F and Williams R S 2003 Nanoscale molecular-switch crossbar circuits *Nanotechnology* **14** 462–8

[3] Hutchby J A, Bourianoff G I, Zhirnov V V and Brewer J E 2002 Extending the road beyond CMOS *IEEE Circuits Devices Mag.* **18** 28–41

[4] Reed M A, Chen J, Rawlett A M, Price D W and Tour J M 2001 Molecular random access memory cell *Appl. Phys. Lett.* **78** 3735–7

[5] Collier C P, Wong E W, Belohradsky M, Raymo F M, Stoddart J F, Kuekes P J, Williams R S and Heath J R 1999 Electronically configurable molecular-based logic gates *Science* **285** 391–4

[6] Bandyopadhyay A and Pal A J 2003 Large conductance switching and memory effects in organic molecules for data-storage applications *Appl. Phys. Lett.* **82** 1215–7

[7] Tehrani S T *et al* 2003 Magnetoresistive random access memory using magnetic tunnel junctions *Proc. IEEE* **91** 703–14

[8] DeBrosse J *et al* 2004 A high-speed 128-kb MRAM core for future universal memory applications *IEEE J. Solid-State Circuits* **39** 678–83

[9] Tehrani S, Engel B, Slaughter J M, Chen E, DeHerrera M, Durlam M, Naji P, Whig R, Janesky J and Calder J 2000 Recent developments in magnetic tunnel junction MRAM *IEEE Trans. Magn.* **36** 2752–7

[10] Reohr W *et al* 2002 Memories of tomorrow *IEEE Circuits Devices Mag.* **18** 17–27

[11] Wang F 2000 Diode-free magnetic random access memory using spin-dependent tunneling effect *Appl. Phys. Lett.* **77** 2036–8

[12] Zheng Y, Wang X, You D and Wu Y 2001 Switch-free read operation design and measurement of magnetic tunnel junction magnetic random access memory arrays *Appl. Phys. Lett.* **79** 2788–90

[13] Sakimura N, Sugibayashi T, Honda T, Miura S, Numata H, Hada H and Tahara S 2003 *A 512Kb Cross-Point Cell MRAM,* ISSCC paper 16.1

[14] Stan M, Franzon P, Goldstein S, Lach J and Ziegler M 2003 Molecular electronics: from devices and interconnect to circuits and architecture *Proc. IEEE* **91** 1940–57

[15] Ziegler M M, Picconatto C A, Ellenbogen J C, DeHon A, Wang D, Zhong Z and Lieber C M 2003 Scalability simulations for nanomemory systems integrated on the molecular scale *Mol. Electron. III Ann. New York Acad. Sci.* **1006** 312–30

[16] SEMATECH Corp. Austin, TX 2001 *International Technology Roadmap for Semiconductors* 2001 edn (online) Available: http://public.itrs.net

[17] Gregori S, Cabrini A, Khouri O and Torelli G 2003 On-chip error correcting techniques for new-generation flash memories *Proc. IEEE* **91** 602–16

[18] Strukov D B and Likharev K K 2005 Prospects for terabit-scale nanoelectronic memories *Nanotechnology* **16** 137–48

[19] Wicht B, Schmitt-Landsiedel D and Paul S 2001 A simple low voltage current sense amplifier with switchable input transistor *Proc. 27th European Solid-State Circuits Conf. (Villach, Austria, Sept. 2001)* pp 300–3

[20] Chen J, Reed M A, Rawlett A M and Tour J M 1999 Large on–off ratios and negative differential resistance in a molecular electronic device *Science* **286** 1550–2

[21] Blum A S, Yang J C, Shashidhar R and Ratna B 2003 Comparing the conductivity of molecular wires with the scanning tunneling microscope *Appl. Phys. Lett.* **82** 3322–4

[22] Frank D J, Dennard R H, Nowak E, Solomon P M, Taur Y and Wong H-S P 2001 Device scaling limits of Si MOSFETs and their application dependencies *Proc. IEEE* **89** 259–88