The Performance and Experimental Results of a Multiple Bit Rate Symbol Timing Recovery Circuit for PSK Receivers

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Abstract

A low-power all-digital symbol timing recovery circuit for digital PSK transmission systems is implemented in a 0.35-μm Silicon On Insulator (SOI) technology. The symbol timing circuit is designed for a wide range of bit rates (0.1-100 Kbps) and robust against fast and large Doppler shift or frequency error on the input signal. The system is therefore well-suited for receivers in deep-space and satellite applications. It is synchronized within 3 or 4 bits and the total power dissipation of the circuit is only 310 μW.

1. Introduction

In digital communications, symbol timing is essential at the receiver site to detect the transmitted data correctly. Many forms of symbol timing recovery (STR) circuits have been used. The most common traditional STR circuits are square-law [1], maximum-likelihood [2][3] and early-late gate [3]. However, the implementations of these STR circuits are complex and costly. They require longer synchronization time and therefore are not well suited for burst transmission. To take advantage of low-power and flexibility, it is desirable to implement STR circuits all-digitally. Digital approach of PLL to implement in STR circuits has also been studied at system level [4] [5]. However, they cannot be employed directly in space communications due to the effect of Doppler on the received signal.

This paper introduces a new approach to digital STR circuits for low-cost and low timing error for PSK receivers in space communications. Unlike conventional analog or digital STR's , the proposed STR circuit consists of a 1-bit A/D converter (ADC) at the front to convert analog signal to digital NRZ signal, a pre-filter to eliminate frequency error as well as circuit error, and then an all-digital PLL-like feed back system. In addition, the circuit is designed for multiple bit rates and can extract the timing clock from either a phase-shift keyed (PSK) modulated signal or a demodulated baseband signal by using a serial XNOR or XOR gate, respectively. The measurement results show that the circuit is synchronized within 3 or 4 bits and exhibits low jitter.

The circuit is implemented in SOI CMOS technology due to its low-power and radiation hardness characteristics [6]. Figure 1 shows the cross-section of a typical SOI CMOS device. Unlike bulk CMOS, the buried oxide SiO2 is used to isolate the active device thin-film region from the substrate. Hence the parasitic capacitances of SOI CMOS devices are

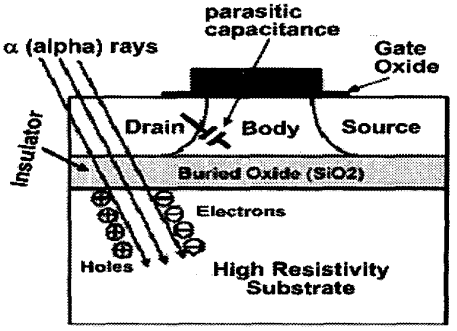

Figure 1. SOI CMOS device

smaller than those of bulk ones. The ability to reduce parasitic capacitances in SOI technologies allow circuits to operate with lower supply voltages, thus reducing the system power consumption and improving speed as well. Therefore, SOI CMOS has been becoming one of the major technologies for next generation receiver circuits. As depicted in Figure 1, due to the isolation between the active region and the substrate, SOI CMOS provides excellent immunity against high-energy particle that exists in space [6]. Having the features of the radiation hardness and robustness against Doppler shift, the proposed STR circuit is well suited for receivers in deep-space and satellite applications.

2. All-Digital Symbol Timing Recovery Circuit

The proposed symbol timing recovery technique is for a PSK modulated channel. As an example, in Figure 2, a digital-IF Binary PSK (BPSK) receiver with symbol timing recovery is illustrated. As shown in this configuration, the symbol timing clock can be recovered by using either the digital IF PSK signal or the demodulated output signal.

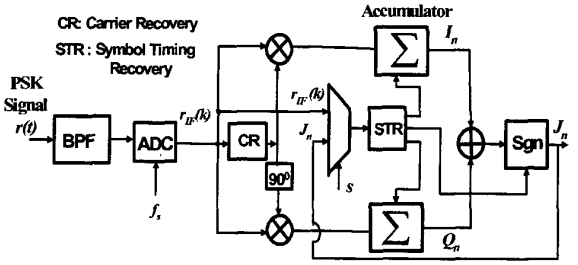

Figure 2. A block diagram of the digital-IF BPSK demodulator with symbol timing recovery

The block diagram of the proposed symbol timing recovery circuit for digital PSK receivers is illustrated in Figure 3. Design parameters are given in Table I. First, input analog signal is converted to digital non-return to zero (NRZ) signal by the 1- bit A/D converter (ADC). And then the rest of the circuit is realized digitally. A sequence of '1010..' or '0101' is sent for timing locking at the beginning and '10' is added to data after every 6 bits to introduce enough transitions in order for the timing circuit to track the data accurately. From test results, the length of preamble bits for the worst cases is observed to be 4 bits (i.e. N_L =4 bits). The divider scaling factor N is programmable and controlled by the Frequency Controller unit based on the frequency of the incoming signal. The Frequency Divider is designed as an increment-decrement counter. As an example, if f_s= 4 MHz and the required clock is for data rate of 100 Kbps, N must be 40 (i.e. $f_s/40$ = 100 KHz).

After the 1-bit ADC, the NRZ signal $s(k)$ and the delayed replica $s_d(k)$ are passed through XOR or XNOR gate to obtain a modified return-to-zero (RZ) signal $z(k)$ (e.g. $Z(t)=S(t).S(t-\tau)$). The selection of XOR or XNOR gate is based on the input signal. As indicated in Figure 3, if the input is a PSK modulated signal which is taken directly from the front-end of the receiver after the ADC (Figure.2), XNOR needs to be used. Otherwise, XOR is used for the demodulated baseband signal. The motivation behind this is to be able to obtain the transition pulses $y(k)$, as explained in Figure 4. Here the ADC is assumed to be 1-bit which can be employed in space communications due to the absence of interference in deep-space environment [7]. The "Prefilter" circuit passes only those pulses having pulse width greater than or equal to $\tau = 2T_s$ = 500 ns and thus eliminates all smaller pulses (caused by Doppler and circuit noise). The circuit is therefore robust against fast Doppler rate with the use of Prefilter unit which is a narrow-band digital filter. The delay is selected as $2T_s$ because it is equal to the duration of each pulse in the digital PSK signal (Figure 4).

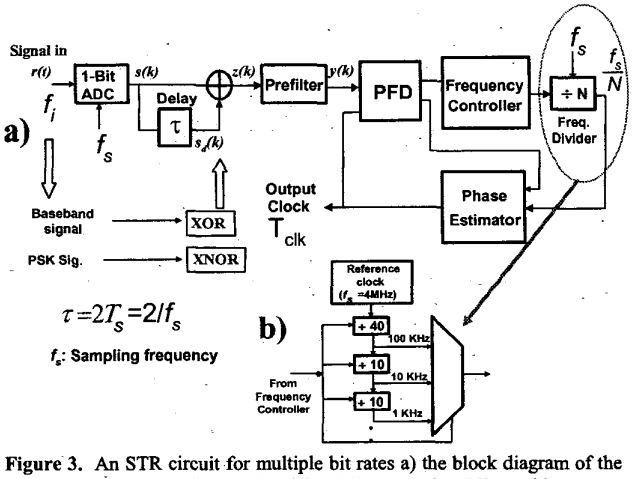

Figure 3. An STR circuit for multiple bit rates a) the block diagram of the STR circuit, b) the implementation of divider stages for different bit rates.

TABLE I. STR circuit parameters	
Input signal frequency, f_i	1 MHz
Sampling frequency, f_s	4 MHz
Data rates, f_b	0.1-100 Kbps
Length of preamble, N_L	4 bits
Power dissipation	310μW @2v

Another important feature of the proposed STR is its ability to recover timing clock (T_{clk}) for multiple bit rates (0.1 Kbps, 1 Kbps, 10 Kbps and 100Kbps). The selection of those bit rates are based on the requirement of space applications [7] which was primary target of this STR circuit. The Frequency Controller unit selects the appropriate down conversion stage depending on the frequency and phase of the incoming data signal (Figure 3-(b)). The reference clock is the sampling clock f_s which is already available in all digitally-implemented receivers. The phase synchronization is done by Phase Estimator unit together with the counters used for frequency division. Like all other units, it uses the sampling clock as a reference to detect the phase. The system is locked when the phase error is within the duration of the sample clock period T_s. In other words, there is a phase ambiguity of $\pm T_s$ (= ±250 ns) which is quite small considering small data rates ($T_s << T = 1/f_{b\text{-}max}$= 10 μs).

The timing diagram of the STR circuit where the input is a PSK modulated signal is displayed in Figure 4. If the input signal $s(k)$ and the delayed replica $s_d(k)$ are passed through XNOR, the transition pulses $z(k)$ will be obtained. The input is a digitized PSK signal obtained at the output of the 1-bit ADC. There is an 180° phase difference between bit "1" and bit "0" in a binary PSK modulated signal. Note that the small error pulses in $z(k)$ are eliminated after passing $z(k)$ through Prefilter. If one calculates the power spectrum of $y(k)$, it would show the existence of discrete spectral lines at multiples of the data rate frequency because the pulses are repeated every period of data rates [4]. Finally, the loop behaves as a narrow-band tracking filter and recovers output clock T_{clk} by using the modified RZ signal $y(k)$.

The most critical block in the system is the delay unit. Recall that the Prefilter detects the pulses having the width of $2T_s$.

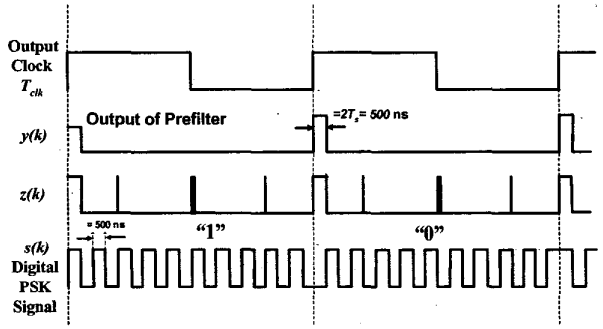

Figure 4. Timing diagram of the STR circuit for a PSK input signal

Every transition (from bit "1" to "0" or "0" to "1") is very important since the remaining part of the STR circuit uses transition pulses to generate the timing clock. To guarantee having width of $2T_s$ for every transition pulses in $z(k)$, the delay unit is implemented as given in Figure 5. Two flip-flops with the inverter chain will give a delay slightly bigger than $2T_s$. As a result, none of transition pulses will be lost after pre-filtering.

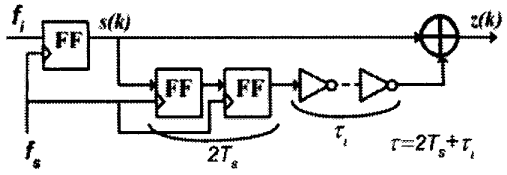

Figure 5. Implementation of the delay unit

To analyze the STR circuit assume that the input is a phase-modulated sine wave. The input waveform to the ADC can thus be described as

$$r(t) = A\cos(2\pi(f_i + \Delta f)t + \phi_i(t)) + n(t) \qquad (1)$$

where A is the amplitude of the signal, f_i is the input signal frequency which is usually a carrier frequency f_c or a downconverted IF frequency f_{IF}, Δf is the frequency offset generally caused by Doppler as well as oscillators' instability, the information is modulated on the phase ϕ_i, and $n(t)$ is additive white Gaussian noise from the communication channel.

The sampling frequency f_s is chosen as $f_s=4/(2n+1)f_i$, where n is an integer number. The principal motivation behind this sampling rate is that it reduces the hardware complexity when employed at the front-end of receivers [7][8]. As indicated earlier, the reference clock for the proposed STR circuit is the sampling frequency. This is one of the advantages of digitally-implemented receivers, eliminating the need for a separate oscillator to generate a reference clock.

In case of n >1, the input signal will be sampled with a frequency lower than the Nyquist rate (i.e. *subsampling*) [7][8]. To avoid aliasing, the sampling frequency must be at least twice the data rate (i.e. $f_s \geq 2f_b$) or the bandwidth of band pass filter (BPF) which is used at front-ends of most receivers [8]. In circuit simulations we particularly chose the sampling frequency equal to 4 MHz (i.e. f_s=4 MHz). Table II shows some examples of input frequencies with appropriate sampling factors based on the equation given in above. Here we assume the input signal is a PSK modulated signal not a demodulated signal. However, when the input signal is a demodulated baseband signal (i.e. $f_i=f_b$) we cannot mention subsampling in this case since $f_s>>f_b$.

After being sampled at $t=kT_s$, the signal (1) will be given by

$$r(k) = A\cos\{(2n+1)\pi k/2 + 2\pi\frac{\Delta f}{f_s}k + \phi_i(k)\} + n(k) \qquad (2)$$

TABLE II. Input frequencies for f_s= 4 MHz.	
Input signal frequency, f_i	Sampling factor, n
1 MHz	0 (oversampling)
3 MHz	1 (subsampling)
5 MHz	2 (||)
25 MHz	12 (||)

The signal is actually 1-bit quantized (i.e. hard-limiting) to obtain NRZ data $s(k)$. At the output of the 1-bit ADC, the signal can be written as

$$s(k) = \mathrm{sgn}(r(k)) = \begin{cases} 1 & if\ r(k) \geq 0 \\ 0 & if\ r(k) < 0 \end{cases} \qquad (3)$$

As can be seen from (3), the signal at the output of 1-bit ADC is a digital NRZ signal, whether the input is a PSK signal or demodulated baseband signal. Note that since the clock T_{clk} is extracted after two-narrow band filters-the Prefilter and the loop, the contribution of the wide band Gaussian noise is significantly reduced and hence can be neglected [4].

3. Experimental Results

The microphotograph of the STR circuit is shown in Figure 6. The circuit is fabricated through Honeywell SOI CMOS 0.35 μm process. The die area of the circuit is 0.7mmX2 mm. The total power dissipation is only 310 μW from a 2-V supply. For the following measured waveforms, the parameters given in Table I are used.

The waveform in Figure 7 shows how the timing circuit recovers the clock for a data sequence of 100 Kbps. As clearly seen from transition pulses in Figure 7-(2), the input signal is a random data, and the circuit is synchronized in phase within 3 or 4 bits. After synchronization, the output clock is still a proper clock despite the fact that no transition may occur sometimes during random information. As indicated previously, the circuit is capable of recovering symbol timing clock for different data rates. It can easily track a data changing from a low rate to a high rate or a high rate to a low rate. This is illustrated in Figure 8. The measured results in the Figure 8 show two different output clocks generated from a 1 MHz PSK signal in which data sequence of 100 Kbps and 10 Kbps modulated. As clearly seen, the output is a neat 100 KHz clock or 10 KHz clock.

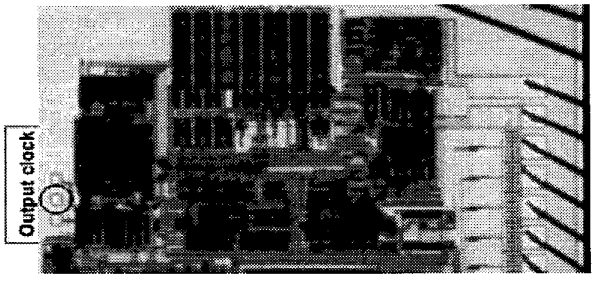

Figure 6. Microphotograph of the SOI CMOS STR circuit chip

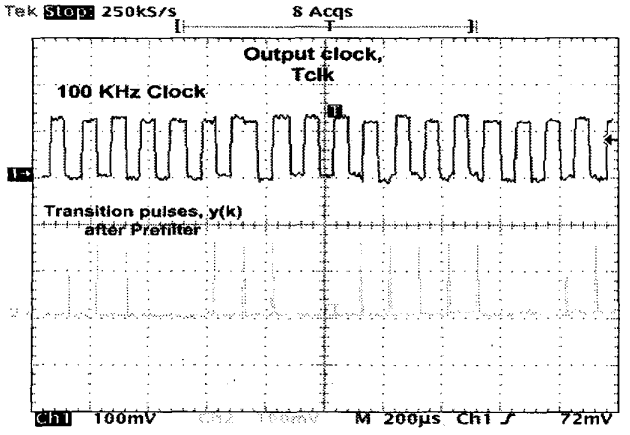

Figure 7. 100KHz clock generation from a 1 MHz PSK input signal wherein 100 Kbps data is modulated.

Figure 9 shows another output clock waveform where frequency error is added to the input signal. The input signal (Figure 11-(3)) is a 1 MHz PSK signal in which a data of 100 Kbps is modulated. It includes a frequency offset Δf=10 KHz (i.e. f_i=1MHz ± 10KHz). As seen from Figure 11-(2), the pulses smaller than $2T_s$ resulted from random frequency offsets. They will be eliminated at the output of the Prefilter. The worst-case observed timing offset for all data rates is less than 1/10 of the symbol period of the highest bit rate 100 Kbps (i.e ΔT =1 µs), which was our initial goal. The measured jitter is approximately 84 ps, as shown in Figure 10. This jitter will have no effect on the communication system since the data rates are small enough.

4. Conclusion

We have presented a new low-power all-digital symbol timing recovery circuit for PSK receivers. Although the presented circuit is designed for digital PSK receivers, it could be applied to digital FSK receivers or other modulation schemes with little modification. The significance of the STR is that it offers the design of low-cost, low timing offset, and fast synchronization. Furthermore, the design is especially suited for digital communication systems where there exists strong and fast Doppler shift.

Acknowledgment

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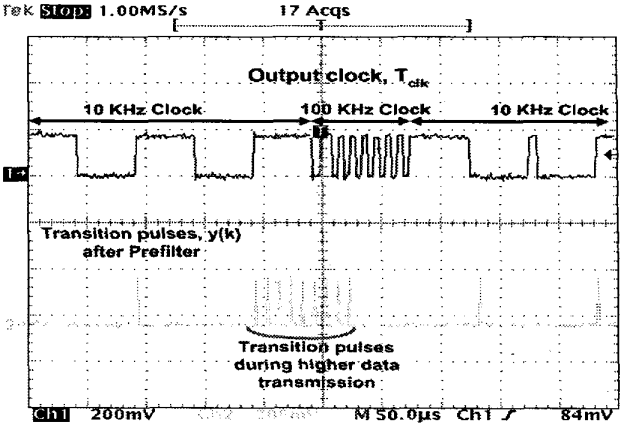

Figure 8. Output clocks when input signal includes different data rates.

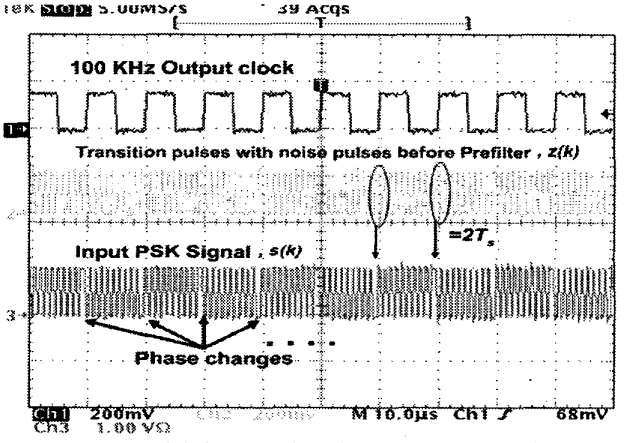

Figure 9. Recovered timing clock for a data sequence of 100 Kbps in the presence of frequency noise.

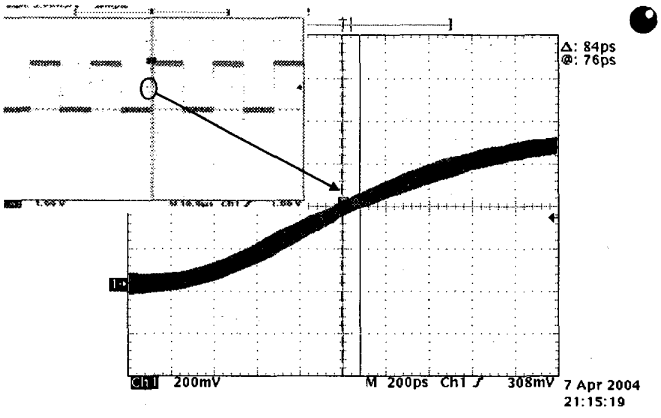

Figure 10. Jitter performance of the STR circuit