Simultaneous Switching Noise in IBIS models

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Abstract:

In this paper, a tool to convert SPICE netlists to IBIS (Input/Output Buffer Information Specification) models is presented. This tool simulates the netlist on a user-desirable SPICE engine and produces both static and dynamic characteristics of the IBIS model. A CMOS driver circuit is simulated in HSPICE and compared with an equivalent circuit created with IBIS models of the same drivers. Outputs from the drivers are compared. IBIS models are also compared against macro-models of non-linear digital drivers using spline functions with finite time difference approximation modeling techniques.

1. Introduction

Any large power/ground network will incur considerable noise related to simultaneous switching noise (SSN), also known as ground bounce, or simultaneous switching output (SSO). It occurs because of voltage glitch induced due to an inductive voltage drop when I/O drivers switch simultaneously [6]. With increasing I/O counts, accurate SSN modeling is becoming more important. To model this noise source, it is not always a good idea, or even possible, to model it using SPICE which is slow and compute intensive. For such purposes, behavioral modeling of I-O buffers using IBIS is fast becoming popular with system level designers as well as chip designers and has turned out to become a viable alternative. As a final step, the design of the system modeled with IBIS could be verified using SPICE.

In section 2, a brief introduction to IBIS is presented. IBIS is a widely used standard in the industry (EIA standard 656 -A) to model different kinds of I/O buffers. To bridge the two worlds of transistor level modeling with SPICE and behavioral modeling using IBIS, SPICE to IBIS (S2IBIS) was created. Now in its third release, S2IBIS is a tool that uses a SPICE netlist of an I/O buffer and generates its IBIS model.

An IBIS model constitutes of a set of VI tables that describe the static characteristics of the buffer and a set of VT tables that represents the dynamic information of the buffer. S2IBIS sets up SPICE simulations that derive all the static and dynamic characteristics of the model. Section 3 introduces S2IBIS. This paper also presents how the various voltage sweeps are setup as well as the other subtleties that are involved with S2IBIS.

Section 4 introduces S2IBIS3 – the latest addition to the S2IBIS tools family. One of the major issues that concerns model developers is the non-convergence of a SPICE netlist during simulations for IBIS models. S2IBIS3 resolves this issue, allowing the modeling engineer to choose the voltage range with which to sweep the device. S2IBIS3 conforms to IBIS v3.2 with backward compatibility to all the previous versions.

Simultaneous switching noise is analyzed for SPICE and IBIS modeled drivers in section 5. These IBIS models are derived using S2IBIS3. In section 6 of the paper, a new method of modeling using spline functions and finite time difference approximation is also compared with equivalent IBIS and SPICE drivers. Section 7 discusses future direction of research. Section 8 summarizes and concludes the paper.

2. IBIS

IBIS models cater to the need for fast, accurate models of Integrated Circuit drivers and receivers for board level simulations. These models are purely behavioral i.e. they contain VI, VT tables and other information such as die capacitance and packaging information which is derived from the actual simulation of the I/O pin characteristics of the chip, using tools or a measurement setup. IBIS models are thus fast, accurate and do not reveal any proprietary information contained in the IC. Figure 1 shows the block diagram of a CMOS buffer [1]

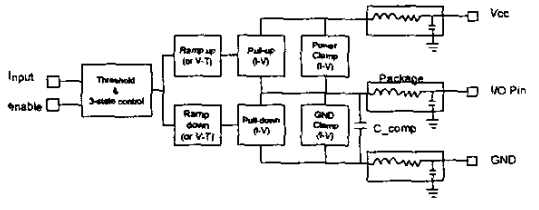

Figure 1 Block Diagram of a CMOS buffer structure in IBIS

3. S2IBIS2

An IBIS model can be generated either 1) by measurement – which requires having a well-controlled environment and measurement devices[2] or 2) by using the SPICE generated netlist and running multiple SPICE simulations to get the necessary IV and VT table data.

SPICE to IBIS is software written in C programming language that uses the SPICE netlist of a buffer and generates its IBIS model. S2IBIS2 conforms to IBIS v2.1 specifications. The user sets up a S2IBIS command file that accepts the required user inputs to generate the IBIS model of the buffer. S2IBIS supports HSPICE, PSPICE, SPICE2, SPICE3 and Spectre.

S2IBIS2 generates the required VI curves for the model. These are the pullup, pulldown, power clamp and ground clamp curves (figure 2). The pullup and pulldown curves are derived only for *output* models. The clamp curves are derived for both *output* and *input* models. It also generates the VT curves for all *output* models. These are the Rising Waveforms and the Falling Waveforms. To derive all these curves, S2IBIS2 makes SPICE runs with different settings and extracts the relevant information from the SPICE output.

For each component that needs to be evaluated, the command file has a header that provides all the default values such as the temperature range, voltage range, all the reference values and the packaging details. The command file also provides the pin list that describes which models connect to which pins and which pins serve as inputs or enables for output pins. The command file also describes each model specified in the pin list with the exception of the reserved model names POWER, GROUND and NC.

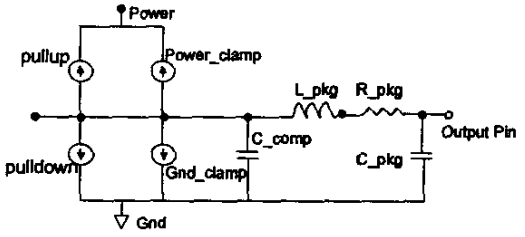

Figure 2: IBIS Output behavioral model

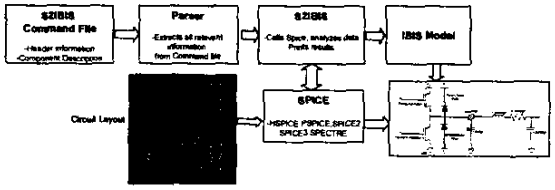

Figure 3: S2IBIS Tool Flow

Figure 3 shows a block diagram of the S2IBIS tool flow. The parser grabs all the information that has been passed by the user. The program then sets up all the file names and the SPICE files that are run once SPICE is invoked. As soon as the SPICE output files are created, they are examined for any errors or aborts. If there are no errors, the VI and VT tables are extracted from their respective files and formatted according to IBIS specification. The last step is to print the IBIS model into a file. The next section describes how the VI and VT tables are obtained using S2IBIS2.

3.1 Pullup and Pulldown curves.

Pullup and pulldown curves are derived for *output* models only. For both pullup and pulldown curves, S2IBIS2 attaches an input voltage source and an output voltage source. The input voltage is set so the output tries to drive high (for the pullup curve) or low (for the pulldown curve). The output voltage is swept from (Vgnd – Vcc) to 2* Vcc, and the output current at each output voltage is recorded. If the driver has an enable input, the sweep is performed a second time with the driver disabled. This gives the performance of the clamping structure that may be present. The two curves are then subtracted – resulting in a curve that models the performance of only the driver.

3.2 Clamp curves

Power and ground clamp curves are derived for *input* models and the *output* models with enable inputs. To find the power and ground clamp curves for input models, S2IBIS2 attaches a voltage source to the associated pin and sweeps the voltage source. The current at each voltage point is recorded. To find the clamp curves for the 'output' models with enable inputs, a voltage source is attached to the associated pin, the driver is disabled (using the voltage source attached to the enable pin), and the output voltage is swept. The resulting current at each voltage point is recorded. The sweep range for ground clamp curves is (Vgnd – Vcc) to (Vgnd + Vcc), and Vcc to 2*Vcc for power clamp curves.

3.3 Ramp rate curves

Ramp rates are derived for all *output* models. To find the ramp rates, S2IBIS2 attaches the output pin of the driver to the appropriate termination voltage through the resistor Rload, and provides the appropriate stimulus at the input. It should be noted that no packaging parasitics are involved in the simulations. The output waveform is then examined to find the 20% and 80% voltage points, and the time between them. Rload is specified in the command file. If it is not specified, it defaults to 50 Ohms.

3.4 Rising and Falling Waveform curves

Rising and Falling waveforms are produced for *output* models when they are requested with the [Rising Wavefrom] and [Falling waveform] commands. Deriving rising and falling waveforms is similar to deriving ramp rates.

4. S2IBIS3

S2IBIS2 was written in C programmable language along with Lex and Yacc (for the purpose of parsing the command file). As such, different operating systems needed different versions of the tool. Moreover, S2IBIS2 could only generate IBIS V2.1 or lower generation models only whereas IBIS itself had evolved to Version 3.2. As such, S2IBIS3 was developed. The programming language used to develop S2IBIS3 is Java which makes it platform independent. S2IBIS3 is also backward compatible to all versions of IBIS.

S2IBIS3 also implements the [series MOSFET] keyword from IBIS version 4.0. Other related keywords such as [series pin mapping] [series switch groups] are also implemented. The series MOSFET is implemented as per IBIS ver 4.0 where a change was made to accommodate PMOS and NMOS parallel MOSFET circuits.

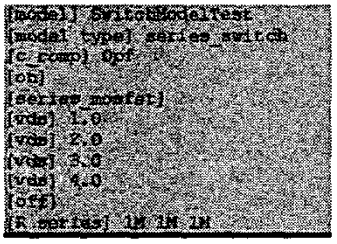

Figure 4: Snapshot of a section of the command file (.s2i) that needs to be setup to run the series mosfet keyword

A significant improvement in S2IBIS3 is an improved ability for solving convergence issues with HSPICE. Non-convergence occurs because the SPICE netlists are not accurate for the voltage range that they are swept with. If non convergence is detected, the user is asked to enter new sweep values for the beginning and the end of the sweep. SPICE is again run with the new values and if again faces non-convergence, comes back and asks for new values again. This procedure is repeated until SPICE converges or the user aborts.

5. Comparing SPICE and IBIS

To demonstrate that S2IBIS3 produces accurate models and to test how simultaneous switching noise is represented in IBIS, a test involving 4 cascaded drivers is setup. Figure 5 shows the buffer circuit.

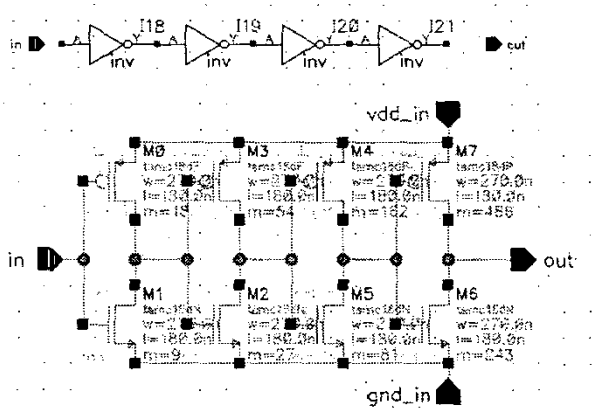

Figure 5: Cascaded - Non Inverting buffer

A circuit is setup with the 4 non-inverting drivers using the same power – ground plane through LC circuits that models the power and ground plane parasitics as well as pin parasitics. The drivers are connected to 50 ohm ideal (lossless) transmission line and terminated with 50 ohms resistors (figure 6). Simultaneous switching inputs were applied on 3 drivers and the fourth driver is connected to ground.

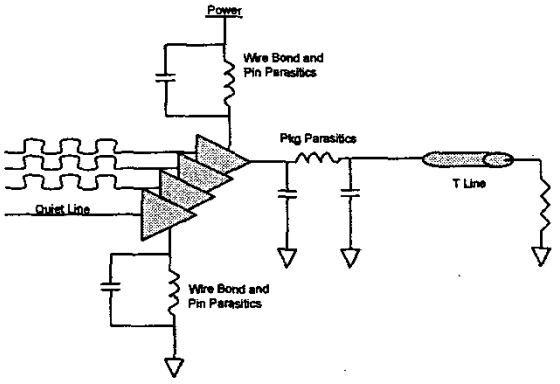

Figure 6: Test setup to compare IBIS and SPICE. 3 buffers are given simultaneously switching inputs and the 4th input is grounded.

One of the driver (all four drivers are identical) is now converted to an IBIS model using SPICE to Ibis (S2IBIS3) tool from North Carolina State University. This model is then read back in SPICE using the B element in HSPICE as shown in figure 7. As a circuit to account for parasitic RLC is connected to the power and ground source to simulate power/ground bounce and simultaneous switching noise, power sources internal to the IBIS models are not used. This is denoted by the *power = off* keyword in the B element in figure 7.

```
.subckt  buffer11 nd_pu0 nd_pd0 nd_out0 nd_in0
b0 nd_pu0 nd_pd0 nd_out0 nd_in0
+ file = 'driver_s.ibs'
+ model = 'driver'
+ typ = typ power = off
.ends
```

Figure 7: Using the B element in HSPICE to call an IBIS model

An identical circuit is recreated using the model as the driver and simultaneously switching signals are applied to 3 drivers while the fourth driver is grounded.

SPICE simulation show that while the first 3 driver show expected non-inverting output, as shown in figure 8, the fourth driver has noise (figure 9). This noise is di/dt noise that is present in the plane due to multiple drivers switching simultaneously. Due to this switching, V_{ss} rises and V_{dd} droops resulting in changed I/V characteristics. This is shown in figure 10.

In the circuit with IBIS driver, similar results are observed on the 3 drivers with signals, the quiet line does show significant noise. It should be pointed out that the representation of SSN/SSO noise is not accurate as IBIS overestimates the noise when compared to SPICE simulations. This result is not surprising as IBIS does not model the well known "feedback effect," in which the collapsing voltage rails reduce driver di/dt. The consequences of this worst case scenario representation could severely restrict a designer's options when designing with IBIS models.

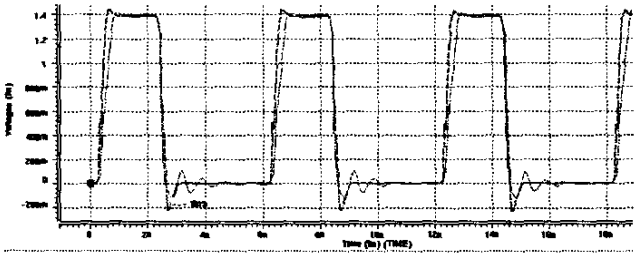

Figure 8: Output from the switching drivers. The response from IBIS modeled drivers (dashed) overshoots significantly more than the response from the SPICE transistor modeled driver (straight)

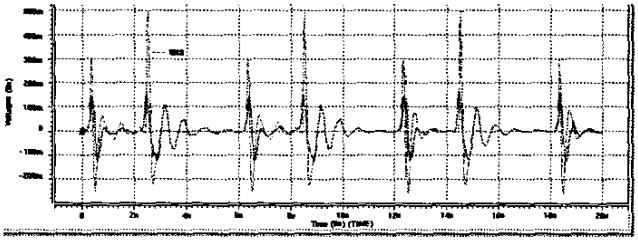

Figure 9: Noise in the quite line. The IBIS modeled driver (dashed) is shown against the SPICE transistor modeled driver (straight). The overshoot in the noise of IBIS models are significant.

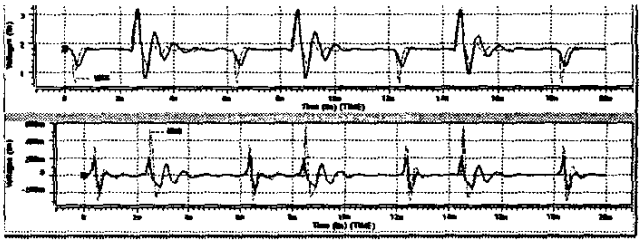

Figure 10: Power (top) and ground (bottom) signals for IBIS and SPICE.

6. Comparing SPICE, IBIS and Spline Functions with Finite Time Difference Approximations.

IBIS models were also tested against macro-models of drivers created using spline functions with finite time difference approximation. This is a black-box modeling technique that does not need information about the internal circuitry of the driver. The macro-models created using this method are known to be more accurate than IBIS and have shown excellent results for moderately complicated digital drivers [3].

A simulation to evaluate IBIS and spline models with SPICE is setup. The circuit involves single driver circuits for each method connected with lossless transmission lines. The outputs are recorded for each method. Figure 11 shows the outputs from the three methods. As can be seen, IBIS models have overshoots that are higher than the transistor model curve. Table 1 shows that the IBIS models have a higher mean square error with respect to with the values from SPICE when compared to the macro-models created using the spline functions with finite time difference approximations, though not very significant. The maximum error for the Spline macro-model is larger than the IBIS model. Note that while IBIS over-predicts SSN, the spline model under-predicts. This can be seen in figure 12 as well which shows the ground bounce for the three simulated techniques.

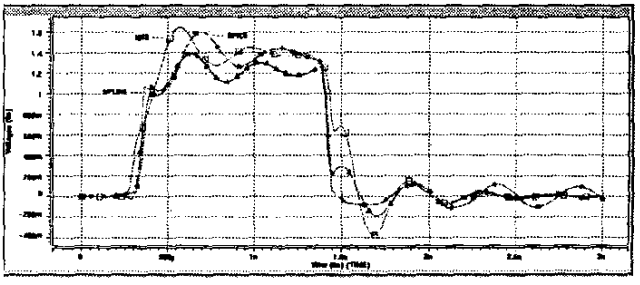

Figure 11: Comparison of SPICE (stars), IBIS (squares) and Spline (triangles) method

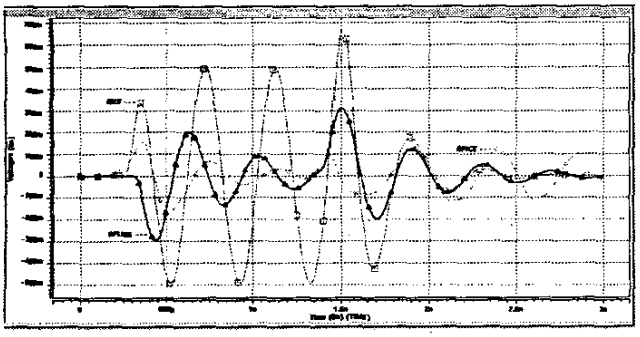

Figure 12: Noise in ground for SPICE (stars), IBIS (squares) and Spline (triangles). While IBIS overestimates the ground bounce when compared to SPICE, Spline underestimates it.

	IBIS	Spline
Mean Square Error	3.71E-02	3.65E-02
Maximum Error	6.10E-01	8.80E-01

Table 1: Mean Square error and Maximum error for IBIS models and Spline macro-model in comparison with SPICE.

7. Future Work

As shown in this paper, simultaneous switching noise is not represented accurately in IBIS models. Various solutions have been proposed to rectify this shortcoming in the IBIS model. A number of potential solutions are under investigation. One possible solution to bring better accuracy to IBIS models would be to integrate the spline function based macro-models with IBIS. As it stands at present, the modeling technique using spline functions and finite time difference approximations is not automated and quite involved whereas producing IBIS models is relatively easy and straightforward because of tools such as S2IBIS3. An integrated solution would produce the accuracy of the spline function based macro-models and the speed and automation of IBIS models. Conversely, some other proposed solutions to this issue complicate practical implementation in a simulator.

8. Conclusion

A tool to produce IBIS models from SPICE netlist is discussed. Critical issues such as non-convergence of buffers over a wide range of voltage sweep and setting up parameters to generate the static and dynamic characteristics are presented.

A test setup to access the accuracy of the IBIS models is also presented and discussed. The IBIS models are compared with transistor level models with regards to simultaneous switching noise (SSN). IBIS models need to improve in order to accurately correlate IBIS parameters with SPICE transistor models.

IBIS models are also compared against macro-models produced using spline functions and finite time difference approximations. These macro-models are more accurate than IBIS models but are slower and harder to obtain.

Acknowledgments:

The authors would like to thank Bhyrav Mutnury and Prof. Madhavan Swaminathan at Georgia Institute of Technology for providing valuable help in understanding the technique to produce macro-models using spline functions and finite time difference approximations.

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