SSN issues with IBIS models

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Abstract:

In this paper, a CMOS driver circuit is simulated in HSPICE and compared with an equivalent circuit created with IBIS (Input/Output Buffer Information Specification) models of the same drivers. The IBIS models are created using the s2ibis tool from North Carolina State University. IBIS model of the driver is also compared against model created using spline functions with finite time difference approximation modeling techniques. The three modeling techniques are analyzed for accuracy in modeling simultaneous switching noise in drivers.

1. Introduction

IBIS models have become popular with system and circuit designers as they are fast and do not disclose propriety information to the end user. As they gain in popularity, a thorough analysis is needed to figure out what IBIS is capable of and where it falls short. This paper investigates how well IBIS can model simultaneous switching noise (SSN), also known as ground bounce, or simultaneous switching output (SSO). SSN occurs because of voltage glitch induced due to an inductive voltage drop when I/O drivers switch simultaneously [1].

In section 2, a brief introduction to IBIS and North Carolina State University's S2IBIS tool is presented.

SPICE and IBIS modeled drivers are compared for simultaneous switching noise in section 3. A new method of modeling using spline functions and finite time difference approximation is also compared with equivalent IBIS and SPICE drivers in section 4. Section 5 discusses future direction of research and concludes the paper.

2. IBIS and S2IBIS

IBIS is a widely used standard in the industry (EIA standard 656 -A) to model different kinds of I/O buffers. IBIS models cater to the need for fast, accurate models of Integrated Circuit drivers and receivers for board level simulations. These models are purely behavioral i.e. they contain VI, VT tables and other information such as die capacitance and packaging information which is derived from the actual simulation of the I/O pin characteristics of the chip, using tools or a measurement setup. IBIS models are thus fast, accurate and do not reveal any proprietary information contained in the IC. To bridge the two worlds of transistor level modeling with SPICE and behavioral modeling using IBIS, SPICE to IBIS (S2IBIS) was created. Now in its third release, S2IBIS is a tool that uses a SPICE netlist of an I/O buffer and generates its IBIS model [3].

3. Comparing SPICE and IBIS

To demonstrate that S2IBIS3 produces accurate models and to test how simultaneous switching noise is represented in IBIS, a test involving 4 cascaded non-inverting drivers is setup. Figure 1 shows the buffer circuit.

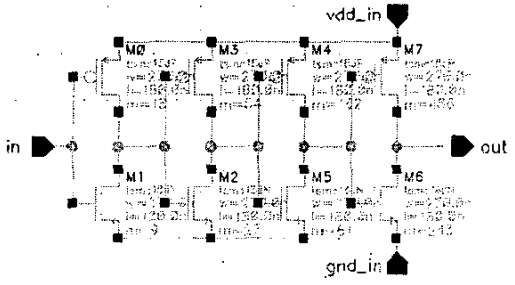


Figure 1: Cascaded - Non Inverting buffer

A circuit, as shown in figure 2, is setup with the 4 non-inverting drivers. These drivers use the same power – ground plane through LC circuits that models the power and ground plane parasitics as well as pin - package parasitics. The drivers are connected to 50 ohm ideal (lossless) transmission line and terminated with 50 ohms resistors. Simultaneous switching inputs were applied on 3 drivers and the fourth driver is connected to ground to simulate a quite line.

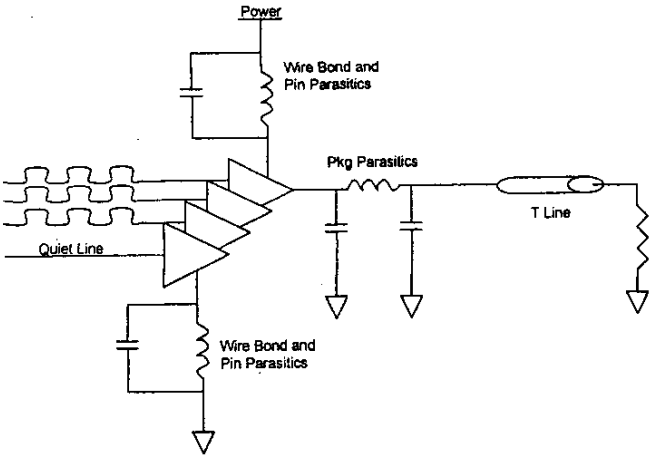


Figure 2: Test setup to compare IBIS and SPICE. 3 buffers are given simultaneously switching inputs and the 4th input is grounded.

One of the four identical drivers is now converted to an IBIS model using SPICE to IBIS (S2IBIS3). This model is then read back in SPICE using the B element in HSPICE as shown in figure 3. As a circuit to account for parasitic RLC is connected to the power and ground source to simulate power/ground bounce and simultaneous switching noise, power sources internal to the IBIS models are not used. This is denoted by the *power = off* keyword in the B element in figure 3.

HSPICE has provisions to distribute the silicon die capacitance (C_Comp) into all the nodes of the model. This is done to simulate power and ground bounce more accurately.

This feature of HSPICE is not implemented in this test as it is tool dependant and not available in all IBIS simulators.

An identical circuit is constructed using the model as the driver and simultaneously switching signals are applied to three drivers while the fourth driver is grounded.

SPICE simulation show that while the first three driver show expected non-inverting output, as shown in figure 4, the fourth driver has noise (figure 5).

This noise is di/dt noise that is present in the plane due to multiple drivers switching simultaneously. Due to this switching, V_{ss} rises and V_{dd} droops resulting in changed I/V characteristics. These observations are shown in figure 6.

In the circuit with IBIS driver, similar results are observed on the 3 drivers with signals, the quiet line does show significant noise.

```
.subckt  buffer11 nd_pu0 nd_pd0 nd_out0 nd_in0
b0 nd_pu0 nd_pd0 nd_out0 nd_in0
+ file = 'driver_s.ibs'
+ model = 'driver'
+ typ = typ power = off
.ends
```

Figure 3: Using the B element in HSPICE to call an IBIS model

It should be pointed out that the representation of SSN/SSO noise is not accurate as IBIS overestimates the noise when compared to SPICE simulations. This result is not surprising as IBIS does not model the well known "feedback effect," in which the collapsing voltage rails reduce driver di/dt. The consequences of this worst case scenario representation could severely restrict a designer's options when designing with IBIS models.

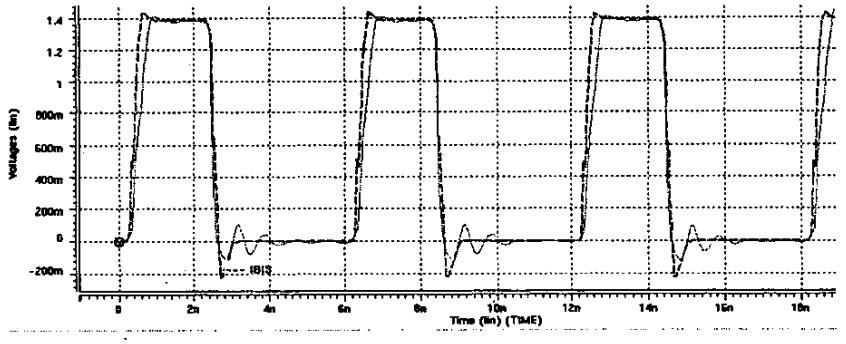


Figure 4: Output from the switiching drivers. The response from IBIS modeled drivers (dashed) overshoots significantly more than the response from the SPICE transistor modeled driver (straight)

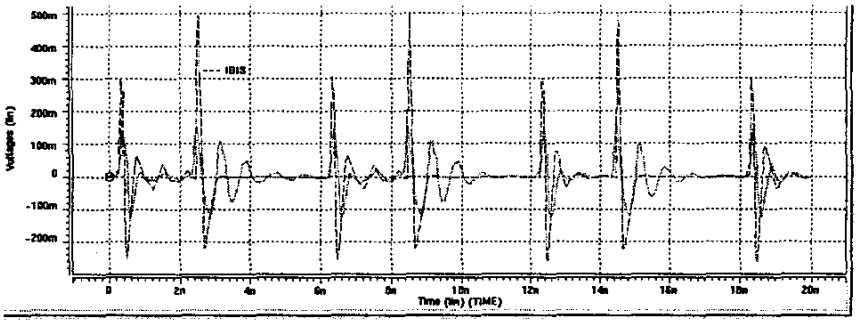


Figure 5: Noise in the quite line. The IBIS modeled driver (dashed) is shown against the SPICE transistor modeled driver (straight). The overshoot in the noise of IBIS models are significant.

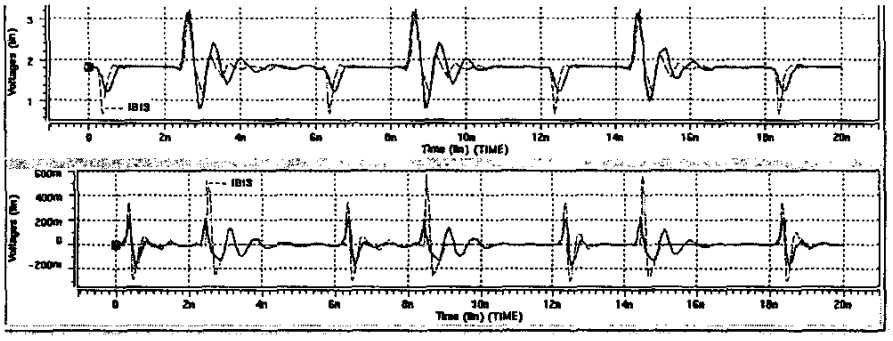


Figure 6: Power (top) and ground (bottom) signals for IBIS and SPICE.

4. Comparing SPICE, IBIS and Spline Functions with Finite Time Difference Approximations.

IBIS models were also tested against macro-models of drivers created using spline functions with finite time difference approximation. This is a black-box modeling technique that does not need information about the internal circuitry of the driver. In this modeling methodology, the static characteristics are modified to incorporate past time instances to capture the dynamic data. Static characteristics are represented using voltage controlled voltage sources whereas dynamic characteristics are represented using state equations. The macro-models created using this method are known to be more accurate than IBIS and have shown excellent results for moderately complicated digital drivers [5].

A simulation to evaluate IBIS and spline models with SPICE is setup. The circuit involves single driver circuits for each method connected with lossless transmission lines. The outputs are recorded for each method. Figure 7 shows the outputs from the three methods. As can be seen, IBIS models have overshoots that are higher than the transistor model and the spline model curve. Table 1 shows that the IBIS models have an almost 50% higher mean square error with respect to with the values from SPICE when compared to the macro-models created using the spline functions with finite time difference approximations. The maximum error for the IBIS model is also larger than the Spline macro-model. Note that while IBIS over-predicts SSN, the spline model under-predicts. This can be seen in figure 8 as well which shows the ground bounce for the three simulated techniques.

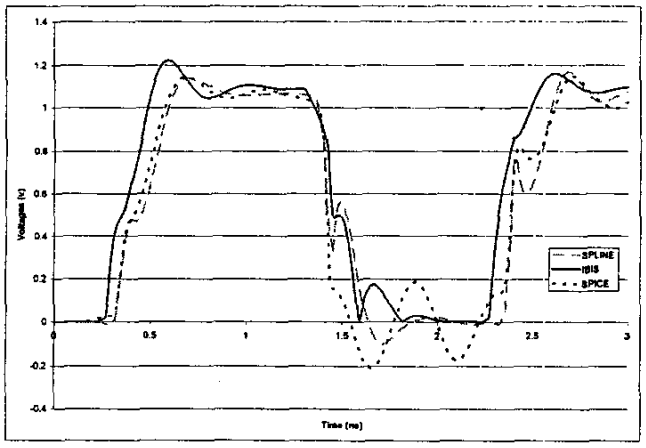
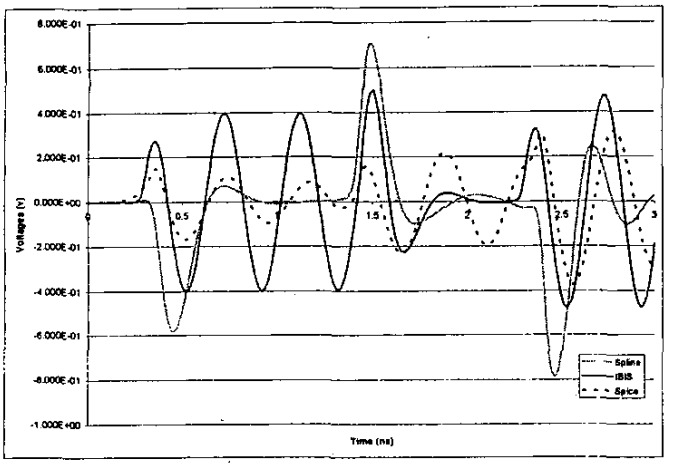


Figure 7: Comparison of SPICE (stars), IBIS (squares) and Spline (triangles) method



	IBIS	Spline
Mean Square Error	3.05E-02	1.87E-02
Maximum Error	6.08E-01	5.08E-01

Table 1: Mean Square error and Maximum error for IBIS models and Spline macro-model in comparison with SPICE.

Figure 8: Noise in ground for SPICE (stars), IBIS (squares) and Spline (triangles).
While IBIS overestimates the ground bounce when compared to SPICE, Spline underestimates it

5. Future work and conclusion.

As shown in this paper, the NCSU tool is capable of producing accurate models the IO buffers. The tool has helped in bringing to light a shortcoming in IBIS modeling methodology that will be a problem in high speed simulations where signal integrity is a priority. Various solutions have been proposed to improve simultaneous switching noise simulations using IBIS models [7]. A number of potential solutions are under investigation. One possible solution to bring better accuracy to IBIS models would be to integrate the spline function based macro-models with IBIS. The question then would be whether it is attractive to have a 50% improvement in SSN/SSO simulation accuracy and sacrifice some of the speed advantage that IBIS has over competitive modeling methodologies such as speed and simplicity and ease of creating an IBIS model.

As it stands at present, the modeling technique using spline functions and finite time difference approximations is not automated and quite involved whereas producing IBIS models is relatively easy and straightforward because of tools such as S2IBIS3. An integrated solution would produce the accuracy of the spline function based macro-models and the speed and automation of IBIS models. Conversely, some other proposed solutions to this issue complicate practical implementation in a simulator.

Acknowledgments:

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