Integrated Dynamic Body Contact for H-gate PD-SOI MOSFETs for High Performance / Low Power

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INTRODUCTION

PD-SOI circuit designers often must explicitly account for the MOSFET body voltage. Floating body effects can be undesirable, but avoiding them through the use of body contacts comes with an area penalty. A dynamic body bias scheme with body contacts and additional control circuitry requires even greater area overhead. Here, a dynamic body bias is implemented with a compact layout style to achieve improved performance and reduced power consumption.

EXPERIMENTAL

The new structure resembles a standard "H-gate" [1] PD-SOI MOSFET. The H-gate structure, illustrated in Figure 1(a), uses polysilicon gate extensions parallel to the channel for contact isolation. The body contact is created with a high-dose implant to ensure a low resistance contact to the transistor body. The H-gate structure is an "edgeless" design which is attractive for radiation-hard applications [2]. This layout style enables an independent body bias and hence independent control of V_{BS}. The body voltage can be fixed or dynamically controlled using a variety of configurations, often at the expense of increased layout area. The proposed MOSFET H-gate structure, shown in Figure 1(b), stretches the drain implant across the polysilicon extensions on both ends of the channel. This creates two parallel parasitic transistors between the drain and body of the H-gate FET, with the primary and parasitic transistors sharing a common gate. An advantage of the proposed structure is its compact layout. The parasitic transistors use the existing polysilicon extensions that isolate the body contact, and the layout adheres to design rules. By modifying the inverter design first described in [3] with the proposed transistor layout, dynamic control of the transistor body during switching with zero area overhead can be achieved. Schematics for standard and modified inverters are shown in Figure 2. When the inverter input switches from "0" to "1", the NMOS transistor turns on to pull the output from "1" to "0". The charge from the initial "high" value on the output is shifted to the NMOS body through the parasitic extension transistors. V_{BS} increases, and with positive V_{BS} the NMOS V_{TH} drops and NMOS I_{DS} increases. This improves rise/fall times and the f_{MAX} of the inverter. Simulation results for the inverter structure, shown in Figure 3, show the NMOS / PMOS body potential V_{BS} shifts 0.52V / 0.45V upon switching. The transient shift in V_{BS} reduces the gate delay 20% at 3V V_{DD} compared to the source-tied configuration. It can be seen in Figure 3 that, after switching, V_{BS} is restored to zero as V_{DS} drops.

Two test structures were designed and fabricated in Honeywell's 0.35um PD-SOI CMOS process to characterize the proposed transistor design. The first test structure, a five-stage ring oscillator, is shown in Figure 4. The oscillator frequency f_{OSC} was measured using high-impedance probes over a range of supply voltage V_{DD} for oscillators with standard inverters and modified inverters with the drain-body parasitic transistors. Electrical results are shown in Figure 5. Ring oscillators with the modified inverters displayed 20-54% higher f_{OSC} over V_{DD} ranging from 3.0V-1.0V. The second test structure, a logic chain shown in Figure 6 consisting of 37 inverters in series, was also measured over V_{DD} and the results were compared to an identical chain with standard inverters. The test input was a PRBS signal generated with an HP8133A and the chain delay was measured with high-impedance probes. A summary of the electrical results is shown in Figure 7. The total delay through the chain was reduced by 23-33% over the full range of V_{DD} with no increase in area. Alternatively, higher performance can be traded to achieve low power goals. Figures 5 and 7 demonstrate that for a given performance target, the modified transistor structure enables use of lower V_{DD}, reducing power consumption.

CONCLUSION

The H-gate structure with parasitic drain-body transistors across the polysilicon extensions offers improved performance without area penalty. For V_{DD} from 3.0V-1.0V, the ring oscillator displays an f_{OSC} increase of 20-54% while the inverter chain test structures displays a chain delay reduction of 23-33%.

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REFERENCES

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[2] Y. Li et al., IEEE Transactions on Nuclear Science, vol. 48, p. 2146, 2001.
[3] I.-Y. Chung et al., IEEE Int'l SOI Conference Proceedings, p. 20, 1996.

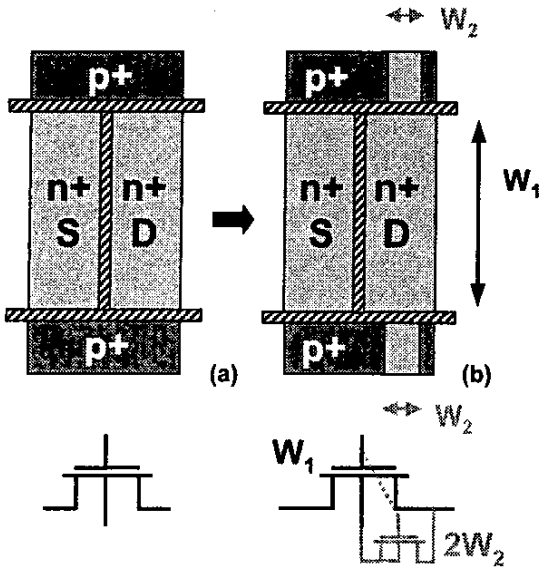

Figure 1. Layout of (a) standard nMOSFET and (b) modified nMOSFET with drain-body transistors formed stretching n+ implants across polysilicon extensions.

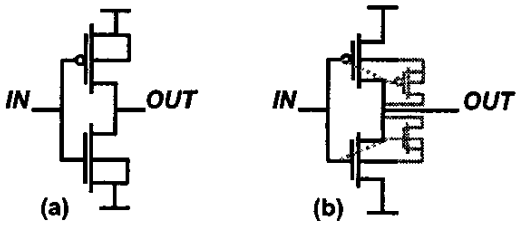

Figure 2. Schematics of (a) standard inverter with source-tied FETs and (b) modified inverter with parasitic drain-body FETs.

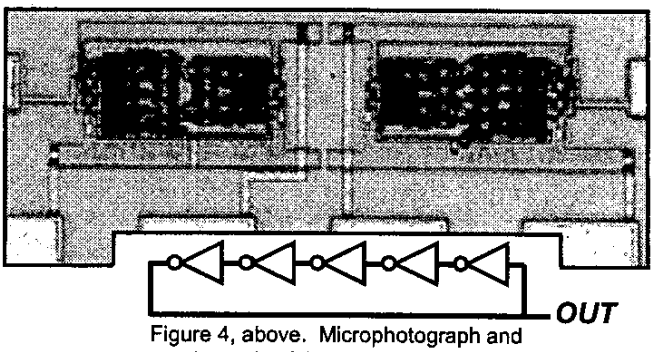

Figure 4, above. Microphotograph and schematic of 5-stage ring oscillator

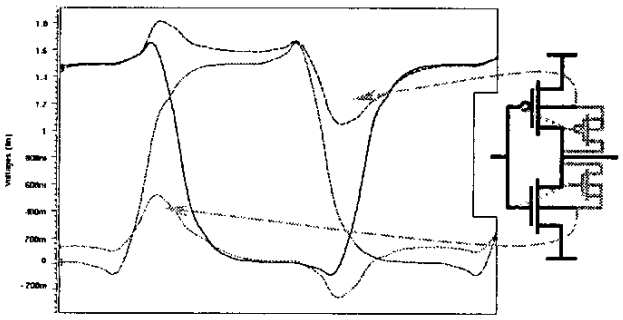

Figure 3. Simulated waveforms of modified inverter during switching with nFET and pFET body voltages indicated.

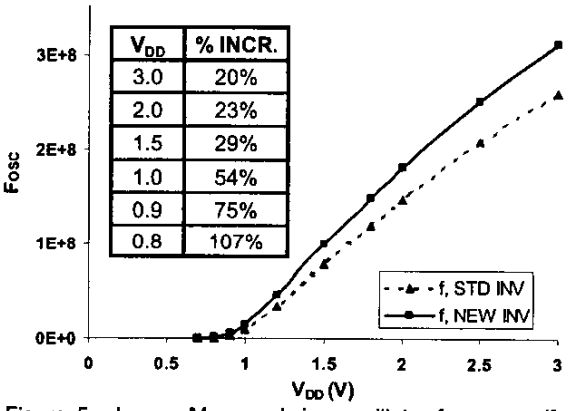

Figure 5, above. Measured ring oscillator frequency (f_{OSC}) vs. V_{DD} for baseline inverter (STD) and inverter with drain-body parasitic transistors (NEW).

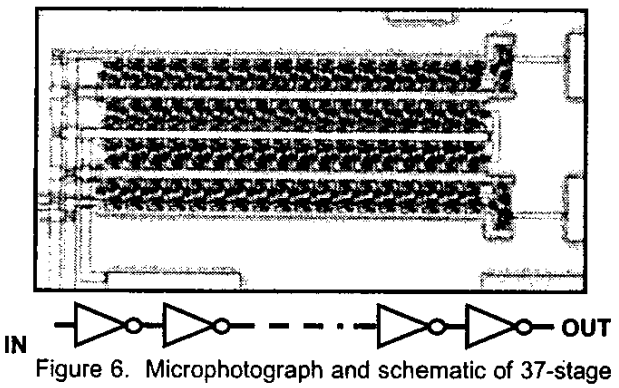

Figure 6. Microphotograph and schematic of 37-stage inverter logic chain.

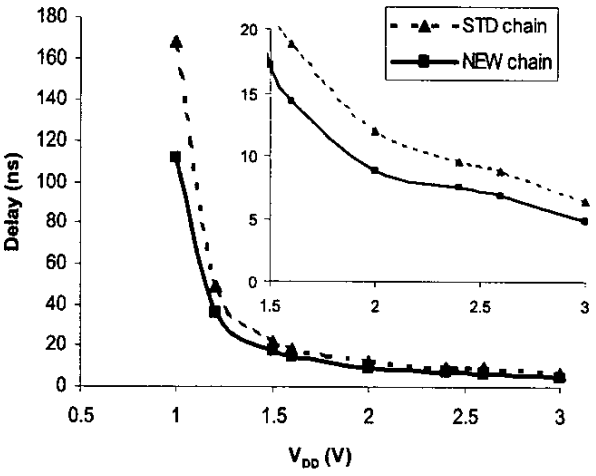

Figure 7, at right. Inverter chain delay vs. V_{DD} for baseline chain (STD) and inverter chain with drain-body parasitic transistors (NEW). Inset: Delay results at high V_{DD}.