Translating the Integration Challenges to Molecular Device Requirements - Analysis of Scaling Constraints in Molecular Random Access Memories

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ABSTRACT

Integrating molecular memory devices into large scale arrays is a key requirement for translating the miniature size of molecular devices into ultradense memory systems. This in turn imposes constraints on the individual molecular memory devices. A circuit theory approach is used to derive a general parameterized memory circuit model, from which quantitative relationships between the device on:off ratio, noise margin and memory size are studied. Assuming a small interconnect impedance and a reasonable noise margin, a 7:1 on:off ratio would be sufficient for a 4kbit memory, while a 16kbit memory would require a 13:1 ratio. Parasitic impedances become significant in architectures employing molecular interconnect, and full-scale memory circuit simulations are presented as a case study. This way, trends for the impact of all system parameters on system scalability are examined.

Keywords: molecular electronics, random access memories, scalability, device integration, molecular memory

1 MOLECULAR RAM SYSTEM

Translating the size advantage of molecular memory devices into ultradense memory systems requires large-scale integration. In this paper, we examine how the molecular device characteristics affect the scalability of these devices into large-scale random access memory arrays. A general resistive m by n crossbar is shown in Figure 1.
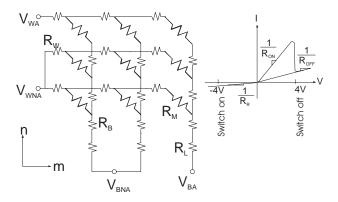

Figure 1: Molecular Random Access Memory and molecular current-voltage characteristic

The horizontal (word) lines have resistance R_W, the vertical (bit) lines have resistance R_B. These represent the interconnect resistance. A load resistor R_L is connected to the bitlines, and the resistors at the crosspoints, R_M, represent the molecular memory device. The value of R_M is either R_{ON} or R_{OFF}, depending on the state of the device. The inset current-voltage (I-V) characteristic, based on [1-3] shows the molecular memory behavior, exhibiting voltage-controlled switching between two conductivity states, with resistance R_{ON} or R_{OFF}.

The accessed memory cell is at the crosspoint of the accessed wordline, with voltage V_{WA} applied, and the accessed bitline, which is biased to V_{BA}. V_{WNA} and V_{BNA} are applied at the remaining non-accessed wordlines and bitlines, respectively.

Ignoring interconnect resistance, the voltage across the load resistor is always determined by the voltage divider formed between the load resistance and the device resistance. Thus, the difference between the voltages across the load resistor in the two states, which is the memory noise margin, is given as:

$$\Delta V = (V_{WA} - V_{BA})(\frac{R_L}{R_L + R_{ON}} - \frac{R_L}{R_L + R_{OFF}}) \qquad (1)$$

The optimal load resistance value can be obtained by setting the derivative of equation (1) equal to zero, which yields that R_L should be the geometric mean of R_{ON} and R_{OFF}.

2 DEVICE ON:OFF SCALABILITY

If negligible interconnect resistance (R_W and R_B) can be assumed, circuit transformations based on the superposition principle for linear circuits can be applied on an arbitrarily large memory array of the type shown in Figure 1. The m–1 bitlines terminating in V_{BNA} can be merged into a single bitline with all resistors divided by m–1, since they are all in parallel. The n–1 wordlines terminating in V_{WNA} can be expressed as a single wordline with all resistors divided by n–1, since they are also all in parallel. This results in the circuit template shown in Figure 2, where an arbitrarily large array can be analyzed with a circuit consisting of 6 resistors, whose values change with array size. From this template, the impact of individual parameters on scalability can be predicted qualitatively.

The assumption of negligible interconnect resistance is likely to be accurate in the case where the architecture

relies on lithographically defined metal wires, such as in [4, 5]. Even nanoscale metallic wires have impedances that should be negligible compared to the device resistance. Most metals have bulk resistivity on the order of at least $10^{-6}\Omega$m, so lithographically defined nanowires (pitch=133nm, width=40nm, height=8nm [5]) should have resistance on the order of 100-1000Ω. This is still several orders of magnitude lower than the resistance of molecular devices [1,2,6,7]. However, one cannot assume negligible resistances in architectures employing molecules as part of the interconnect structure, which will be analyzed in the latter part of this work. In either case, capacitive and inductive parasitic effects are neglected, since operating speed performance is not examined in this study.
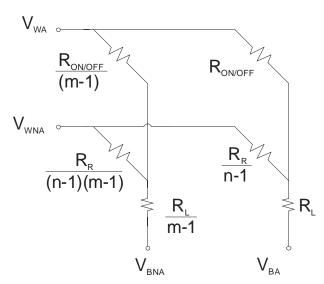

Figure 2: Circuit Template parameterized by RAM size

In order to quantitatively explore the relationship between the memory size, the noise margin and the memory device's on:off ratio, k, the memory operations were defined as given in table 1.

Parameter	Reset	Write	Read
V_{WA} (V)	6	-3	3
V_{WNA} (V)	-1	-1	-1
V_{BA} (V)	0	2	0
V_{BNA} (V)	0	0	0

Table 1: Applied voltages for memory operations

Furthermore, it was assumed that the device's reverse-bias resistance is equal to the off-state resistance, i.e. $R_R=R_{OFF}$, and that $R_L = \sqrt{R_{ON}R_{OFF}}$. Then, the noise margin can be derived by using superposition analysis on the circuit template in Figure 2. Summing up the contributions of all the voltage sources, an expression for the output voltage, V_{OUT}, across R_L can be derived.

$$V_{OUT} = \frac{R_L R_R V_{WA}}{(n-1)(R_L + \frac{R_R}{n-1})(\frac{R_L R_R}{(n-1)(R_L + \frac{R_R}{n-1})} + R_M)}$$
$$- \frac{R_L V_{BA}}{R_L + \frac{R_M R_R}{(n-1)(R_M + \frac{R_R}{n-1})}}$$
$$+ \frac{R_L R_M V_{WNA}}{(R_L + R_M)(\frac{R_L R_M}{R_L + R_M} + \frac{R_R}{n-1})} \quad (2)$$

By taking the difference between V_{OUT} for $R_M=R_{ON}$ and $R_M=R_{OFF}=k*R_{ON}$, the noise margin can be derived:

$$NM = \frac{(k-1)(n-1)(V_{WLA}-V_{WLNA})+(k^{\frac{3}{2}}-\sqrt{k})(V_{WLA}-V_{BLA})}{(k-1+\sqrt{k}+n)(\sqrt{k}+n)} \quad (3)$$

Figure 3 graphically explores the relationships between the memory size (given as the number of memory words), the noise margin (as a fraction of the applied bias between the word- and bitline during a read operation, as defined in table 1), and the ratio between the resistances of the two molecular conductivity states (on:off ratio).
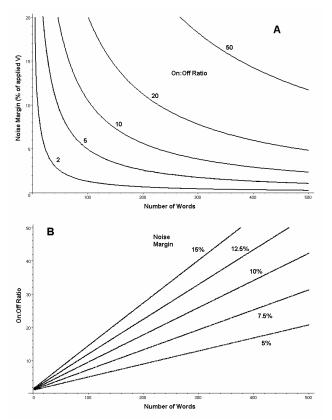

Figure 3: (a) Achievable noise margin vs. memory size for various on:off ratios (b) Required on:off ratio vs. memory size for various noise margins

For a 64x64 memory, a on:off ratio of 7:1 is sufficient for a noise margin of 10% of the applied voltage. A 13:1 ratio would allow for a 128x128 (16kbit) RAM circuit with a similar noise margin. Based on these results in conjunction with on:off ratios cited in existing literature [1-3,5,6], it is thus estimated that achieving sufficient on:off ratio of molecular memory devices will not be the most critical challenge towards building molecular memories, as other issues such as device reliability, reproducibility and architectural fault tolerance will likely impose more strict constraints on the RAM scalability.

3   INTERCONNECT SCALABILITY

In order for molecular memory to take full advantage of molecular dimensions and achieve the greatest possible integration density, a physical architecture must be developed which employs molecules not only for the memory devices, but for interconnect as well. In this scenario, molecular "wires" will likely exhibit resistances that are no longer negligible compared to the molecular memory devices [7]. The fraction of voltage dropped across the load resistor cannot exceed that of a voltage divider formed with the molecular device as well as $m*R_W$ and $n*R_B$. Thus, if R_W and/or R_B becomes significant, the noise margin diminishes quickly with increasing memory size. Full-scale simulations were performed using commercial circuit simulation software [8], since lumped models were found to have insufficient accuracy. This also prohibits using a modified version of the circuit template, since accurate results would only be obtained for a limited range of parameters. Thus, a case study was performed on a sample molecular RAM system. The system parameters, summarized in table 2, represent an attempt to start from a realistic estimate for what a fully molecular RAM architecture might look like, based on current experimental results [1,2,3,4,5].

Parameter	Value
R_{ON} (Ω)	10e6
R_{OFF} (Ω)	100e6
R_R (Ω)	1e9
R_W (Ω)	100e3
R_B (Ω)	100e3

Table 2: Default parameters chosen for case-study of fully molecular RAM

For a 16x16 RAM, the noise margin of a read operation, which is the most critical, is about 32% of the applied wordline-bitline bias of 3V. As shown in Figure 4, the noise margin decreases rather rapidly as the memory size is increased.
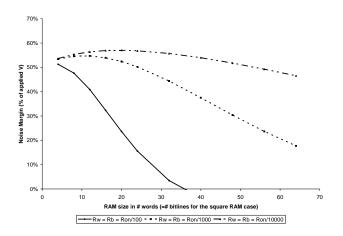

Figure 4: Scalability of fully molecular RAM for different system parameters

The solid line representing the default parameters shows that increasing the array size beyond a 32x32 causes the noise margin to become zero. The impact of the parasitic wire impedance becomes so severe that reading an "off" molecular device close to the edge of the array results in a higher voltage at the output than reading an "on" device far from the edge. Sizing the load resistor becomes nontrivial when significant parasitic degradation from the interconnect resistance is present – the geometric mean of the two molecular conductivity states in no longer the optimal value. Heuristically, an analysis similar to the case without wire resistance can be performed if only the accessed wordline and bitline is considered, which leads to:

$$R_L = \sqrt{(mR_W + nR_B + R_{ON})(mR_W + nR_B + R_{OFF})} \quad (4)$$

For a 16x16 array with the default parameters, the load resistance is 36.9MΩ. In order to avoid obtaining misleading results, R_L was fixed at this, albeit nonideal, value, so that the impact of memory scaling was measured directly rather than the secondary impact of changing the load resistance being incorporated into the results as well. As a result, the dashed lines in Figure 4, representing more ideal interconnect, show a better noise margin for a 16x16 memory than for a 2x2.

Figure 4 also shows the correlation between achievable memory size and the necessary interconnect conductivity. Reasonable noise margins are only achievable for large arrays if the interconnect is several orders of magnitude more conductive than the devices. It is important to note that for the assumed molecular characteristic, the wordline impedance plays a much more significant role than the bitline impedance. The current at each crosspoint along the wordline is divided between the input resistance looking into the memory device, and the input resistance looking into the remaining wordline. On the bitline, however, this current division occurs according to the ratio between the input resistance looking back at the wordline through the

reverse-biased device, and the input resistance of the remaining bitline. Since the reverse-biased device has a much higher resistance (R_R, which is assumed to be at least as large as R_{OFF}) than the forward biased device (which can be as low as R_{ON}), the input resistance of the wordline, and thus R_W, has to be much lower than the input resistance of the bitline, and thus R_B. This means that for scaling this type of molecular memory, with this particular I-V characteristic, to large memory arrays, it is preferable to build very asymmetrical arrays, where n>>m, and/or focus on making R_W<<R_B in the physical architecture.

For the case of square arrays with the fixed load resistance, if the number of memory elements in the array exceeds the interconnect-to-device conductivity ratio R_W/R_{ON} by more than a factor of 4, unacceptably low noise margins result.

4 CONCLUSION

The scalability of molecular electronic random access memories based on molecular memory elements relying on binary information storage as two conductivity states was analyzed. For the case of small interconnect resistance, such as would be the case in a lithographically defined crossbar, a circuit template was presented that allows accurate prediction of the scalability based on the molecular on:off ratio. It was found that molecular memory devices with a reliable and repeatable 7:1 on:off ratio can scale up to a 64x64 array in a low-parasitic physical architecture. For the case of significant interconnect resistance, such as would be present in a fully molecular memory system employing molecular "wires", the additional interconnect resistance parameters make analysis significantly more complex. For this scenario, a case study was performed for a sample molecular memory system with parameters chosen based on estimates of what might be realizable based on existing literature. It was found that interconnect impedance has a rather significant impact on system scalability. For the molecular memory device model we employed, the wordline resistance presents a much more restrictive limitation than the bitline resistance, suggesting that constructing square memory arrays is disadvantageous, and memory arrays where the total wordline resistance is much smaller than the total bitline resistance results in improved scalability.

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