AC Coupled Interconnect for Dense 3-D ICs

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Abstract—This paper presents the potential application of AC coupled interconnect (ACCI) for dense three-dimensional (3-D) integrated circuits (ICs). The concept of inductive ACCI for 3-D ICs has been proposed. Combined with the "through vias" technology, inductive ACCI can provide small pitch vertical interconnects, as well as an excellent thermal solution for dense 3-D ICs. Transformer modeling and transceiver circuit design have also been investigated. Simulations predict that, for 20 μm thinned die stacks coupled by a 100 μm diameter transformer, the transceiver circuit fed with a 5 Gbps data stream consumes 14.5 mW power.

Index Terms—AC coupled, inductive coupling, spiral inductor, three-dimensional integrated circuits (3-D ICs), through vias, vertical interconnect.

I. INTRODUCTION

AS an alternative architecture to two dimensional (2-D) planar ICs, three-dimensional (3-D) stacked ICs can alleviate interconnect related problems such as delay and power dissipation [1]. One challenge in building dense 3-D ICs is to provide a large number of vertical interconnects, which include signal paths as well as the power/ground distribution, between die stacks. Another challenge is to provide a thermal solution that can efficiently remove heat from the interior dies. Through vias and staggered (buried) vias, shown in Fig. 1, are the traditional vertical interconnects in 3-D ICs. Both, especially through vias, have good thermal conductivity. However, increasing the number of vertical vias reduces the amount of chip area that can be used for active circuitry and signal routing within each die. This limits the density of vertical vias.

AC coupled interconnect (ACCI) [2], which includes capacitive coupling and inductive coupling, can provide contact-less signal paths between neighboring dies in stacks. ACCI is an attractive alternative to vertical signal vias, in which DC components are not needed. Vertical signal transmission by capacitive coupling in 3-D ICs has been investigated previously [3]. A low power wireless super-connect interface scheme based on capacitive coupling has also been presented [4].

In this paper, an overview of ACCI and 3-D ICs is presented and the concept of inductive ACCI for dense 3-D ICs is proposed. Some details about inductive ACCI, such as the transformer modeling and transceiver circuit design, are also discussed.
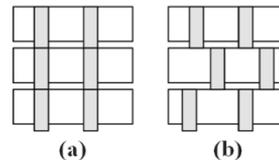
Fig. 1.   Vertical vias in 3-D ICs. (a) Through vias. (b) Staggered vias.
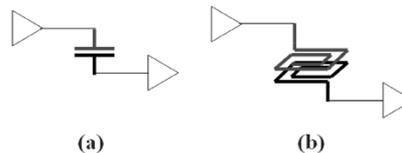
Fig. 2.   Concepts of ACCI. (a) Capacitive ACCI. (b) Inductive ACCI.

II. ACCI

A. Concepts of ACCI

For a full swing digital signal, its edges carry the digital information and its DC component carries no information. Thus the DC component is not necessary for the transmission of digital information. ACCI transmits digital information on the edges of a signal; therefore it can act as an alternative to DC interconnects. Two forms of ACCI, capacitive coupling and inductive coupling, have been investigated by researchers at NC State University [2].

The concepts of ACCI are shown in Fig. 2. In capacitive ACCI, a voltage-mode driver transmits a signal which is converted into voltage pulses after passing through the coupling capacitor. In inductive ACCI, a current-mode driver transmits a signal which is converted into current pulses after passing through the inductors pair (transformer). The voltage or current pulses are reshaped to a full swing digital signal by the receivers.

B. Benefits of ACCI

Compared with conventional DC interconnects, ACCI has advantages such as dense I/O, high speed and the potential high yield for manufacturing. From previous studies by Mick *et al.*[5], capacitive ACCI can be placed on a 100 μm pitch, which allows $\sim$8000 AC signal paths in an area of 1 cm^2. Simulation results show less than 10^{-12} bit error rate (BER) at 6 Gbps over a lossy transmission line.

ACCI technologies for both die and packaging are compatible with current manufacturing. There is no need to change the base fabrication process and materials. In contrast, it is difficult to build reliable dense DC interconnects because of mechanical compliance issues such as stress absorption.
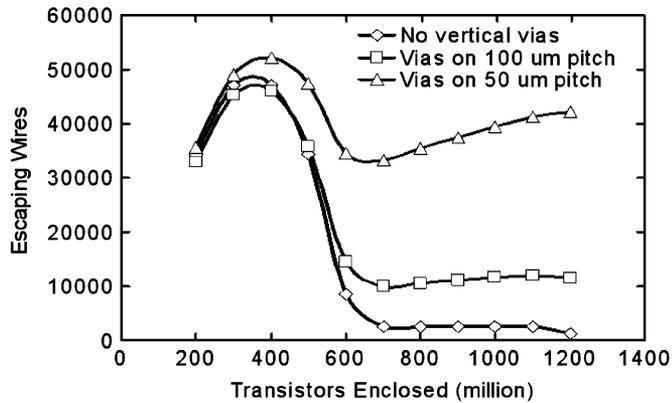
Fig. 3. Rent's Rule. Wires escaping from a box versus transistors enclosed in a box. "No vertical vias" represents the standard 2-D IC; "vias on 100 μm pitch" represents the 3-D ICs with 100 μm vertical vias pitch; "vias on 50 μm pitch" represents the 3-D ICs with 50 μm vertical vias pitch.

III. 3-D ICs

A. Benefits of 3-D ICs

For complex digital systems, the primary advantage of 3-D ICs is in improving the availability of interconnect resources within a system or sub-system. Rent's Rule [6], which can be used to predict the ratio of the count of wires escaping from a box to the number of gates (transistors) enclosed within that box, is a long standing metric for evaluating wiring resources. Within a conventional 2-D chip, this ratio is normally limited by the achievable average horizontal wiring pitch. In 3-D ICs, it is supplemented by vertical wiring, though at the cost of a compensating loss of horizontal wiring. An evaluation of this metric based on the 2005 technology node from ITRS [7] is given in Fig. 3. In this figure, escaping wires versus transistors enclosed are compared for two different 3-D ICs technologies and the standard 2-D IC technology. It can be seen that the count of escaping wires will decrease dramatically after the total number of transistors enclosed in a box exceeds 600 million. However, if there are enough available vertical vias, in the case of dense 3-D ICs, the total count of escaping wires continues to scale.

B. Potential Applications of 3-D ICs

Compared with 2-D chips, the 3-D architecture can significantly reduce interconnect delay [1]. In addition, memory bandwidth can be greatly increased in 3-D ICs. This is invaluable in many memory intensive applications such as Digital Signal Processing (DSP), networking and graphics.

Mixed signal systems can be more easily designed using 3-D architecture [1]. The key aspect is the ability of 3-D ICs to reduce noise, which is coupled from the digital portion to the RF/analog portion through the chip substrate and power/ground system. The reduction of noise is achieved by separating RF/analog portion and digital portion to different dies in 3-D ICs.

C. Barriers to Deployment in 3-D ICs

3-D ICs dramatically increase internal heat density. Thermal resistance degrades with increasing distance from the external heat sink and this may place an upper limit on the size of 3-D
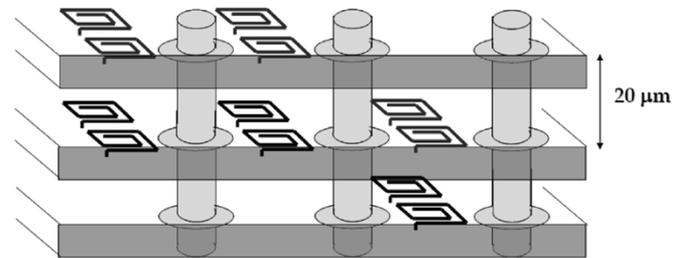
Fig. 4. Inductive ACCI interspersed with through vias. Drawing is not scaled.
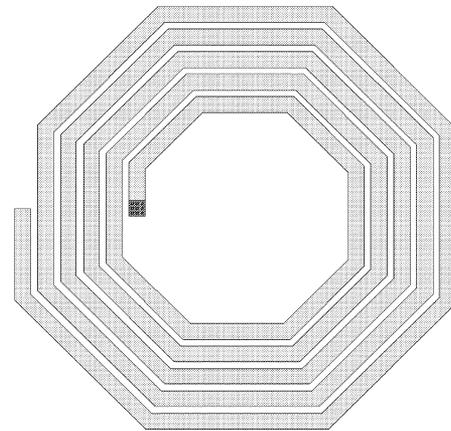
Fig. 5. Layout of a spiral inductor. 100 μm diameter, 5 turns, 2.3 nH.

ICs. In addition, 3-D ICs have the "known good die" problem which requires that presorting of dies must be done before stacking. The yield of vertical vias between die stacks is also an issue during 3-D ICs manufacturing.

IV. ACCI Potential Application to 3-D ICs

A. ACCI Alternatives

AC coupled interconnect can provide contact-less signal paths between neighboring chip stacks. This provides unique properties for their applications to 3-D ICs.

Capacitive ACCI uses a simple two-plate structure and exhibits low power dissipation. However, to achieve high density I/O the pitch of capacitive coupling plates needs to be small. Consequently, the distance, which includes dielectric material and air gap, between two plates is limited to less than 5 μm to achieve the desired coupling capacitance. Thus, the capacitive ACCI can be used for the face-to-face stacking of two dies.

For the case of inductive ACCI the distance between two inductors can be larger, e.g., 20 μm. Therefore, the 3-D stacks do not need to be face-to-face. The contact-less vertical signal paths for multidie face-to-back stacking can be achieved through inductive ACCI. Although inductive ACCI requires design that is more complex and consumes more power than capacitive ACCI, it is less sensitive to the parasitic capacitance parameters of the coupling elements.

B. Concept of Inductive ACCI 3-D ICs

3-D IC technology must focus on maximizing vertical density while not sacrificing the routing within each chip. It must also include a thermal solution that can efficiently remove heat from
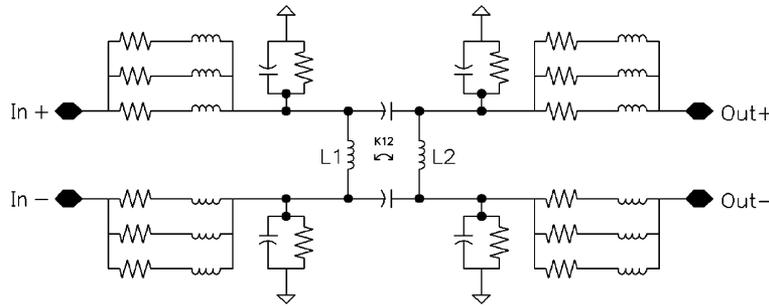
Fig. 6.   Differential transformer model.
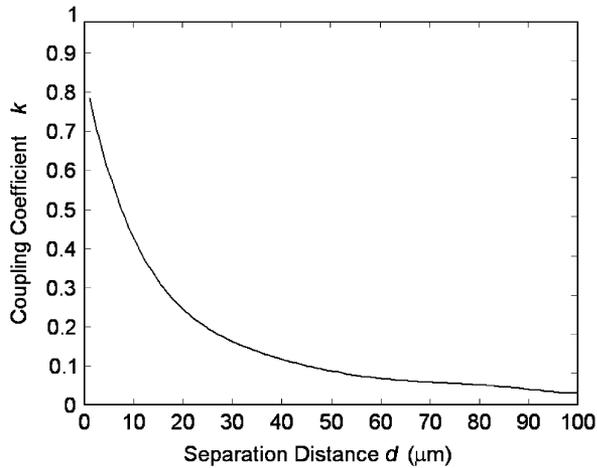
Fig. 7.   Coupling coefficient k versus separation distance d. Data based on two inductors with 100 μm diameter and 5 turns.
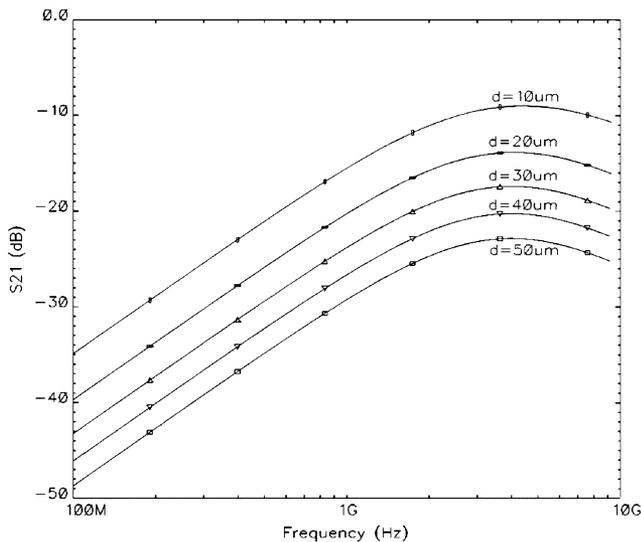
Fig. 8.   Transformer frequency response. Scattering parameter S_{21} represents the forward transmission coefficient with a 50 Ω terminated output.

Fig. 9.   Schematic of inductive ACCI transceiver system.

Fig. 10.   Schematic of inductive ACCI transmitter for 3-D ICs.

is the interdie transformer which spans two neighboring dies and communicates digital information between them. Through vias are used for power/ground distribution and heat dissipation. Since the inductors only require two metal layers per die, they disrupt intra-die routing less than buried vias do. This in turn permits more through vias to be used for power/ground distribution. A dense array of power/ground DC interconnections is essential for providing good power/ground integrity, and also provides an excellent thermal path for cooling.

C. Advantages & Disadvantages

Compared with conventional buried vias processes, inductive ACCI technology has some valuable advantages. One of the main advantages is that it can achieve high density I/O with significantly lower mechanical complexity. The inductive ACCI consumes less chip "volume" because the inductors only consume two metal layers, and does not sacrifice active layer area and multiple metal layers to interdie signal vias. However, the feasibility of using free active area beneath inductors for circuitry needs to be investigated.

the interior dies. In addition to the provision of through vias, we propose to use inductive ACCI to build 3-D stacked ICs. The combination of through vias and inductive ACCI technologies for 3-D ICs is illustrated in Fig. 4.

In this figure, the vertical pitch of dies in a 3-D IC is assumed to be 20 μm, which includes the thickness of each die and the gap or filling between two dies. A key role in inductive ACCI

Fig. 11.   Schematic of inductive ACCI receiver for 3-D ICs.
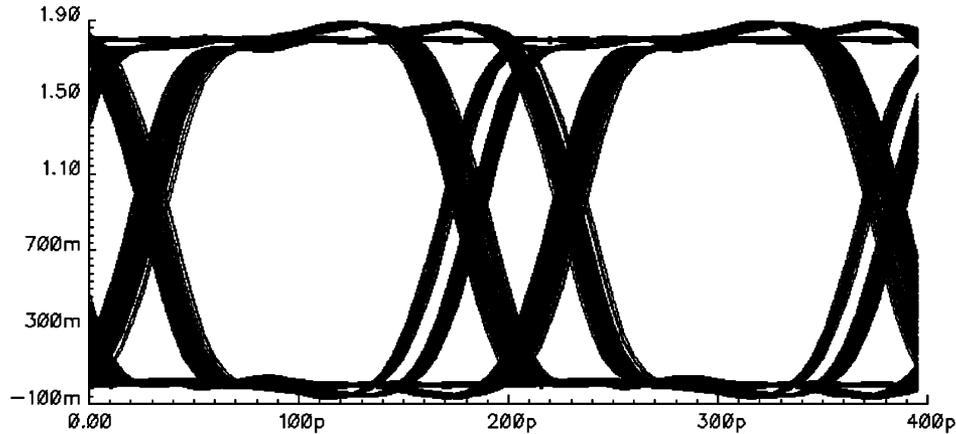
Fig. 12.   Eye diagram for output voltage of receiver.

In general, inductive ACCI has high yield and excellent reliability due to the contact-less nature of the structure. The use of inductive ACCI for signal paths and through vias for DC connections would produce high yield multidie 3-D ICs. The failure mechanisms that would impact a signal path relying on vertical vias do not affect an inductive ACCI signal path. Moreover, the DC connections, used for power/ground distribution, would be designed redundantly to tolerate the expected loss during manufacturing and any anticipated long-term via failure.

The main disadvantage of inductive ACCI 3-D ICs is that the transceiver circuit has higher power consumption compared with the simple buffer pair in pure vertical vias 3-D ICs. In addition, the interference between two neighboring inductors and the effects of inductors on the function of neighboring circuits are issues to be studied.

D. Transformer Construction and Modeling

A transformer can be created by stacking two spiral inductors together. Fig. 5 shows the layout of a spiral inductor on a CMOS test chip. It has 100 μm diameter with 5 turns, and its estimated inductance is 2.3 nH.

A differential transformer model was created and shown in Fig. 6. This model was based on measurements of on-chip transformers and simulations using field solvers to determine the decrease in coupling for the larger separations that will occur in inductive ACCI 3-D ICs. L_1 and L_2 represent the coupled inductors; k_{12} represents the coupling coefficient between L_1 and L_2. The two capacitors connecting L_1 and L_2 represent the parasitic interwinding capacitance between them and capture common mode coupling. The shunt capacitors and resistors represent the parasitics of spiral inductor to the substrate. The series inductors and resistors in parallel segments model the skin effect in the windings of the spiral inductor.

The coupling coefficient k between two spiral inductors strongly depends on the separation distance d between them. The dependence of k on d was extracted using a CAD tool ASITIC [8] and plotted in Fig. 7. From this plot, for two 2.3 nH inductors with 20 μm separation distance, the coupling coefficient is 0.25.

The frequency response for a 100 μm diameter transformer with separation varying from 10 to 50 μm is shown in Fig. 8. This plot shows that the transformer reaches its peak perfor-

mance at 4 GHz, indicating 8 Gbps digital data rate. With a smaller separation, or a thinner die in 3-D stacks, improved inductive coupling can be achieved.

E. Transceiver Circuit for Inductive ACCI 3-D ICs

The schematic for an inductive ACCI transceiver system designed for 3-D ICs is shown in Fig. 9. The transmitter (TX) and the receiver (RX) are on two stacked dies. Two coupled inductors overlap in the horizontal direction but are separated in the vertical direction. To transfer signals using inductive coupling, a current mode transceiver is desired. To improve common mode noise rejection, fully differential signaling is needed.

Shown in Fig. 10 is the schematic for a transmitter circuit. The H-bridge, which includes transistors $MP1 \sim 2$ and $MN1 \sim 2$, is a current steering structure. From a single-end input signal the complementary signal is produced, and both signals are used to control the switching of H-bridge and result in a strong differential current swing (~ 7.0 mA peak to peak). Transistors $MP3 \sim 4$ and $MN3 \sim 4$ are diode-connected and tune the output impedance of transmitter. The inductor pair (transformer), shown in Fig. 9, captures the edges of the current swing and converts them into current pulses.

The receiver circuit, shown in Fig. 11, can be divided into two stages. The first stage of the receiver, which includes transistors $MP1 \sim 4$ and $MN0 \sim 4$, senses differential current pulses and converts them into single-end voltage pulses. In this stage the four diode-connected transistors $MN1 \sim 2$ and $MP1 \sim 2$ form a structure with low input impedance, and are used to detect and convert differential current pulses ($\sim 180 \mu A$ peak to peak) into differential voltage pulses (~ 60 mV peak to peak). They are followed by a self-biased differential amplifier which converts differential voltage pulses into single-end voltage pulses (~ 225 mV peak to peak).

The second stage of the receiver, which includes inverters $INV1 \sim 5$ and transistors MP5/MN5, amplifies the voltage pulses and converts them into full swing digital signals. In this stage the transmission-gate feedback, MP5/MN5, clamps INV1 and INV2 to operate at the point of half supply voltage and maintains high bandwidth to keep sharp pulses, which help reject intersymbol interference (ISI). INV3 and INV4 form a latch that is used to convert the pulse signals to full swing logic signals. INV5 is an output buffer.

F. Simulation Results

In Hspice simulations, the following parameters, $L = 2.3$ nH, $d = 20 \mu$m, $k = 0.25$ were assumed. Based on 0.18-μm CMOS technology, and simulated using a 20 000 bit pseudo random data stream at 5 Gbps and supplied by a 1.8 V voltage source, an eye-diagram for the output voltage of receiver, shown in Fig. 12, was obtained. The jitter of the output signal is about 70 ps, which is acceptable when compared with its 200 ps data period.

The total power dissipation of one TX/RX pair is 14.5 mW, in which the transmitter consumes 7.1 mW and the receiver consumes 7.4 mW.

V. CONCLUSION

Capacitive ACCI can be used for two-die 3-D ICs with face-to-face stacking. Inductive ACCI is more suitable for multiple-die 3-D ICs with face-to-back stacking because of its higher tolerance to the separation distance between coupling elements. Combined with through vias technology, inductive ACCI can achieve dense pitch as well as excellent thermal performance for 3-D ICs.

For 20 μm thinned die stacks coupled by a 100 μm diameter transformer, simulations predict that the transceiver circuit fed with a 5 Gbps input stream consumes 14.5 mW power and maintains 70 ps of jitter at the output.

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