CAD Flows for Chip-Package CoDesign

Ambrish Varma, Alan Glaser, Paul Franzon
{akvarma,paulf}@unity.ncsu.edu, awg@adc.idt.com
ECE Department, North Carolina State University
Box 7911, Raleigh NC 27695
Ph - 919 515 7351, fax – 919 515 2285

Abstract

A unified method is presented for layout and package design implemented within a commercial design environment that will reduce design time and enable chip-package codesign.

1. INTRODUCTION

Today CAD flows for Integrated Circuit design are very separated from CAD flows for package design. The tools behave differently, are often provided by different vendors, and are typically based on different user interface paradigms. This leads to a number of problems and difficulties in the design of complex systems, especially with today's high performance designs and tight design cycles. First, it leaves open the scope for simple errors to propagate through to the first design iteration. For example, pin mis-naming, subtle package and board mounting errors, etc. Today there is no established approach for consistency checking across the system or module. Second, timing closure becomes much more difficult. With tight timing margins, the on-chip delay is as important as the package and board induced delays. A prioiri budgets do not make it easy to identify and exploit intelligent tradeoffs. In addition, such budgets do not guarantee complete signal integrity of a net that spans two chips, two packages, one board, etc. Third, lack of coordination prevents many optimizations to be discovered. A prime example would be the case where pin location re-assignment improves routability at the package and board level, possibly to the extent of saving layers. Finally, with growing interest in System On a Package (SOP), the package will be an integrated part of the design, rather than an afterthought. Examples include RF systems with on-package passives [9,10], as well as the concept of using the package routing resources as an extension of on-chip resources. The latter, as explored in the SHOCC project (e.g. [8]) was an important motivator for the work reported here. Chip-package codesign is identified as a critical issue in the ITRS.

The thesis behind the work reported here is that Integrated Circuit tools are sufficiently capable and flexible to solve this problem. The tools are capable of capturing the package design as well as the IC design, and to permit verification within one environment. This paper illustrates this is feasible within the context of one commercial tool set. It explains how the tool set was modified to permit capture of the physical and connectivity design of the package, to carry out Layout Versus Schematic (LVS) verification of the complete system, and to allow automatic extraction and simulation.

This paper illustrates the feasibility and practicality of this paradigm using the Cadence commercial IC design package. It builds upon previous work of delivering CAD flows using this tool set [1] and previous work in chip package codesign [2,3,4]. In fact it was the difficulties experienced in verifying the IC/MCM combination described in [2,3] that motivated the work reported here. Though it illustrates this process using flip-chip MultiChip Module (MCM) packaging, it can be easily extended to other package types. An example of an extension to simple wire-bond frame package is given at the end of the paper. All the files described in this paper are available for download [4].

Note, that the authors are not proposing that package and board designers replace their current tools with IC tools. There are a number of practical reasons not to do this. Instead, it is suggested that it is relatively simple to import a partial, or complete, package and board design into the IC environment so that design tradeoffs can be easily explored and final verification performed.

This paper is structured as follows. Section II discusses the technology file that forms the core of the tool flow. Section III presents the DIVA rule deck. These are three rule files that have been created to permit designs that can be fabricated. These rules are Design Rule

0-7803-8128-9/03/$17.00 © 2003 IEEE

Checking (DRC), Extraction rules and Layout versus Schematic (LVS) rules. Section IV discusses a case study that was used to demonstrate the toolset that was developed. The work is summarized in section V followed by the conclusion in section VI.

II. TECHNOLOGY FILE

By necessity, IC CAD systems are very flexible as they have to be applicable to a wide variety of IC processes, ranging from simple 8 mask ones to processes requiring 20 masks or more. This flexibility is created by providing the provision to describe all the relevant data for the IC process, in a set of "Technology Files". No presumption of the details of the fabrication process are buried in the tools and their algorithms. The technology file defines the materials and rules we can use in the IC fabrication process. It contains the following:

Layer Definitions, Device Definitions, Layer, physical and electric rules and Rules specific to individual tools and applications.

The flow described here uses these highly flexible technology files to capture package information. Essentially, the package layers are treated simply as additional IC mask layers. The MCM metal, via and pad layers were captured in a technology file that specifies the layer descriptions, their adjacencies and what each via layer connects. The file also specifies minimum dimensions, grid size, etc., as well as how the layers are to be described on the screen.

III. DIVA DECK

This section deals with the Interactive Verification inside Design Automation (DIVA) rule decks. Three rule files are necessary, one each for Design Rule Checking (DRC), Extraction and Layout verses Schematic (LVS).

A. Design Rule Checking.

This rule file will permit design rule checking of the substrate and solder bumps against a geometric set of manufacturing design rules. Design rules exist so that a part can be reliably fabricated without any flaw. A designer would run the Cadence Diva package to perform these checks.

DRC files can be written incrementally. That is a DRC file could only check design rules for certain layers and/or certain rules only. Hence one DRC file could be used for on chip design and another could be used for on substrate (i.e. off chip) design.

The Design Rule Check deck checks for rules such as separation between same metal layer, separation between different metal layers, metal-via enclosures, minimum width of a layer etc.

B. Extraction

An extraction rule file allows the generation of a simulator-ready netlist from a layout. It detects devices such as transistors, capacitors, solder bumps etc from the layout and connects them so that a meaningful circuit can be interpreted from the layout. In this case study, we extract long off chip interconnects as transmission lines, and on-chip interconnect as RC lines. Signal from the on-chip interconnect is passed on to the substrate through a solder pad. These solder pads are distributed uniformly throughout the chip surface. The pad layer in case study is represented by a layer named mcm4. Whenever a metal layer and mcm4 overlap, a solder bump is placed in the extracted view. On the substrate, we have 2 metal layers to propagate the signal - X route (mcm2) and Y route (mcm3). The two layers are modeled as U elements (lossy transmission lines). To place the desired components (solder bumps and transmission lines) in the extracted view, the divaEXT.rul file was written.

C. Layout Vs Schematic

The Layout versus Schematic (LVS) Deck compares two versions of a circuit and isolates any differences. It can be used to compare two layouts, two schematics, or a layout and a schematic [7]. For our purpose, we use LVS to compare the extracted version of the layout and the schematic as drawn by the designer or as provided by a customer or a third party.

Such automation is particularly valuable in this application, as simple miscommunications between package and chip designers could lead to disastrous connectivity mistakes. LVS compares the netlist from the extracted view of the layout with the netlist from the schematic that has been drawn that represents the layout. The divaLVS rule file is incorporated with the existing tech files and the diva deck so that simultaneous design and verification can be performed.

IV. CASE STUDY – DRIVER RECEIVER CIRCUIT

To demonstrate that the tool-set designed for this study works satisfactorily, a driver and a receiver circuit were connected via off chip MCM layers. Signal from the driver was brought onto the substrate. The signal was propagated using the X and Y layers and was brought back on the chip to be connected to the inverter. This circuit was checked for design rule errors, extracted and then the extracted netlist matched against the schematic netlist thus checking for any Layout Versus Schematic errors.

The technology file written for the co-design and analysis of chips and substrate employing the SHOCC paradigm has a total of five additional layers and four via layers that serve as connection between these layers. New layers that are added to permit co-layout of chips are given in table 1:

Layer	Description
mcm0	Ground plane (A shape on mcm0 signifies a hole on the layer)
mcm1	Power plane (A shape on mcm0 signifies a hole on the layer)
mcm2	X Metal on the Substrate
mvmV1	Via Between mcm2 and mcm0
mcmV2	Via Between mcm2 and mcm1
mcm3	Y Metal on the Substrate
mcmV3	Via Between mcm2 and mcm3
mcm4	Top pad metal
mcmV4	Via Between mcm3 and mcm4

Table 1. New layers added for package codesign.

Layout of the test circuit was done by creating an instance of the driver and an instance of the receiver (which is a simple inverter). The output of the driver is connected to the input of the receiver via the substrate layers. Metal 3 at the output of the driver is laid out in such a way such that it overlaps mcm4 layer (a SHOCC top pad layer). From there, the signal is passed through to mcm3 (which is the Y Plane on the substrate) via the contact, mcmV4. The signal is then passed on to mcm2 (which is the X Plane on the substrate) via the contact layer mcmV3. The signal is then brought back to mcm3 from where it is connected to mcm4 and back to metal 3 to the input of the inverter. Once the circuit has been laid out using Cadence, we checked the validity of the design by running DRC. The rules for DRC that have been implemented in this project are from MicroModule Systems MCM-D Technology Kit [6]. The kit is provided to support the multi-chip module (MCM) designer to accurately develop an MCM design.

For extracting the substrate layers and the solder bumps, HSPICE models were created for the X and Y metal layers modeled as U element transmission lines. The bumps were replaced by a RLC sub-circuit. The extracted circuit is shown in fig. 1. Once we have extracted the Driver – Inverter circuit, we can obtain the HSPICE netlist of the extracted view using Analog Circuit Design Environment and choosing HSPICE as the simulator. Layout Versus Schematic program compares the obtained netlist from the extracted view of the layout with the netlist from the schematic that has been drawn that represents the layout (which can be drawn by the designer or can be provided).

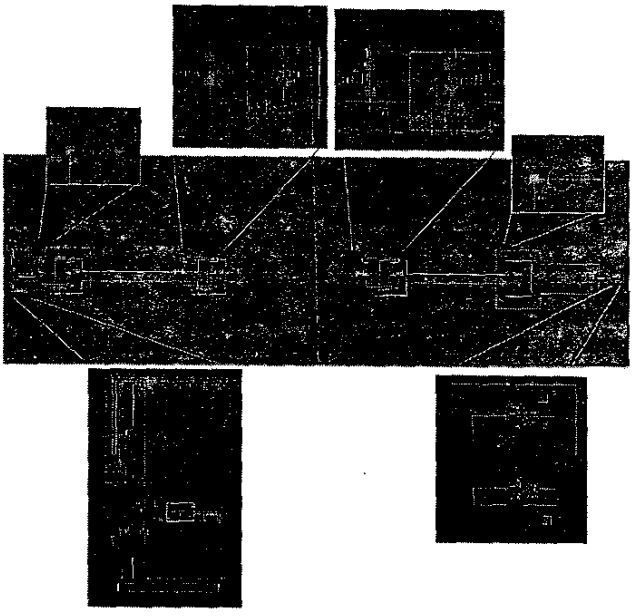

Figure 0. Extracted Driver-Receiver Circuit

V. DISCUSSION

This paper demonstrates the feasibility of using IC tools for codesign of chips and packages. The results of running these tools can be used for the tasks like the following:

- Checking for design rule violations at the physical chip-package interface.
- Optimizing a net or set of nets, spanning both chip and substrate, so as to meet timing or maximize performance.
- Checking for correct connectivity for nets spanning the chip and package together, as well ensuring the design is consistent with the circuit model presumed.

The decks written to perform these tasks were close to 1300 lines long. No modifications were made to the execution code of the tool, nor any external new tools added. It would be possible to extend this work to perform other tasks benefiting from automation. For example, chip-package nets could be sorted by criticality, filters could be written to enable selective or incremental extraction, etc. In mixed signal designs, on-package passives could be extracted and modeled together with the IC. None of these would require changes to the CAD tool codes, just to the associated decks.

VI. CONCLUSION

This paper demonstrates that IC design tools can be readily extended to enable the co-design and verification of high performance chip-package systems. The IC tool extensions do not require modification of the code but of the rule decks that direct the tools. This co-design environment permits optimization of nets spanning both chips and packages, as well as verification of system-wide connectivity.

Acknowledgements

This work was supported by the Semiconductor Research Corporation and by DARPA, via the SHOCC consortium. It was also supported in part by the National Science Foundation.

References

[1] Franzon, P.D.; Wentai Lui; Gloster, C.; Schaffer, T.; Glaser, A.; Stanaski, Infrastructure and course progression for complex IC design education, A. Microelectronic Systems Education, 1999. MSE'99. IEEE International Conference on , 1999 Page(s): 88 – 89.

[2] T. Schaffer A. Stanaski A. Glaser, P. Franzon, "The NCSU Design Kit for IC Fabrication through MOSIS," available at http://www.ece.ncsu.edu/cadence/CUG1998/index.html

[3] Schaffer, T.; Glaser, A.; Rao, S.; Franzon, P., "A flip-chip implementation of the Data Encryption Standard (DES)," IEEE Multi-Chip Module Conference, 1997. MCMC '97., 1997 IEEE , 1997 Page(s): 13 –17.

[4] http://www.cadence.ncsu.edu/SHOCC_Kit/SHOCC_home.html

[5] Franzon, P.D.; Stanaski, A.; Tekmen, Y.; Banerjia, S., "System Design Optimization for MCM-D/Flip-Chip," Components, Packaging, and Manufacturing Technology, Part B: Advanced Packaging, IEEE Transactions on, Volume: 18 Issue: 4 , Nov. 1995, 620 –627.

[6] MCM-D Technology Kit – MicroModule Systems and Mentor Graphics Rev 1.01 1 –Sep 1994.

[7] Cadence Openbook – online documentation for cadence specific topics.

[8] Afonso, S.; Schaper, L.W.; Parkerson, J.P.; Brown, W.D.; Ang, S.; Naseem, H.A. "Modeling and electrical analysis of seamless high off-chip connectivity (SHOCC) interconnects." Advanced Packaging, IEEE Transactions on [see also Components, Packaging and Manufacturing Technology, Part B: Advanced Packaging, IEEE Transactions on] , Volume: 22 Issue: 3 , Aug. 1999; 309 –320.

[9] Pence, W.E; "Packaging for wireless communications". Electrical Performance of Electronic packaging, 1994., IEEE 3rd Topical Meeting on , 1994 Page(s): 157 –158.

[10] Laskar, J.; Jokerst, N.; Brooke, M.; Harris, M.; Chun, C.; Pham, A.; Liang, H.; Staiculescu, D.; Sutono, S. "Review of RF packaging research at Georgia Tech's PRC". Advanced Packaging Materials, 1998. Proceedings. 1998 4th International Symposium on , 1998
Page(s): 139 –150.