The development of a Macro-modeling tool to develop IBIS models

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Abstract:

A tool to convert SPICE netlists to IBIS (Input/Output Buffer Information Specification) models is presented. This tool simulates the netlist on a user-desirable spice engine and produces both static and dynamic characteristics of the IBIS model.

1. Introduction

Behavioral modeling of I-O buffers is fast becoming popular with system level designers as well as chip designers. IBIS(Input/Output Buffer Information Specification) is a widely used standard in the industry (EIA standard 656 -A) to model different kinds of I/O buffers. At the same time, the popularity of SPICE and SPICE like simulators to simulate digital circuitry is time tested and widespread. To bridge the two worlds of system level design and simulation and circuit level design and simulation, SPICE to IBIS (S2IBIS) is presented in this paper. Now in its third release, S2IBIS is a tool that uses a SPICE netlist of an I/O buffer and generates its IBIS model.

An IBIS model constitutes of a set of VI tables that describe the static characteristics of the buffer and a set of VT tables that represents the dynamic information of the buffer. S2IBIS sets up SPICE simulations that derive all the static and dynamic characteristics of the model. This paper presents how the various voltage sweeps are setup as well as the other subtleties that are involved with S2IBIS.

This paper also presents S2IBIS3 – the latest addition to the S2IBIS tools family. One of the major issues that concerns model developers is the non-convergence of a spice netlist during simulations for IBIS models. S2IBIS3 resolves this issue, allowing the modeling engineer to choose the voltage range with which to sweep the device. S2IBIS3 conforms to IBIS v3.2 with backward compatibility to all the previous versions.

An IBIS model of a simple four stage non-inverting buffer is derived using S2IBIS3 and presented in this paper as well.

2. IBIS

IBIS models cater to the need for fast, accurate models of Integrated Circuit drivers and receivers for board level simulations. These models are purely behavioral i.e. they contain VI, VT tables and other information such as die capacitance and packaging information which is derived from the actual simulation of the I/O pin characteristics of the chip, using tools or a measurement setup. IBIS models are thus fast, accurate and do not reveal any proprietary information contained in the IC. Figure 1 shows the block diagram of a CMOS buffer [1]

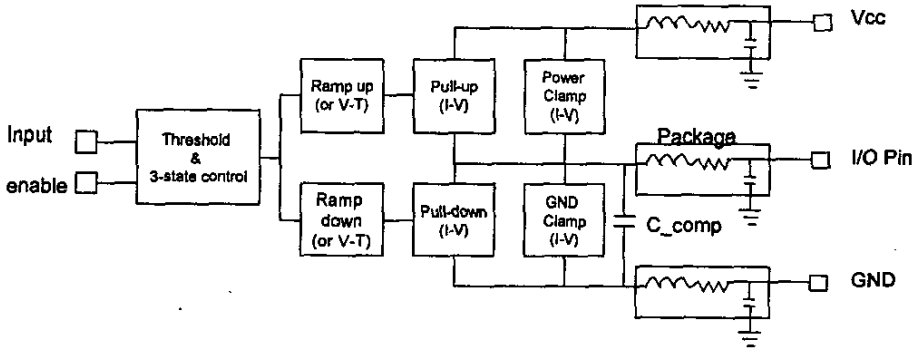


Figure 1 Block Diagram of a CMOS buffer structure in IBIS

3. S2IBIS2

An IBIS model can be generated either 1) by measurement – which requires having a well-controlled environment and measurement devices[2] or 2) by using the SPICE generated netlist running multiple SPICE simulations to get the necessary IV and VT table data.

SPICE to IBIS is software written in C programming language that uses the SPICE netlist of a buffer and generates its IBIS model. S2IBIS2 conforms to IBIS v2.1 specifications. The user sets up a S2IBIS command file that accepts the required user inputs to generate the IBIS model of the buffer. S2IBIS supports HSpice, PSpice, Spice2, Spice3 and Spectre.

S2IBIS2 generates the required VI curves for the model. These are the pullup, pulldown, power clamp and ground clamp curves (figure 2). The pullup and pulldown curves are derived only for *output* models. The clamp curves are derived for both *output* and *input* models. It also generates the VT curves for all *output* models. These are the Rising Waveforms and the Falling Waveforms. To derive all these curves, S2IBIS2 makes SPICE runs with different settings and extracts the relevant information from the SPICE output.

For each component that needs to be evaluated, the command file has a header that provides all the default values such as the temperature range, voltage range, all the reference values and the packaging details. The command file also provides the pin list that describes which models connect to which pins and which pins serve as inputs or enables for output pins. The command file also describes each model specified in the pin list with the exception of the reserved model names POWER, GROUND and NC.

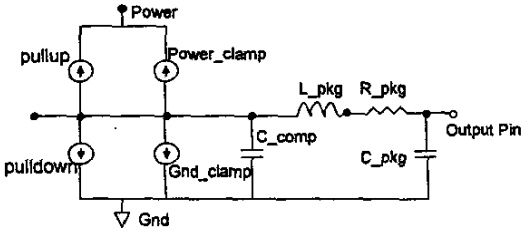


Figure 2: IBIS Output behavioral model

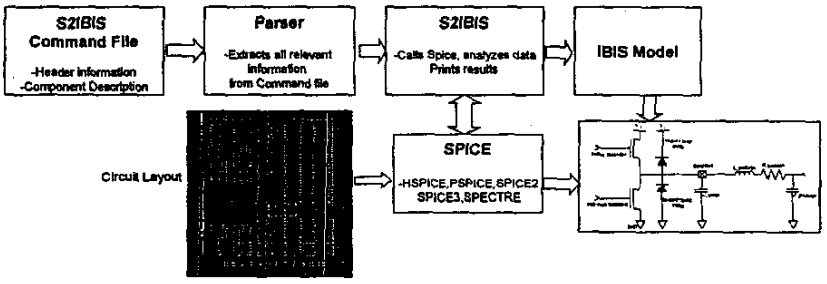


Figure 3 S2IBIS Tool Flow

Figure 3 shows a block diagram of the S2IBIS tool flow. The parser grabs all the information that has been passed by the user. The program then sets up all the file names and the SPICE files that are run once SPICE is invoked. As soon as the SPICE output files are created, they are examined for any errors or aborts. If there are no errors, the VI and VT tables are extracted from their respective files and formatted according to IBIS specification. The last step is to print the IBIS model into a file. The next section describes how the VI and VT tables are obtained using S2IBIS2.

3.1 Pullup and Pulldown curves.

Pullup and pulldown curves are derived for *output* models only. For both pullup and pulldown curves, S2IBIS2 attaches an input voltage source and an output voltage source. The input voltage is set so the output tries to drive high (for the pullup curve) or low (for the pulldown curve). The output voltage is swept from (Vgnd – Vcc) to 2* Vcc, and the output current at each output voltage is recorded.

If the driver has an enable input, the sweep is performed a second time with the driver disabled. This gives the performance of the clamping structure that may be present. The two curves are then subtracted – resulting in a curve that models the performance of only the driver.

3.2 Clamp curves

Power and ground clamp curves are derived for *input* models and the *output* models with enable inputs. To find the power and ground clamp curves for input models, S2IBIS2 attaches a voltage source to the associated pin and sweeps the voltage source. The current at each voltage point is recorded

To find the clamp curves for the 'output' models with enable inputs, a voltage source is attached to the associated pin, the driver is disabled (using the voltage source attached to the enable pin), and the output voltage is swept. The resulting current at each voltage point is recorded.

The sweep range for ground clamp curves is (Vgnd – Vcc) to (Vgnd + Vcc), and Vcc to 2*Vcc for power clamp curves.

3.3 Ramp rate curves

Ramp rates are derived for all *output* models. To find the ramp rates, S2IBIS2 attaches the output pin of the driver to the appropriate termination voltage through the resistor Rload, and provides the appropriate stimulus at the input. It should be noted that no packaging parasitics are involved in the simulations. The output waveform is then examined to find the 20% and 80% voltage points, and the time between them

Rload is specified in the command file. If it is not specified, it defaults to 50 Ohms.

3.4 Rising and Falling Waveform curves

Rising and Falling waveforms are produced for *output* models when they are requested with the [Rising Wavefrom] and [Falling waveform] commands.

Deriving rising and falling waveforms is similar to deriving ramp rates.

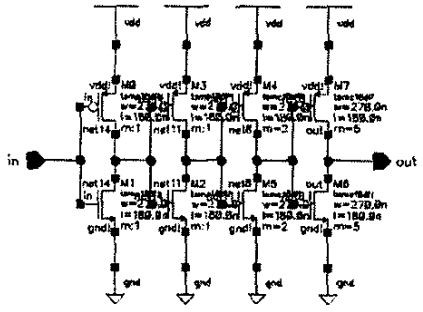
4. S2IBIS3

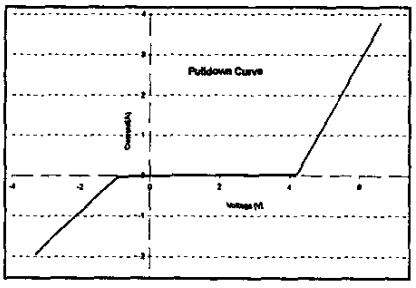
S2IBIS2 was written in C programmable language along with Lex and Yacc (for the purpose of parsing the command file). As such, different operating systems needed different versions of the tool. Moreover, S2IBIS2 could only generate IBIS V2.1 or lower generation models only whereas IBIS itself had evolved to Version 3.2. As such, S2IBIS3 was developed. The programming language used to develop S2IBIS3 is Java which makes it platform independent. S2IBIS3 is also backward compatible to all versions of IBIS.

A key feature that has been implemented in S2IBIS3 is the capability of handling convergence issues with HSPICE. Non-convergence occurs because the SPICE netlists are not accurate for the voltage range that they are swept with. If non convergence is detected, the user is asked to enter new sweep values for the beginning and the end of the sweep. SPICE is again run with the new values and if again faces non-convergence, comes back and asks for new values again. This procedure is repeated until SPICE converges or user aborts.

5. Buffer example and conclusion

Using S2IBIS3, an IBIS buffer model of a four stage, non-inverting buffer is created and the pullup, pulldown and the rising and falling waveforms are plotted and shown in figure 4.





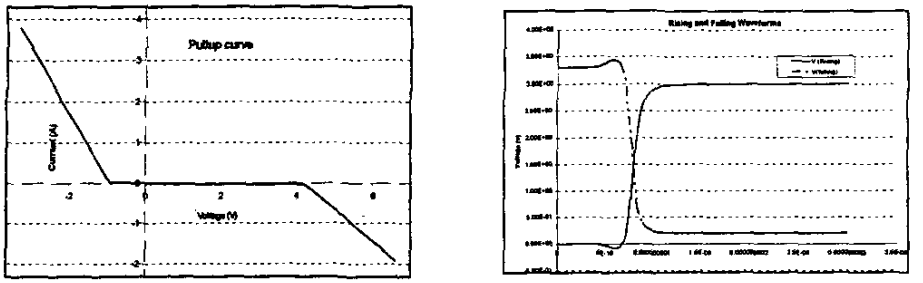


Figure 4 (from clockwise): 4 stage driver buffer, pulldown curve plotted from IBIS data, Rising and Falling waveform and Pullup curve.

This paper discussed the issues involved with the development of S2IBIS2 and S2IBIS3. These utilities are used to derive IBIS models of I/O buffers using their SPICE netlists. Critical issues such as non-convergence of buffers over a wide range of voltage sweep and setting up parameters to generate the static and dynamic characteristics are presented.

References

1. Introduction to IBIS Models, *Arpad Muranyi*, IBIS Model Training, San Jose, California - April 26, 2000
2. An Experimental Procedure to Derive Reliable IBIS Models, *Zak, T.; Ducrot, M.; Xavier, C.; Drissi, M.*; Electronics Packaging Technology Conference, 2000. (EPTC 2000). Proceedings of 3rd , 5-7 Dec 2000.