

AC Coupled Interconnect for Dense 3-D Systems

Stephen Mick, John Wilson, Lei Luo, Karthik Chandrasakhar, Paul Franzon
Department of Electrical and Computer Engineering,

Box 7914

NC State University,
Raleigh NC 27695

paulf@ncsu.edu; 919.515.7351

Abstract

AC Coupled Interconnection (ACCI), in conjunction with buried solder bump technology, provides a method to achieve signal I/O pitches of less than 100 μm and signaling rates greater than 3 Gbps per I/O on integrated circuits, while preserving excellent signal integrity. This paper presents a summary of approaches, status, advantages and disadvantages for two- and three-dimensional variations of AC Coupled Interconnect Systems.

Introduction

Achieving high-density connectivity with conventional I/O schemes presents a number of difficulties. All these schemes have, at their root, the concept of using a mechanical connection for signal transmission. To achieve reliable connections, the mechanical connection must be sufficiently compliant to withstand thermal cycling. Achieving a tight pitch, while maintaining compliancy is very difficult, as it usually results in a tall, thin, and thus relatively fragile and difficult-to-make mechanical structure. In addition, high density interconnect connections require greater smoothness and flatness of the surfaces being mated, often increasing their cost.

Transmission of digital (and many analog) signals do not require the DC and low frequency components. Thus the signals can be transmitted through series capacitors and transformers, no mechanical connection is needed. Previous efforts to explore capacitive coupling [1][2] have shown success but did not address issues such as how to connect power and ground.

An approach has been identified that solves this, and other, problems with AC coupling. The basic concepts are illustrated in the figures below. The first figure shows the physical structures. Half capacitors, or spiral inductors, are fabricated on the chip and the opposing chip or package surface. The chip side is covered with a thin overglass, to prevent accidental shorting. DC connections are provided through a dense field of conventional solder bumps. The bumps are buried either in the package or in the redistribution layer on the chip. This geometry brings the opposing half capacitors or spirals into close and controlled proximity.

The second figure shows equivalent circuits that can be enabled by these structures. Single-sided, partial and full differential can all be supported, with the normal tradeoffs. Inductive coupling provides the interesting potential for creating a differential circuit with only one pad per I/O.

This scheme has a number of advantages over the mechanical alternatives, including excellent compliance, good tolerance to temperature changes etc. It also permits high-speed signaling with excellent signal integrity.

Demonstrations

In previous work, we have demonstrated the following:

- The basic feasibility of capacitive coupling to support multi-Gbps signaling.
- The feasibility of using buried solder balls to precisely control the spacing and alignment within the structure.

Details will be included in the full presentation.

Discussion

This scheme has significant potential to provide for tight-pitch, low-cost 3-D interconnect structures:

- Capacitive connections have been demonstrated down to 20 μm pitch. However, to get a sufficiently high capacitance, the inter-plate spacing has to be small ($\sim 1 \mu\text{m}$) and well controlled ($\pm 0.5 \mu\text{m}$). The buried solder balls provide the basis for this control.
- While not capable of such tight pitches, inductive connections are feasible with much larger inter-winding gaps. Sufficient coupling levels can be obtained with inter-winding spacings up to half the inductor diameter. This reduces, possibly eliminating, the need for backside metallization and extensive thinning for 3-D stacked structures.

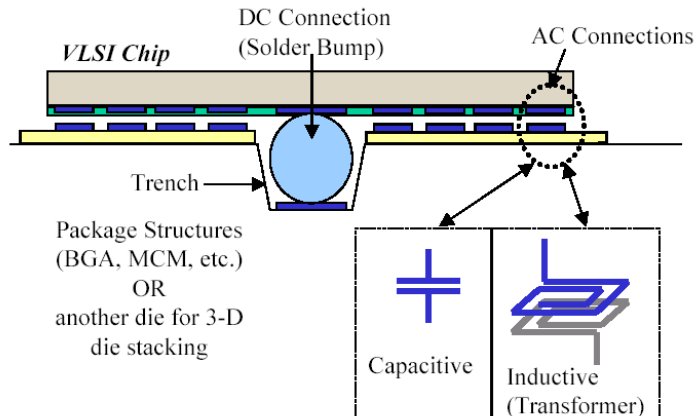
Details of the approaches and tradeoffs in using AC Coupled Interconnect for 3-D structures will be presented.

Acknowledgements

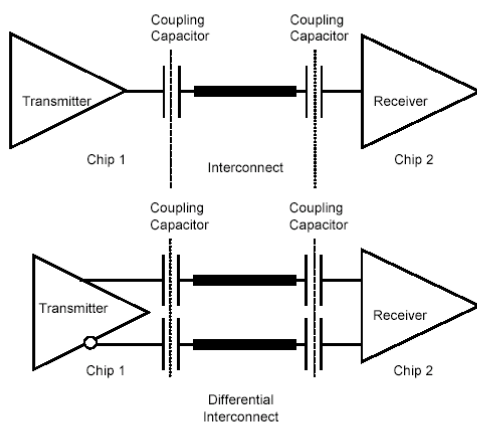
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References

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Capacitive Coupling



Inductive Coupling

