A Low Power PSK Receiver for Space Applications in 0.35-μm SOI CMOS

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Abstract

An all-digital and low power PSK baseband receiver circuit using silicon on insulator technology (SOI) is designed for space applications. The receiver employs double differential detection to improve receiver's robustness to Doppler effect as well as 1-bit A/D at the front to reduce complexity and power. Operating at UHF frequency (435 MHz), the receiver supports a wide range of data rates (0.1-100 kb/s). From test results, the power consumption of the baseband circuit including 1-bit A/D converter is below 1 mW for data rates up to 100 kb/s.

Introduction

Demand for low cost, compact and low power receiver circuits for use in wireless communication technology has continued to increase. Additionally, deep space communication receivers must be robust to radiation hardness and Doppler effect as well. SOI CMOS technology is attractive for deep space applications, offering high-performance, low power and good radiation radiation hardness [1]. The Doppler shift is sometimes several times wider in a space application for low data rates and often must be handled by circuit techniques. In an environment with a high Doppler shift, many modulation schemes require either pilot transmission technique or additional circuits [2][3] to handle the frequency shift. When used with a double differential technique, however, PSK is *invariant* to Doppler frequency offset [4] and enables a simplified, low power circuit implementation. The receiver requires no extra circuit such as pilot signal or PLL for carrier recovery, therefore resulting in high transmission efficiency and low circuit complexity.

The receiver presented in this paper is for Mars orbiter-lander communication system in a deep space environment. And low power is one of the most critical priorities. All digital baseband circuit makes the design of low power receiver feasible. The power consumption in a digital CMOS circuit is $P \propto CV^2f$, where C is the capacitance in the circuit, V is the supply voltage, and f is the operating frequency [5]. In order to minimize C, V and f, we adopt subsampling technique [3][6] to reduce the operating frequency, 1-bit A/D converter to reduce circuit complexity and capacitance, as well as SOI CMOS technology to potentially reduce the operational voltage and capacitance [1]. A novel timing recovery circuit for a multiple data rate (0.1–100 Kbps) is also designed and described for the receiver given here. Combining all these with power efficient circuit methods has resulted in a highly flexible and low power receiver.

Receiver Circuit

The double differential PSK (DDPSK) receiver with a 1-bit A/D is shown in Fig. 1. The baseband is designed for being used in two fully integrated receivers with two alternative front-ends. One of the receivers uses subsampling front-end, while the other includes one-stage downconverter as indicated in Fig.1. Both front-ends are currently being designed [7] [8]. In subsampling front-end, the received signal is sampled with a frequency less than the carrier but at least twice of data rate [3]. The sampling frequency (f_s) is chosen as $f_s=4/(2n+1)f_i$ $=[4,4/3,4/5,4/7\ldots\ n=0,1,2,3\ldots]f_i$ [9]. Depending on the front-end approach the incoming signal to the A/D is assumed to have the frequency f_i which can be equal to either the carrier frequency or a downconverted IF frequency. In this design, the receiver carrier frequency is 435 MHz and it is downconverted to 1 MHz if IF front-end approach is used. The sampling frequency, f_s is 4MHz which is obtained when n=0 for low-IF and n=217 for subsampling. Choosing the sampling rate as $4/(2n+1)$ provides the input signal to be sampled at the values of 1,0 and -1, resulting in significant reduction in hardware complexity.

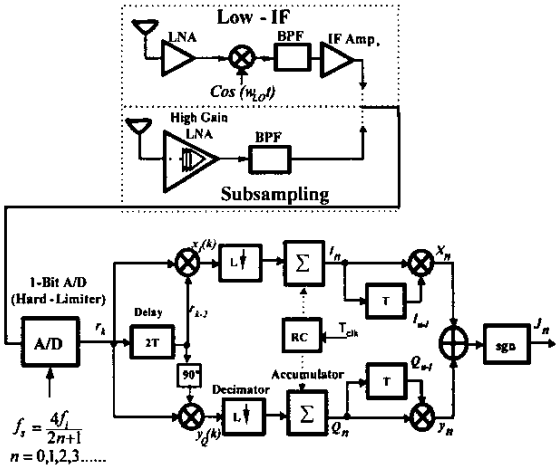

Fig. 1. Digital double DPSK receiver with the two front-ends

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A. Analog Front-end

A 1-bit A/D circuit has been designed for both front-ends. The analog signal is first quantized into 2 levels and sampled at 4 MHz (f_s=*4MHz*). It consists of a comparator followed by a sampling circuit (Fig.2). The comparator converts analog input sine signal to square wave (i.e. hard-limiting, Fig.3). The loss resulting from the hard limiting is about 2 dB, which is also reported in [9]. The comparator is designed as a two-stage differential amplifier providing further gain (~ 60dB @1 MHz) to the input signal to ease baseband receiver.

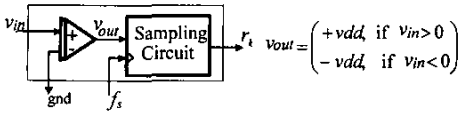

Fig. 2. 1-bit A/D converter

The required input dynamic range of the A/D is provided by the gains of the previous circuits. For the approach of low-IF front-end, the received signal is amplified by a LNA at 435 MHz and followed by an IF amplifier. However, for subsampling approach, the high gain required at the RF stage must be provided by a high gain LNA at 435 MHz.

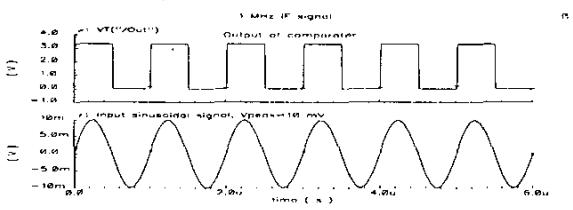

Fig. 3. 1 MHz IF signal converted to digital waveform by A/D

B. Baseband

The baseband includes two-stage differential decoders in order to remove any frequency shift. The first stage implements the autocorrelation technique; it converts frequency error into phase error, and then the second stage eliminates the phase error. This is because of the fact that the adjacent symbols are affected from the same frequency shift and phase error. As a result, the receiver utilizes non-coherent technique and does not require exact phase and frequency. Adding a 1-bit A/D at the front relaxes the power dissipation since the baseband becomes nearly all-digital and four mixers in the baseband are replaced by four logic *XNOR*'s. The low pass filters (the match filters) are implemented as accumulators or by up/down counters. The accumulators' size depends on the number of samples taken by the 1-bit A/D and the decimator. The number of samples is dropped more by the decimator and thus the size of the accumulators is reduced.

The implementation of delay units in digital DDPSK for variable bit rates is shown in Fig.4. It is important to point out that (2T, T) delay combination used in Fig.1 is to prevent high noise correlation at the output of the receiver [10]. Here T is the symbol duration, and T= 1/R where R is data rate. In the chip, either (T,T) or (2T,T) delay combination can be selected by a control MUX (e.g. as in Fig.4). In (1), we have the phase information encoded as a second-order phase difference. Assuming each phase sample is affected by an independent noise with variance σ^2, then $\Delta\varphi_n^1$ will have a variance of $6\sigma^2$ and $\Delta\varphi_n^2$ will have a variance of $4\sigma^2$. Accordingly, a 1.8 dB is gained by using (2T,T) combination over (T,T) one.

$$\Delta\varphi_n^1 = \varphi_n - 2\varphi_{n-1} + \varphi_{n-2} \quad \text{---}T,T \qquad \text{(1a)}$$

$$\Delta\varphi_n^2 = \varphi_n - \varphi_{n-1} - \varphi_{n-2} + \varphi_{n-3} \quad \text{---}2T,T \qquad \text{(1b)}$$

Fig. 5 shows an example of timing diagram at transmitter and receiver for digital DDPSK receiver. The binary data a_k is differentially encoded twice before transmission. After the first and second stage of differential encoding, the data is $c_k = a_k \oplus c_{k-1}$ and $d_k = c_k \oplus d_{k-1}$ respectively. Fig. 5(c) represents the second order phase difference modulated signal (PDM-2) of the actually transmitted data a_k which is obtained from the data d_k multiplied by a sinusoidal carrier frequency. Fig. 5 (d) illustrates that the received signal has a different frequency (i.e. half cycle loss) from the transmitted signal due to Doppler effect. Nevertheless after the second stage differential decoder, the signal (in Fig. 5(f)) is the same as a_k sent by the transmitter and no bit is detected erroneously.

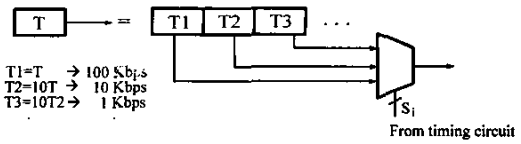

Fig. 4. Delay units in digital DDPSK for different bit rates

C. Timing circuit and Synchronization

A variety of impairments exist in practice that could cause performance degradation. The synchronization is the most critical issue in the practical implementation of a receiver. Digital DDPSK receiver is very robust to the impairments while many receivers are highly sensitive. The receiver utilizes non-coherent technique and does not require exact phase information. As mentioned previously, it is also invariant to frequency error. The two stage differential decoder in the baseband removes any frequency shift and phase uncertainty. The only critical part is the symbol timing synchronization. Block diagram for recovering symbol-timing clock (T_{clk}) for different data rates (0.1 Kbps, 1 Kbps, 10 Kbps and 100 Kbps) is given in Fig.6. A preamble sequence of '1010..' is sent for timing synchronization at the beginning,

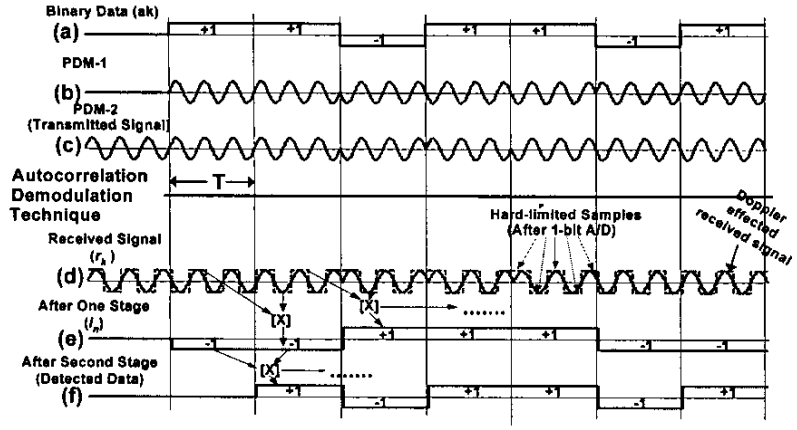

Fig.5 Timing diagram of autocorrelation techniques for digital DDPSK receiver

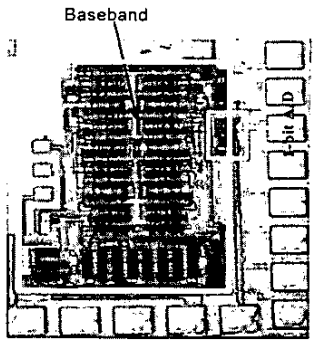

Fig. 8. Die photo of the chip

and '10' is added to data after every 8 bits to introduce enough transitions in order for the timing circuit to track the data. The simulation result in Fig.7 shows how the timing circuit recovers the clock from a sequence of 100 Kbps. The "Filter" circuit passes only those pulses having pulse width greater than or equal to $\tau = 2T_s$. This makes the circuit robust against fast Doppler rate and circuit noise. The Frequency Controller selects the appropriate down converter stage depending on the frequency and phase of the incoming data signal. The timing error results from inaccuracy of the timing circuit and reset circuit (RC) as well. From the simulation, the worst-case timing offset is less than 1/10 of the symbol period, which was our initial goal in order not to exceed a degradation of 0.1 dB.

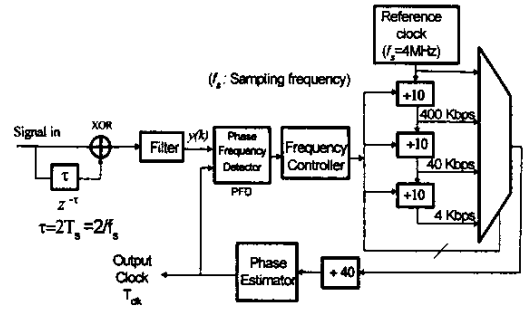

Fig. 6. Timing circuit for multiple bit rates

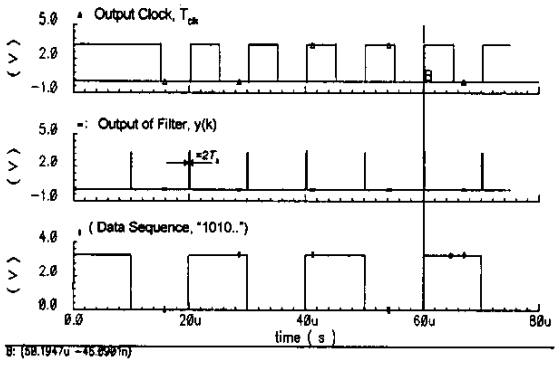

Fig. 7. Recovered timing clock for a data sequence of 100 Kbps.

Experimental Results

The receiver baseband with analog front-end of A/D converter is fabricated in 0.35-μm Silicon On Insulator (SOI) CMOS process at Honeywell. The die microphotograph is shown in Fig. 8. Fig. 9 shows the measured output for a 1 MHz input double differential PSK signal. The data a_k is the binary data that is differentially encoded twice (d_k) before transmission. In this testing result, the (T, T) delay unit in the chip is selected for simplicity of showing waveforms. Fig. 9(a) shows the input double differential PSK signal which is obtained from the data a_k. Fig. 9(b) represents the data observed at the output of the chip which is the same as the actually transmitted data a_k.

Fig. 10 illustrates the BER performance of the receiver for K=20,64 and 128, where $K=f_sT/L$, the number of samples at the accumulators in a symbol duration of T, and L is the decimator rate. Each accumulator has to be reset (by RC unit) every period of T in order to realize uncorrelated samples. These values are corresponding to different symbol rates for a constant sample frequency (f_s=4 MHz). For example, K=20 is for a data rate of 100 Kbps (when L=2). As can be noticed from Fig.10, at high SNR values the quantization effect becomes more obvious. In Fig.10 we also show BER performance of ideal DDPSK for BT=1 where BT is the product of the bandwidth and symbol duration [4]. Including the A/D, the baseband circuitry consumes a power of less than 1mW. At a BER of 10^{-4} (SNR~14 dB), the receiver sensitivity is –107 dBm for a noise figure of 3 dB and data rate of 100 Kbps. Table I summarizes the receiver performance.

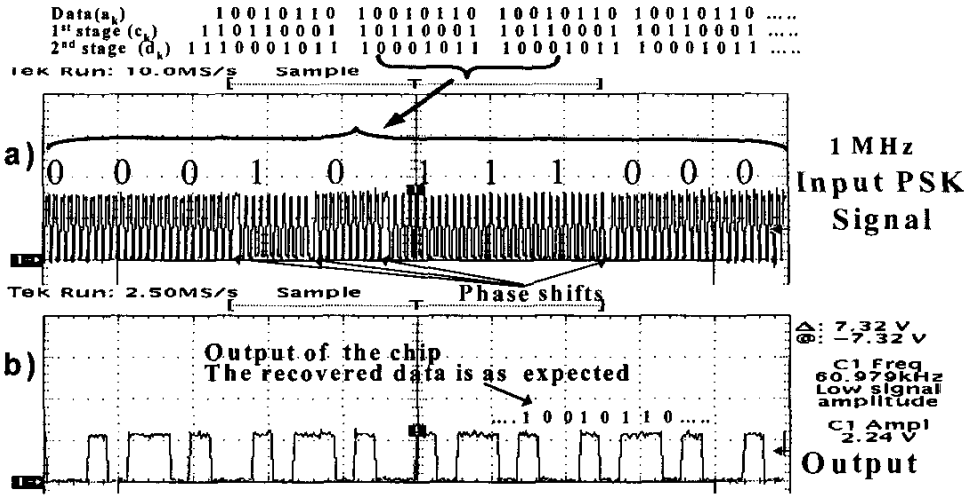

Fig. 9. The measured baseband output a) the input PSK signal-after two stage differential encoder b) the recovered data (= a_k)

Conclusions and Future Work

We have presented a low-power digital double differential PSK receiver using a 1-bit A/D. The baseband circuit including 1-bit A/D converter has been designed, simulated and fabricated through Honeywell's 0.35-μm SOI CMOS process. The receiver is designed for low power and tolerates large and fast frequency offsets due to Doppler. The critical practical implementation issues have also been addressed. The receiver has a sensitivity of -107 dBm for the data rate of 100 Kbps. Including 1-bit A/D, the digital baseband circuit consumes a power less than 1 mW.

A complete receiver including baseband, timing circuit in Fig.6, and low-IF front-end (in Fig.1) is being designed as a fully integrated system and will be fabricated soon.

Acknowledgement

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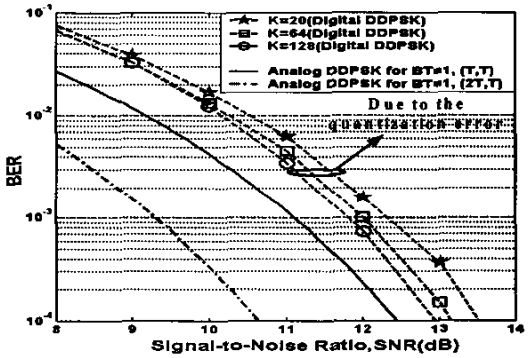

Fig. 10. BER performance of digital DDPSK (K=20,64 and 128)

TABLE I
RECEIVER PERFORMANCE

Modulation type	PSK
Carrier frequency	435 MHz
Input frequency to A/D	1 MHz (Low-IF) 435 MHz (Subsampling)
Sampling frequency	4 MHz
Technology	0.35-μm SOI
Sensitivity	-107 dBm
Data rate	0.1-100 Kbps
Power consumption	1mW
Supply	3 V for A/D 2V for Baseband