

AC Coupled Interconnect for High-Density High-Bandwidth Packaging

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Abstract

AC Coupled Interconnection (ACCI), in conjunction with buried solder bump technology, provides a method to achieve signal I/O pitches of less than 100 μm and signaling rates greater than 3 Gbps per I/O on integrated circuits, while preserving excellent signal integrity. This paper presents a summary of approaches and status capacitive and inductive versions of AC Coupled Interconnect Systems.

1. Introduction

Achieving high-density connectivity with conventional I/O schemes presents a number of difficulties. All these schemes have, at their root, the concept of using a mechanical connection for signal transmission. To achieve reliable connections, the mechanical connection must be sufficiently compliant to withstand thermal cycling. Achieving a tight pitch, while maintaining compliancy is very difficult, as it usually results in a tall, thin, and thus relatively fragile and difficult-to-make mechanical structure. In addition, high density interconnect connections require greater smoothness and flatness of the surfaces being mated, often increasing their cost.

Transmission of digital (and many analog) signals do not require the DC and low frequency components. Thus the signals can be transmitted through series capacitors and transformers, no mechanical connection is needed. Previous efforts to explore capacitive coupling [1][2] have shown success but did not

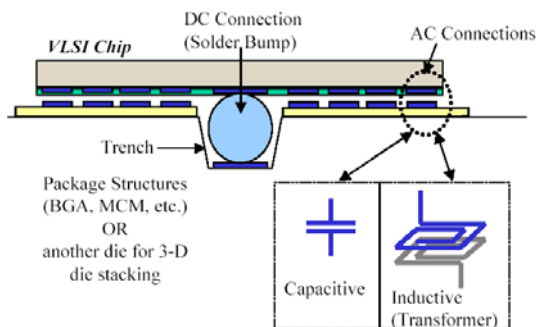


Figure 0. Overview of Scheme

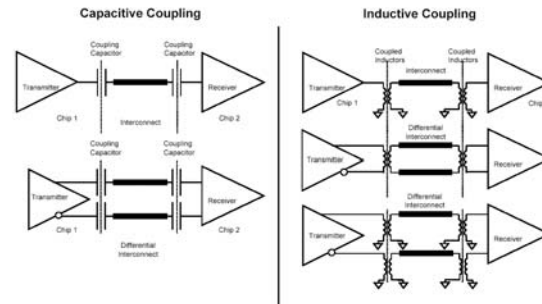


Figure 2. Electrical Equivalent Circuits for Interconnect.

address issues such as how to connect power and ground., and signal integrity.

An approach has been identified that solves this, and other, problems with AC coupling. The basic concepts are illustrated in the figures below. Figure 1 shows the physical structures. Half capacitors, or spiral inductors, are fabricated on the chip and the opposing chip or package surface. The chip side is covered with a thin overglass, to prevent accidental shorting. DC connections are provided through a dense field of conventional solder bumps. The bumps are buried either in the package or in the redistribution layer on the chip. This geometry brings the opposing half capacitors or spirals into close and controlled proximity.

Figure 2 shows equivalent circuits that can be enabled by these structures. Single-sided, partial and full differential can all be supported, with the normal tradeoffs. Inductive coupling provides the interesting potential for creating a differential circuit with only one pad per I/O.

This scheme has a number of advantages over the mechanical alternatives, including excellent compliance, good tolerance to temperature changes etc. It also permits high-speed signaling with excellent signal integrity.

2. Demonstrations

In previous work, we have demonstrated the following:

- The basic feasibility of capacitive coupling to support multi-Gbps signaling [3].

- The feasibility of using buried solder balls to precisely control the spacing and alignment within the structure [4].

Details will be included in the full presentation.

3. Discussion

This scheme has significant potential to provide for tight-pitch, low-cost high-density level one packaging.

Physically, no special steps or unusual materials are required to build the structure. The inductive coupled version can withstand larger inter-winding spacings than capacitive coupling, as is likely to be suitable for laminate packaging.

Electrically, the interconnect system is equivalent to a band-pass filter. Thus it is necessary to code the data to reduce low-frequency content. 4b/5b coding suffices in practice. Significant power savings are achieved as the interconnects acts as a differentiator, transforming edges into pulses. This reduces the pulse high time, and thus the power. The details of the band-pass can be tuned by changing physical parameters in the structure. Low crosstalk characteristics have been measured.

Good Bit Error (BER) rates can be achieved. The key factors that permit a low BER include having sufficiently high coupling factors, full-swing drivers, and coding.

4. Conclusions

AC Coupled Interconnect has high potential to permit the low-cost construction of

high pin-count packages. It can achieve the pin-counts specified at the end of the International Technology Roadmap for Semiconductors using today's physical technologies.

Acknowledgements

This work was supported by SRC under contract 99-NJ-722, NSF under grants EIA-9703090 and CCR-0219567, and USAF under contract F29601-03-2-0135. The authors wish to thank MCNC for providing solder bump services.

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