Buried Solder Bump Connections for High-Density Capacitive Coupling

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Abstract

AC coupled interconnects enable reliable, multi-gigabit-per-second communication data rates between integrated circuits with very high pin counts and low power consumption. When used in conjunction with NRZ-tolerant receivers, interconnect arrays with pitches below 100μm and data rates of 6Gbps/per pin can be built.

Introduction

Capacitive coupling has been proposed as a means to enable high data rate interconnection between ICs within a multichip module (MCM) [1]. Capacitive coupling has been implemented by forming half of the capacitors on the ICs within the MCM and the other half of the capacitors on the MCM substrate. When the chip is brought into close proximity to the substrate, a capacitor is formed. In [1], no mechanism is presented to allow DC connections to exist across the same interface as the AC coupled signals.

AC coupling has been demonstrated with capacitive elements. Also, a novel physical structure, buried solder bumps, has been developed to solve the lingering problem of previous AC interconnection schemes of providing DC power and ground connections across the same interface as the AC connections. Simulated and measured results as well as the physical package aspects of this work are described.

Buried Bump Technology

In order to operate a CMOS chip, DC power and ground voltages must be supplied. To have numerous DC paths, physical connections must be established, but even the most aggressive connection methodologies introduce a gap between the chip and substrate in the tens of microns. To implement capacitive coupling, the chip and substrate must be brought into close proximity (i.e. between 2 to 5 microns apart). A novel physical structure has been developed that allows both chip-to-chip communication via AC coupled interconnects and DC paths across the chip-substrate interface. The fabrication process of the physical structure is compatible with standard CMOS processing techniques.

A cross-section of the structure is shown in Figure 1. The structure consists of multiple ICs and a common substrate. Trenches are created in the substrate using standard manufacturing processes. Solder bump landing pads are created in the substrate trenches. A routing layer is created on the substrate to allow DC voltages to be brought to the solder bumps and to allow interconnection between ICs via the AC coupling elements. A portion of each AC coupling element is fabricated on the substrate surface wherever AC interconnections to an IC are desired. VLSI chips can be created with any standard CMOS fabrication process. Pads for solder bumps should be fabricated on the top-level metal of the chips where DC connections are desired between the chip and the substrate. The corresponding portion of each coupling element should be fabricated on the chip surface where it is needed to AC couple signals to the substrate.

Using this structure, a bumped chip can be positioned over the substrate so that the solder bumps can be recessed into the trenches and corresponding AC coupling elements aligned. Once the solder bumps are bonded to the substrate, the chip and substrate are separated by a 2 to 5 micron gap and AC coupling can be achieved through corresponding coupling elements.

This technique works because solder balls are well controlled and uniform structures. The solder balls can be made as large as necessary to provide the required compliance. All the usual advantages of solder bump assembly, such as self-alignment, are still useful in this structure. The technique is extendible to other package materials, including ceramics and plastics.

Capacitive Coupling Overview

The physical structure enables the simultaneous creation of DC and AC coupled paths between a chip and substrate, but this structure can be viewed from a circuit point of view. A basic circuit schematic for a capacitively-coupled system is

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shown in Figure 2 where the series capacitances represent the coupled elements formed from the described physical structure. The combination of the intentional series coupling capacitance and driver/receiver shunt parasitic capacitance creates a channel from the driver to the receiver with a bandpass response. The edge rates of the driver output (dV/dt) are an important parameter in passing information through this channel since the transitions of the output of the driver are received as pulses at the input of the receiver. The low pass filtering that occurs due to the output impedance of the driver, the parasitic capacitance of the driver, and the parasitic capacitance of the coupling capacitor slow the edge rate of the transmitted signal. This reduction in dV/dt means that the amplitude of received signal is decreased, and it also increases the duration of the received pulse. Circuits capable of meeting the requirements of a capacitively-coupled system have been described in [2].

Capacitive Coupling Measurements

Measurements were made on integrated CMOS circuits with 3-stage inverter drivers and receiver circuits specifically designed for recovering capacitively coupled data [2]. The tested chips (Figure 3) were fabricated at MOSIS in the TSMC 0.35μm technology. Each driver output was connected in series to an integrated on-chip multi-level metal capacitor– either a small capacitor (75μm x 75μm) or a large capacitor (150μm x 75μm). Also, each receiver input was connected in series to an on-chip capacitor – either a small or large capacitor as described above. The outputs of the transmitter capacitors and the inputs of the receiver capacitors were each connected to probe pads.

Transmitters and receivers were connected to each other with bond wires. Figure 4 shows the measured results from the sequence of transmitter, large coupling cap, bond wire, large coupling capacitor, and receiver. The waveforms in the figure were measured at the transmitter input, at the bond wire, and at the receiver output. The input to the driver was a 3.3V, 2GHz square wave. The total delay through the system was measured to be 212ps. Distortion of the input waveform was an effect of impedance mismatch between the test equipment and the transmitter input. In spite of this, the receiver correctly recovered the input waveform. With NRZ data coding, the transmitter/receiver system recovered data correctly at an operating frequency of 4Gbit/sec. The system was also measured with a 3.3Vpp, 3GHz square wave input, but band-limiting effects in the measurement equipment and the transistors' unity gain frequency caused the output of the receiver to be sinusoidal in shape. Simulation results of the system in the measurement testbed predicted this band-limiting behavior although the receivers still correctly recovered the input signal. A test environment is being fabricated to measure the signal integrity of the capacitively coupled system for random data patterns and for long interconnections. Also, the 0.35μm designs are being redesigned for fabrication in a 0.25μm technology.

Capacitive Coupling Simulations

Recent simulations across all process corners were performed on several system configurations for circuits in the TSMC 0.25μm technology and the performance of the previously fabricated system is expected to improve. In addition, performance metrics have been identified for using capacitive coupling in a transceiver. It has been found that the data must be encoded to avoid long sequences of logic high or low from being transmitted since coding reduces the effects of inter-symbol interference. Also, simulations show that a capacitively-coupled system can correctly recovery 6Gbps NRZ data with a minimum coupling capacitor of 150fF. Figure 5 shows that a capacitive coupling system with a lossy transmission line has a bit error rate of less than 10^{-12} for a 6Gbps, NRz, 4bit-to-5bit coded pseudo-random data with pattern length of 2^{31}-1. In terms of I/O density, a 150fF capacitor would have a physical footprint of 92μm per side with a gap of 2μm between capacitor plates and a dielectric with $\varepsilon_r = 4$ between the capacitor plates. This would allow AC interconnections to be placed on a 100μm pitch.

Discussion

For long connections, each capacitor is seen in series with the transmission line and the impedance of these elements must be considered. A lossy transmission line can be used to attenuate reflections from the receiver, but to completely avoid reflections on the transmission line some form of transmitter-side matching must be implemented. To accomplish this matching, the magnitude of the impedance of the transmitter output in series with the capacitor must be equal to the transmission line impedance. However, a 50Ω capacitor at 2GHz with a 2μm intra-plate gap and an air dielectric must be 1500μm per side to be impedance matched! We are investigating an inductively coupled alternative to capacitive coupling that can provide a 50Ω match to a transmission line.

The prospects for capacitively coupled interconnection improve as transistor technology improves. Communication via capacitive coupling relies on fast edge rates to transfer data across series capacitors and edge rates achievable with a three stage inverting driver will improve as the designs are fabricated in 0.25um and 0.18um technologies. Also, the

unity gain frequency of transistors will continue to increase and thereby allow higher data rates to be achieved. As the operating frequency increases, the capacitors can be made smaller while allowing the possibility of an impedance match. Further, the use of underfills in the physical technology could introduce a dielectric constant larger than air for the capacitors and allow the size of a matched capacitor to shrink.

AC coupled interconnects can be thought of as connecting a transmitter to a receiver through a band-pass channel. The pass band generally covers a decade of frequency and the cut-off frequencies can be manipulated by changing the details of the physical structure. Optimization of the physical structure, the circuit topologies used for the transceiver and the frequency response of the band pass channel is ongoing.

The nature of high-density I/O requires high-density wiring. However, in the case of AC coupled interconnect (capacitive or inductive), the package wiring does not have to match the pitch of the IC wiring. The substrate demonstrations in this work were performed using silicon structures (for ease of fabrication in an R&D environment), however, there is no reason that this approach cannot be used in ceramic or plastic packaging. For example, holes could be punched in the top layer of a ceramic package, when in green tape form, to permit later solder ball attachment. So far, no fundamental barrier to exploitation has presented itself.

Conclusions

A new approach to building 100μm pitched arrays of 6Gbps/per pin digital chip-to-package connections has been developed in which digital signals are carried using contactless series capacitance structures. By being contactless, high densities can be achieved without the mechanical, compliance and rework complexities typically associated with fine pitch interconnects. Buried solder bump DC power and ground connections can be used to keep the opposing half capacitors in close proximity. Interconnect pitches down to 100μm are possible with capacitive coupling and smaller pitches are expected with inductive coupling. NRZ-tolerant transceiver topologies are being optimized to best exploit this technology and inductively-coupled alternatives to capacitive coupling are being investigated. Experiments have been performed to demonstrate the feasibility of both the buried solder bump concept and the overall interconnect circuit structures.

Acknowledgements

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References

[1] T. Knight, "Capacitive Chip to Chip Interconnections", Polychip Inc and M.I.T. Artificial Intelligence Laboratory, ca 1990.

[2] S. Mick, J. Wilson, and P. Franzon, "4Gbps High-Density AC Coupled Interconnection", Proceedings of the IEEE Custom Integrated Circuits Conference, 2002, pp. 133-140.

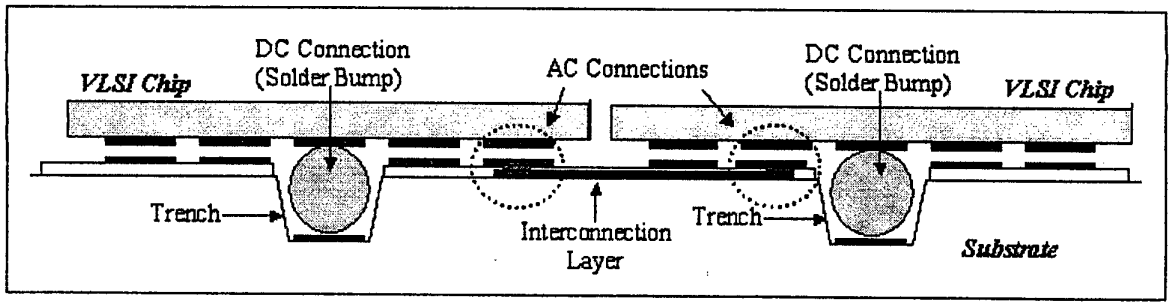

Figure 1: Cross-section of physical technology for AC Coupled Interconnection

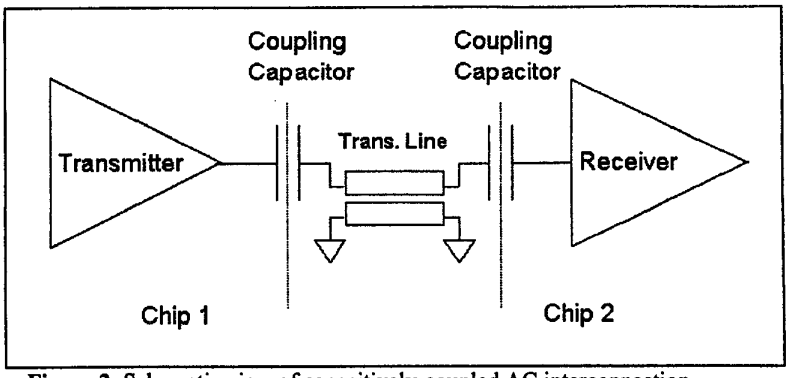

Figure 2: Schematic view of capacitively-coupled AC interconnection

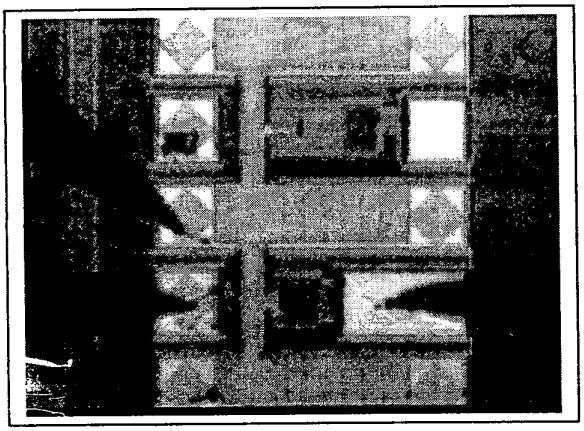

Figure 3: Die photo of capacitively-coupled experiment under measurement, TSMC 0.35μm technology

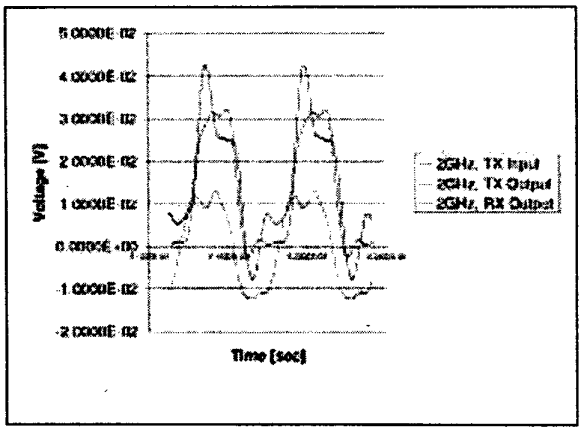

Figure 4: Measured 2GHz waveform (4Gbps NRZ) of capacitively coupled system

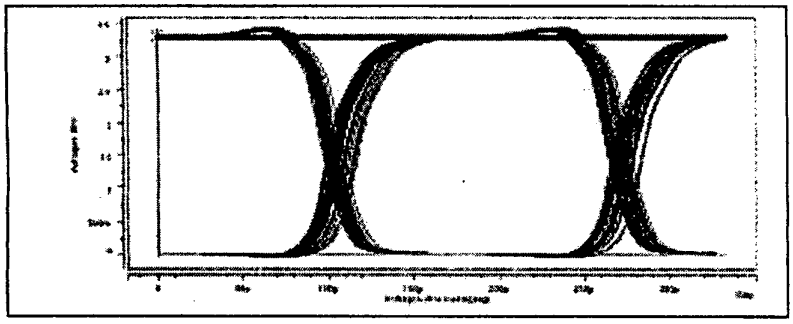

Figure 5: Simulated eye diagram of 6Gbps NRZ data transmission across capacitively coupled system with 150fF coupling capacitors, 200fF parasitic shunt capacitors, 3cm lossy transmission line, TSMC 0.25μm technology.