# Packaging Technology for AC Coupled Interconnection

Stephen Mick (semick@eos.ncsu.edu)[1]
Dr. Paul Franzon (paulf@ncsu.edu)[1]
Alan Huffman (huffman@mcnc.org)[2]

*1. North Carolina State University, Raleigh, NC*
*2. MCNC, Research Triangle Park, NC*

**I. Abstract**
AC Coupled Interconnection is a promising new technology that will provide multi-gigabit-per-second communication data rates between integrated circuits with very high pin counts and low power consumption. This technology can be used to bring signal pad pitches down to 75μm while maintaining a controlled impedance connection. The AC Coupled Interconnect method uses coupled elements to communicate AC signals between integrated circuits and a buried solder bump structure to communicate DC signals between the same interface. Work has been done to design, fabricate, and measure the performance of an innovative physical structure that will enable flip-chip packages to exploit AC coupled interconnects for chip-to-chip communication. This paper presents results from this work and discusses the constraints placed upon the packaging as a result of using both coupled elements and buried solder bumps. Experimental results from bonded chips show that more than 6000 signal I/Os can be fabricated in an area less than $1mm^2$ and that each connection can provide a bandwidth in excess of 2GHz.

**II. Introduction**
The demand is increasing rapidly for high-density, high-bandwidth off-chip I/O. Though the average densities implied by the National Technology Roadmap for Semiconductors are similar to solder bump densities achievable today, the peak I/O densities in future products are expected to be very high (for example to provide wide memory bandwidths for communications and multimedia processing).

The need for increased I/O bandwidth is currently being addressed through research programs aimed at increasing the density of solder bump technology and at improving the signaling rate for each connection. A number of programs are aiming at achieving 50 μm or better solder bump pitches but there are many known difficulties with achieving such pitches over large areas. The difficult compliance issues faced by small solder bumps are well known, and many attempts have been made to produce high aspect ratio solder bumps, with some success but little impact due to manufacturing cost issues.

Simultaneously, a number of circuit design researchers are building new circuit topologies capable of multi-Gbps signaling. Approaches being explored include: Source-synchronous techniques to limit the effects of clock skew [1]; Small-swing differential techniques to improve toggle rate and power-per-bit [2] and; Equalization to compensate for the skin effect [2].

In addition to circuit techniques, high-density and high-bandwidth I/O can be enabled by optimizing the physical interconnection technology. The mechanical limitations of soldered or similar contact technologies can be circumvented by using a contactless technology for AC signals. Specifically capacitively coupled connections can be used, whereby a capacitor is formed by a metal plate on the chip closely spaced to a substrate metal plate and separated by the overglass layer in the IC (Figure 1). Such an approach is appropriate for most I/O signals since it

recognizes that the DC connection carries no information. Further, removing the need for physical compliance greatly relaxes the potential mechanical problems in building high-density connections. Inductively coupled connections could be used whereby inductors are formed both on the surface of a chip and the substrate surface and a coupled connection is formed when the chip surface is brought into close proximity to the substrate (Figure 1). The surface of the substrate can be manufactured to be compatible with solder bumps and thereby maintain DC connections where they are needed (Figure 2).

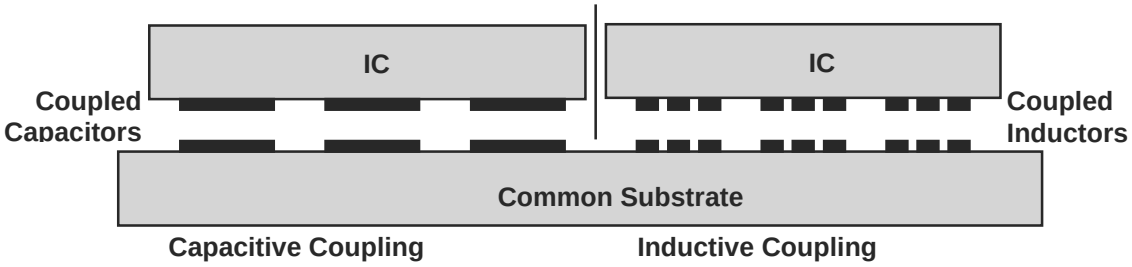


***Figure 1**: Chip-substrate interconnection using (a) capacitive and (b) inductive coupled elements*

This paper presents the physical tradeoffs that constrain the design of a flip-chip system for use in an AC coupled interconnection environment. Results from fabrication of chips and substrates are then presented and discussed.

**III. Substrate Design**

In the proposed interconnection technique, several ICs will be attached to a common substrate. A cross-section of a complete structure with both coupled and direct connections is shown in Figure 2. As a demonstration, the substrate has been fabricated from a silicon wafer. Trenches are created in the silicon substrate using bulk micromachining processes. Solder bump landing pads are created in

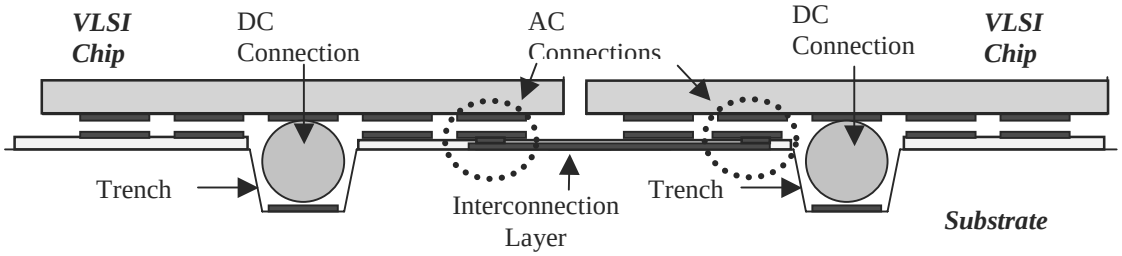


***Figure 2**: Cross-section of substrate to enable both DC and AC-coupled interconnection across the same chip-substrate interface*

the substrate trenches. A routing layer is created on the substrate to allow DC voltages to be brought to the solder bumps and to allow interconnection between ICs via the AC coupling elements. Multiple routing layers can be fabricated to support a greater number of signal connections.

A portion of each AC coupling element is fabricated on the substrate surface wherever AC interconnections to an IC are desired (e.g. one plate of a capacitor or one-half of a transformer using spiral inductors). The ICs can be created with any standard CMOS fabrication process.

Coupling elements should be fabricated on the top-level metal of the chips where AC connections are needed, and solder landing pads should be fabricated on the top-level metal where DC connections are required.

Using this structure, a bumped chip can be positioned over the substrate so that the solder bumps can be recessed into the trenches and corresponding AC coupling elements aligned. Once the solder bumps are bonded to the substrate, the chip and substrate are separated by a small gap (1 to 10 microns) and AC coupling can be achieved through corresponding coupled elements.

**IV. Packaging Constraints**

Several tradeoffs exist in designing a complete physical system (Figure 2). Among the tradeoffs are trench geometry (i.e. depth, width and density), coupling element performance and coupling element density.

The trenches in a prototype of the physical structure were designed to be a depth slightly less than the height of a reflowed solder bump. During the reflow process, the solder bumps pull the chip toward the substrate and define a fixed gap between the surfaces of the chip and substrate.

The width of the trenches in the prototype was set by the desired width of the solder bump landing pad and by the fact that anisotropic micromachining was used to create the trenches in the silicon substrate. With the given trench creation process, the trench sidewalls were fixed by the silicon crystalline planes to be $54.7^{o}$. Thus, the trench width at the top of the trench was constrained to be 1.4 times the depth of the trench plus the width of the solder bump landing pad. With a different material system the trench width could be made independent of the trench depth.

The performance of the coupling elements is related to the height of the chip-substrate gap. The performance of capacitive coupling elements degrades as an inverse function of the squared gap height. Thus, capacitive coupling implementations require a very small gap height (on the order of 1-2μm) that is consistent across the entire chip-substrate interface. The performance of inductive coupling elements is less susceptible to the gap height. As a rule of thumb, the gap needs to be less than a quarter of the diameter of the smallest inductor. Since, the inductors have a diameter on the order of 60μm, the gap between the substrate and chip must be kept below 15μm.

Also, the coupling element performance is affected by the relative alignment of the substrate and chips. Capacitive coupling elements are more susceptible to performance degradation due to misalignment than inductive coupling elements. However, inductive coupling elements are more susceptible to crosstalk than capacitive elements. In either case, alignment must be tightly controlled, but the amount of misalignment can be controlled by appropriately sizing the trench (width and depth) and the solder bump landing pad.

The density of coupling elements is limited by the number of available metals and the design rule constraints upon the metal traces. Consider an array with inductive coupling elements as an example. For each inductive coupling element, a via and perhaps a signal trace are required to connect one terminal to ground and another signal trace is required to route the AC signal from the second inductor terminal. Thus, the standard problem of breakout exists for inductive coupling as for any other high-density interconnect method.

The problem is complicated by the fact that inductors are sensitive to crosstalk and by the fact that inductors on the perimeter of the chip can have many signal lines passing below them depending upon the number of signal layers in between power and ground planes on the substrate.

The exact number of signal lines passing below perimeter inductors will be constrained by the maximum allowable crosstalk for a given application as well as the number and design constraints of the metal traces.

## V. Experimental Results

Chips were fabricated and bumped at MCNC and the corresponding substrates were fabricated at NC State University. A basic unit cell, consisting of a trench surrounded by 12 pads for capacitive AC coupling, was arrayed to create a single substrate. Different unit cell dimensions were used in various substrate designs.

The trenches were micromachined to a depth of 26μm into the silicon substrate using an anisotropic silicon etchant. The under-bump metallurgy used for the solder bump pads consisted of a Ti/Cu stack. SEM images were taken of joined chip/substrate pairs. Figure 3 is an SEM image of a joined chip/substrate pair that had a $30 \times 30$ array of 26μm deep trenches, 80μm bump pads, and 31μm tall solder bumps. This image was taken from the center of the chip/substrate pair. The 7.5μm gap in this image was seen to be uniform across the entire edge of the chip/substrate joint.

Tensile pull tests were performed on several joined chips and substrates and it was found that the joints could withstand a pull between 50 to 70 pounds before tearing apart. Figure 4 is an image of a section of a substrate after separation from a pull test. Although the complete array of solder bumps is not shown in the image, it was observed that all of the solder bumps across the substrate were successfully joined. It was also observed that the alignment of the chip and substrate was moved slightly off-center.

Further experiments that will use inductive coupling elements are in progress. Comprehensive lifetime, reliability, and tensile pull tests are planned.

## VI. Discussion

The density of I/O that can be achieved with coupled elements exceeds the NTRS roadmap requirements. With the least aggressive spacing fabricated in the chips and substrates at MCNC and NCSU, 484 solder bumps and 5808 capacitive AC coupling pads were fabricated in a 9.42mm x 9.42mm area. Thus it was possible to provide 6292 pins for a single chip in an area less than $1cm^2$. Likewise, with 12 inductive elements surrounding the perimeter of each trench, a unit cell can be stepped across a 9mm × 9mm die (assuming 75μm diameter inductors on a 100μm pitch) to yield 6075 AC interconnects and 506 power and ground pins. Of course, other unit cell designs can allow the ratio of DC to AC connections to be easily manipulated. For high-performance applications in the year 2011, a 9mm × 9mm die size is far smaller than the die sizes predicted by [3], but the achievable I/O density is greater than the I/O density requirements. Thus AC coupling may enable a current technological barrier to be overcome.

Achieving these high densities requires little change in the current manufacturing flows, apart from the construction of the solder bump trenches. For capacitively coupled interconnect the capacitor dielectric is simply the normal overglass in series with the expected air gap -- a similar structure is used for inductively coupled structures. If an under-fill is desired, it is anticipated that it can be incorporated in the bump trenches. Moreover with this connection methodology, very aggressive solder bump sizes do not have to be used. Instead, the solder bumps can be made as large as necessary to provide the required number of DC connections as long as the trench size is

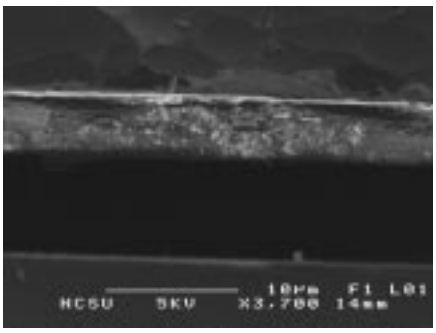


***Figure 3**: Joined chip and substrate -- 26μm deep trenches, 80μm bump pads, 31μm tall solder bumps (before reflow), uniform 7.5μm chip-substrate gap (after reflow)*

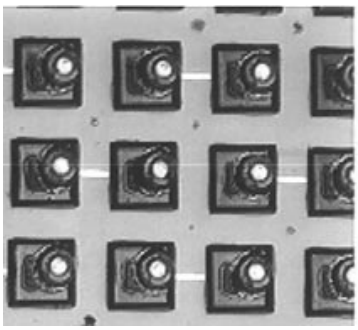

***Figure 4**: Substrate image after tensile pull test separation*

adjusted to ensure that the final structure has a controllable gap between the surfaces of the chip and substrate.

In the frequency domain, AC coupled interconnect can be thought of as a band-pass circuit. The acceptable pass band generally covers a decade of frequency. The cut-off frequencies can be manipulated by changing the details of the coupling elements. Structures presently being built and measured provide connection bandwidth in the range of 2-6GHz per connection. The per-connection bandwidth is limited by transistor performance so the connection bandwidth will increase as transistor technology continues to improve.

Any package that could support over 5,000 signal I/Os will require high-density wiring. However, the package wiring does not have to match the pitch of the IC wiring. In fact, in the case of the inductive coupled structures, this difference in wire width/pitch can be used to improve the system performance. That is, since the IC will allow finer line width and spacing, it can have inductive elements with more turns (and a slightly higher value of inductance) than the inductors on substrate with fewer but wider turns. This difference in inductance can be used to effect an impedance transformation between the chip and substrate and ease the constraints placed upon the signal traces. Another advantage of inductive coupling is that it reduces the co-planarity requirements over capacitive coupling; potentially making even laminates, with their relatively rough surfaces, feasible.

Though the feasibility demonstrations were performed using silicon structures (for ease of fabrication in an R&D environment), there is no reason that this approach cannot be used in ceramic or plastic packaging. For example, holes could be punched in the top layer of a ceramic package, when in green tape form, to permit solder ball attachment. So far, no fundamental barrier to exploitation has presented itself. Moreover, the use of buried solder bump technology could prove useful in other application areas such as connectors and sensors.

## VII. Conclusion

A new approach to building very high density, high bandwidth and low-power digital chip-to-package connections has been developed, in which digital signals are carried using contactless series capacitance and inductance structures. By being contactless, high densities can be achieved without the mechanical, compliance and rework complexities typically associated with fine pitch

interconnects. Solder bumped DC power and ground connections can be used, while keeping the opposing half capacitors or inductor spirals in close proximity, by burying the solder bumps in trenches in the package. Interconnect pitches down to 75μm are possible At a pitch of 100μm, for example, 6075 signal I/O and 506 power & grounds in a 9 x 9 mm die. New transceiver topologies are desired to best exploit this technology. Receivers are best designed to be NRZ tolerant, and current mode circuits have advantages in the inductively coupled structures. Experiments have been performed to demonstrate the feasibility of both the buried solder bump concept and the overall interconnect circuit structures.

**Acknowledgements**
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**References**
[1] T. Arabi, et.al., "Modeling, Simulation and Design Methodology of the Interconnect and Packaging of an Ultra-high speed source synchronous bus", 1998 IEEE EPEP, pp. 8-11.
[2] J. Poulton, "Signaling in High Performance Memory Systems", IEEE ISSSCC tutorial, 1999.
[3] "Assembly and Packaging," *International Technology Roadmap for Semiconductors: 2000 Update*, pp. 7-8.