4 Gbps High-Density AC Coupled Interconnection

(Invited Paper)

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Abstract

AC coupled interconnects enable multi-gigabit-per-second communication data rates between integrated circuits with very high pin counts and low power consumption. AC coupling can be realized with either series capacitive or inductive coupling elements. Capacitive AC coupling offers better performance when low power I/O buffers are required and when there is sufficient area to dedicate to coupling capacitors in the top-level metal of each IC. At a slight expense of circuit complexity, inductive AC coupling can be used to bring I/O pad pitches down to 75μm and maintain a controlled impedance connection. A novel physical structure, buried solder bumps, are used as a solution for providing DC power and ground connections across the same surface as the AC connections. When used in conjunction with NRZ-tolerate receivers, and current-mode signaling, highly effective interconnect structures can be built. As well as presenting both physical and circuit aspects of this work, experimental results are shown.

Introduction

Interconnect methodologies are driven by a number of factors such as interconnect density, aggregate bandwidth, signal integrity and power requirements. High bandwidth interconnect systems capable of multi-Gbps signaling are currently under investigation by a number of groups. These high data rates are being achieved by exploiting source-synchronous techniques to limit the effects of clock skew [1], using small-swing differential techniques to improve toggle rate and power-per-bit [2] and using equalization to compensate for the skin effect [2]. Researchers are also looking at a variety of methods to increase the density of interconnections [3]. One common aspect of each of these interconnection schemes is the dependence upon a direct, mechanical path for every I/O.

Relying upon a direct path for every I/O limits achievable density in pin and ball grid arrays and creates rework and compliance problems in very high-density solder bump arrays [4]. The International Semiconductor Technology Roadmap (ITRS) anticipates future high performance systems requiring 4,000+ pins and that current technologies cannot scale to the required densities [12]. As will be shown, AC coupled interconnects will more than exceed this target while providing a simple mechanical interface.

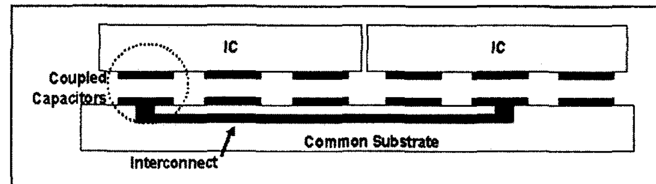

Figure 1 Basic capacitively coupled interconnection

The central thesis is the work hinges on the recognition that the DC component of a digital signal carries no information, and that non-contacting AC connections can be built a lot denser and simpler than DC connections. An array of non-contacting structures is inherently denser, more compliant and more mechanically robust than an array of contacting structures. By imposing direct contacts only where DC signal transfers are needed, this approach will allow very high density interconnects to be realized and alleviate the compliance and rework problems encountered in other high density interconnect technologies.

Capacitive coupling has been proposed as a means to enable high data rate interconnection between ICs within a multichip module (MCM) [5]. Capacitive coupling has been implemented by forming half of the capacitors on the ICs within the MCM and the other half of the capacitors on the MCM substrate (Figure 1). When the chip is brought into close proximity to the substrate, a capacitor is formed. In this implementation, no mechanism is presented to allow DC connections to exist across the same interface as the AC coupled signals.

Inductive coupling has been used extensively in smart cards, radio-frequency identification (RFID) systems, and in other contactless systems to communicate both power and signal information across an interface [6-8]. With these techniques, both AC and DC signals can be coupled across a chip-chip interface onto the same inductor. The size of the inductors must be very large to send both

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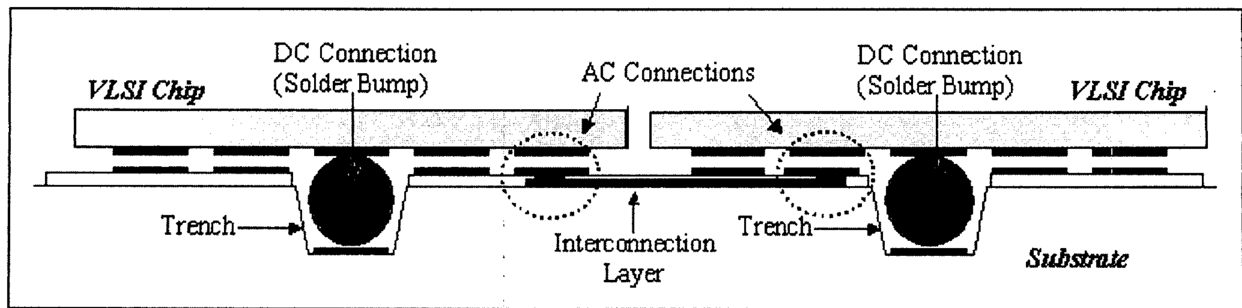

Figure 2 Novel buried bump system enabling DC and AC connections across the same interface

power and AC signals, which negates the ability to have high density I/O. However, if inductive coupling is used only to transfer the information in AC signals across the chip-chip interface then the inductors can be made on the order of 50μm per side. Implementing inductively coupled structures requires replacing the half-capacitor plate shown in Figure 1 with a spiral inductor.

In the remainder of this paper, a novel physical structure is presented that allows both DC connections and AC coupled paths (via capacitive or inductive coupling) across the same interface while maintaining low power, high density, and high data rate communication between integrated circuits. Then, the circuit and system requirements for capacitive coupling are discussed and analysis based upon measured results is presented. Circuit and system requirements for inductive coupling are discussed and analysis is presented based on measured results. Then a discussion is presented on the potential for AC coupled interconnects. In conclusion, a summary of the key points of the physical structure and AC coupled interconnects is presented.

Buried Bump Technology

In order to operate a CMOS chip, DC power and ground voltages must be supplied. With previous technology, the constraints for supplying direct paths from a substrate or PCB to a CMOS IC for DC signals have been in opposition to the constraints for coupling AC signals across the chip-substrate interface. To have numerous DC paths, physical connections must be established, but even the most aggressive connection methodologies introduce a gap between the chip and substrate in the tens of microns. However to implement capacitive coupling, the chip and substrate must be brought into close proximity (i.e. between 2 to 5 microns apart). A novel physical structure has been developed that allows both chip-to-chip communication via AC coupled interconnects as shown in Figure 1 and DC paths across the chip-substrate interface. The fabrication process of the physical structure is compatible with standard CMOS processing techniques.

A cross-section of the structure is shown in Figure 2. As a demonstration, the substrate has been fabricated from a silicon wafer. The structure consists of multiple ICs and a common substrate. Trenches are created in the substrate using bulk micromachining processes. Solder bump landing pads are then created in the substrate trenches. A routing layer is created on the substrate to allow DC voltages to be brought to the solder bumps (not shown in Figure 2) and to allow interconnection between ICs via the AC coupling elements. A portion of each AC coupling element is fabricated on the substrate surface wherever AC interconnections to an IC are desired. The VLSI chips can be created with any standard CMOS fabrication process. Pads for solder bumps should be fabricated on the top-level metal of the chips where DC connections are desired between the chip and the substrate. The corresponding portion of each coupling element should be fabricated on the chip surface where it is needed to AC couple signals to the substrate.

The trenches in this physical structure were designed to be a depth slightly less than the height of a reflowed solder bump. Using this structure, a bumped chip can be positioned over the substrate so that the solder bumps can be recessed into the trenches and corresponding AC coupling elements aligned. Once the solder bumps are bonded to the substrate, the chip and substrate are separated by a small gap (2 to 5 microns) and AC coupling can be achieved through corresponding coupling elements.

This technology has been implemented using silicon as the substrate. It was found that the standoff distance between the chip and substrate surfaces could be precisely controlled and was uniform across the chip to sub-micron scales.

This technique works well because solder balls are well controlled and uniform structures. The solder balls can be made as large as necessary to provide the required compliance. All the usual advantages of solder bump assembly, such as self-alignment, are still useful in this structure. The technique is extendible to other package materials, including ceramics and plastics.

Circuits for Capacitive Coupling

Various transceiver designs are appropriate for use in capacitively coupled systems. A basic schematic of a capacitvely coupled system is shown in Figure 3.

The series coupling capacitance produces a high pass filter. In addition, any significant parasitic capacitance at the output of the driver yields a low pass characteristic, thereby, producing at the minimum a second order bandpass response from the driver to the receiver. As a signal propagates through this band limited channel the signal will be altered differently by the high pass and low pass portions of the response. In the time domain, the high pass filtering passes the edges of the digital signal. The time rate change of the voltage signal (dV/dT) at the output of the driver is received as a pulse at the input of the receiver. The receiver sees positive pulses for rising edges and negative pulses for falling edges. The high pass response also produces a DC wander in the received signal. The low pass filtering that occurs due to the output impedance of the driver, the parasitic capacitance of the driver, and the parasitic capacitance of the coupling capacitor slows the edge rate of the transmitted signal. This reduction in dV/dT means that the amplitude of received signal is decreased. However, it also increases the duration of the received pulse.

Driver Requirements

For capacitvely coupled systems the driver requirements are very straightforward. A simple chain of inverters with adequate drive strength is usually sufficient. In the case of chip-to-chip communication across long substrates (typically used in multi-chip modules), the output impedance of the driver should be matched to the characteristic impedance of the substrate transmission medium. As in many output driver designs, any possible reduction in parasitic capacitance should be leveraged. In the measurements presented in this paper, the driver output capacitance was minimized by using ring shaped transistors. When compared to typical devices, where two transistors share the same drain, the reduction in capacitance is significant. The shared drain devices have almost 2.5x the drain capacitance of the equivalent width ring shaped device.

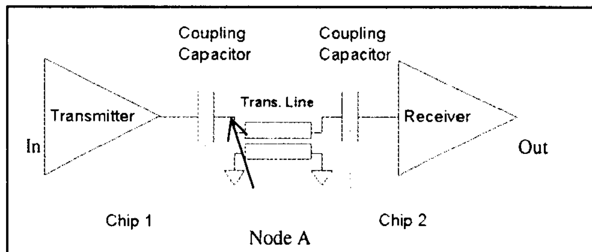

Figure 3 Capacitively coupled system

Receiver Requirements

The receiver requirements depend upon the details of the interconnecting medium and the expected signal degradation from driver to receiver. In addition, it is desired to maximize the data rate along the interconnection. The ability to work with non-return-to zero (NRZ) data patterns instead of return-to-zero (RZ) is desirable since NRZ data transmission yields twice the data rate of RZ data transmission.

A single-ended receiver designed by Kühn et al (Figure 4) is appropriate for short interconnect distances, or in distributed systems where receiver-side mismatch is acceptable [9]. At the input of the Kühn receiver is an inverter that is self-biased to the peak gain region of its transfer characteristic. Kühn describes the feedback mechanism used to bias the input stage as transmission gate feedback. However, the feedback transistors are actually diode connected and the operation is different from devices forming a transmission gate. These diode-connected devices have a dynamic input impedance. When the voltage across them is below their threshold voltage they have an extremely high input impedance. This allows the input impedance of the receiver to remain high for small input signals. It also limits the maximum swing between the receiver input and the output of its first stage. As the output signal of the first stage transitions out of phase with its input signal the diodes eventually turn on and limit the voltage difference. This is important for detecting small pulses with fast edges in a system using minimum sized coupling capacitors. The next stage easily amplifies this signal to on chip digital levels. Following this buffer is a latch that stores the last transition of the input, making the receiver compliant

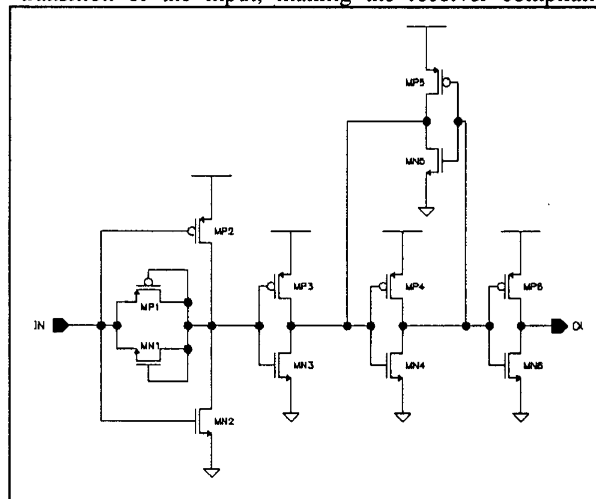

Figure 4 Single-ended modified Kühn receiver schematic for capacitively coupled interconnect

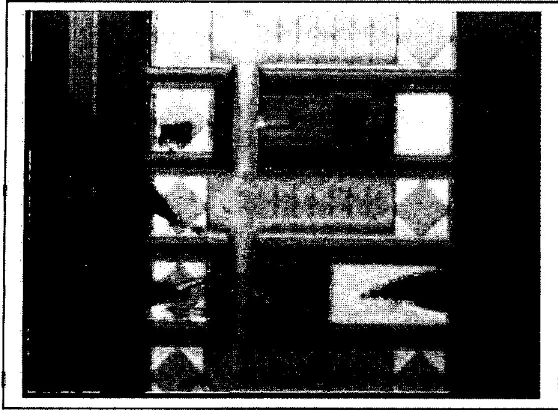

Figure 5 Die photo of CMOS IC with capacitively coupled interconnect experiments

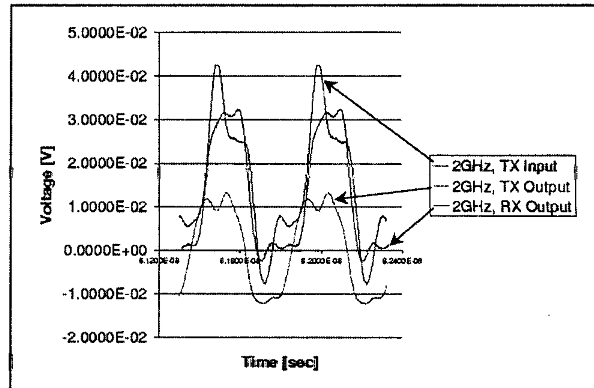

Figure 6 2GHz (4Gbps, NRZ data) capacitively coupled measured results

with NRZ data transmission. A buffer follows the latch.

A differential receiver architecture appropriate for use in capacitively coupled systems was designed by Gabara and Fischer [10]. Differential signaling is often desirable over single-ended signaling because of its improved noise immunity, its ability to interface between different circuit standards, and its ability to communication across large distances where maintaining a common reference is impossible. The operation of the circuit was explained by Gabara and Fischer and was demonstrated in a 0.5μm CMOS process at 800MHz [10].

Capacitive Coupling Measurements

Measurements were made on several integrated CMOS driver and receiver circuits specifically designed for communicating data across a capacitively coupled interface. The tested chips (Figure 5) were fabricated at MOSIS in the TSMC 0.35μm technology. Five chips, each 2mm x 2mm, were mounted into a single 64-pin DIP package for testing. Each chip had its own package pins for power and ground supply voltages

Driver circuits consisting of a 3-stage inverter chain were fabricated. Each driver was connected in series to an on-chip capacitor. HSpice simulations were performed to pick two sizes of capacitors – a small capacitor (75μm x 75μm) with a capacitance calculated to be 0.80pF and a large capacitor (150μm x 75μm) with a capacitance calculated to be 1.19pF. Two different receiver configurations were fabricated and tested. Each receiver circuit implemented the capacitive coupling receiver proposed by Kühn (Figure 4). One configuration of the receiver had the large capacitor connected in series to its input and the other configuration had the small capacitor connected in series with its input. The outputs of the transmitter capacitors and the inputs of the receiver capacitors were each connected to probe pads. This was done so that the outputs of the transmitter capacitors could be probed and a complete system could be created by wirebonding the output of a transmitter capacitor to the input of a receiver capacitor.

Two types of measurements were made on these test chips. First, characterization was performed on several driver/coupling capacitor pairs. With reference to Figure 3, the driver/coupling capacitor measurements were made at the points labeled "In" and "Node A". The input to the driver was a 3.3V peak-to-peak square wave, and frequencies were tested from 40MHz to 3.1GHz. After this, wirebonds were placed between the output of the series driver capacitors and the input of the series receiver capacitors. The bondwires took the place of the transmission line shown in Figure 3 and allowed a complete capacitively coupled driver/receiver system to be tested. For this experiment, the interconnect structure was constrained to being on-chip to avoid the substantial overhead of a solder bumping run.

During the driver characterization, it was found that the delay through the 3-stage inverting driver and 75μm × 75μm series capacitor was only 190ps at both 2.0GHz and 1.5GHz. The DC current drawn by the driver was 8mA at 2.4GHz, 5mA at 1.2GHz, 2mA at 600MHz, and less than 1mA at and below 75MHz. Most importantly, the edge rates at the output of the driver's series capacitor were measured to be 132ps at 2.4GHz and 110ps at 1.2GHz. As confirmed with simulation, the sharp edge rates at 2.4GHz will allow the on-chip capacitors to be reduced to 0.200pF (a 4× decrease in area) while maintaining sufficient current injection into the receivers for correct operation.

After the drivers were characterized, transmitters and receivers were connected to each other with bond wires.

Figure 6 shows the measured results from the sequence of transmitter, large coupling cap (output of transmitter), bond wire, large coupling capacitor (input of receiver), and receiver. The waveforms in the figure were measured at the transmitter input, at the bond wire, and at the receiver output. The input to the driver was a 3.3V, 2GHz square wave. For this configuration, the total delay through the system (transmitter, coupling capacitors, and receiver) was measured to be 212ps. Effects of impedance mismatch between the test equipment and the transmitter input were also seen. In spite of this mismatch, the receiver correctly recovered the input waveform. With NRZ data coding, the transmitter/receiver system recovered data correctly at an operating frequency of 4Gbit/sec.

The complete capacitively coupled system was also measured with the input to the driver as a 3.3V, 3GHz square wave. The resulting measured waveforms were sinusoidal in shape due to band-limiting effects in the measurement equipment and because the transistors were approaching their unity gain frequency. Even though simulation results predicted this behavior, the receivers correctly recovered the input signal. With NRZ data coding, the transmitter/receiver system recovered data at an operating frequency of 6Gbit/sec.

Capacitive Coupling Analysis

Considering the novel physical structure presented earlier along with the circuit discussions, the measurement results, and a few simple formulas for capacitors, several conclusions can be drawn about capacitive coupling.

For short interconnection lengths, a simple wire can replace the transmission line shown in Figure 3. In this case, the two series capacitors can be considered as a single equivalent capacitor. As confirmed with simulations, capacitances of 200fF allow sufficient signal to pass to the receiver for correct system operation. Such a capacitor would be roughly 150μm per side, but the area could be reduced further if the gap between the chip and substrate were to be filled with a dielectric.

For long connections, each capacitor is seen in series with the transmission line and the impedance of these elements must be considered. To avoid reflections on the transmission line, transmitter-side matching can be implemented, but to accomplish this matching, the magnitude of the impedance of the transmitter output in series with the capacitor must be equal to the transmission line impedance. If the transmission line is designed to have a 100Ω impedance and the transmitter is designed with a 50Ω output impedance, then the capacitor must also have an impedance of 50Ω. With current transistor technology (e.g. TSMC 0.35μm process), transistors can operate without observable band-limited effects at 2GHz. Using this frequency, a 2μm gap between the chip and substrate, and assuming an air dielectric, a parallel plate capacitor formed in the context of the presented physical structure must be 1500μm per side to be impedance matched!

The prospects for capacitively coupled interconnection improve as transistor technology improves. The current that can be passed through a capacitor is proportional to the time rate of change of the voltage across the capacitor. Therefore, communication via capacitive coupling relies on fast edge rates to transfer data across series capacitors and edge rates achievable with a three stage inverting driver will improve as the designs are fabricated in 0.25um and 0.18um technologies. Also, the unity gain frequency of transistors will continue to increase and thereby allow higher data rates to be achieved. As the operating frequency increases, the capacitors can be made smaller while still maintaining an impedance match.

Circuits for Inductive Coupling

As with capacitive coupling many transceiver topologies are appropriate for inductively coupled systems. A simple schematic of an inductively coupled system is shown in Figure 7. The two coupled coils act as a lossy transformer. Benefits from varying the turns ratio may be used to increase signal amplitude, or in the case of a distributed system assist with impedance matching. Much like the capacitively coupled interconnect the inductively coupled interconnect also has a band pass filter response that results from the lack of a DC connection and the parasitic capacitance of the inductors.

Driver Requirements

In chip to chip communications scenarios, where distributed effects can be neglected, a simple current mode driver can be used. Depending on system requirements a single ended driver may be adequate, but in some situations, a differential driver may be more suited. A current steering differential driver will help to minimize the noise injected on the power supply lines. In addition, it will also reduce transmitted power supply

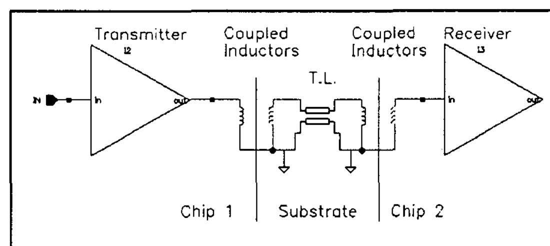

Figure 7 Inductively coupled system (long connections)

noise that would occur in a single mode driver. If the interconnect distance is long enough and distributed effects become significant, then it may be necessary to provide impedance matching on the output of the driver. If the communications channel is fairly narrow band then the impedance matching on the primary side can be provided by carefully designing the inductor elements and their associated parasitics.

Receiver Requirements
A low input impedance current mode receiver on the secondary side of the transformer will work well in both lumped and distributed systems. A current mode receiver with low input impedance will help to reduce the signal attenuation that would occur with voltage mode signaling because of the parasitic capacitance of the inductors and the high input impedance of a voltage mode receiver. In a systems where distributed effects must be considered the receiver should be designed to have an input impedance that can be easily matched to the transmission medium. In addition, since most digital processes do not provide good resistors, and since off chip resistors are out of the question for high-speed communications applications, a receiver architecture that provides low input impedance without additional termination is the best choice.

A differential current mode receiver designed by Ishibe et al (Figure 8) provides a solution for lumped and distributed systems [11]. The input impedance of the receiver is set by the transconductance of the input stage and can be set by adjusting device size and/or bias current. An important highlight of this receiver is its ability to provide almost constant input impedance in the presence of large input signals. This helps the receiver to maintain a match to the transmission medium even when the signal amplitude is large. The receiver uses shunt feedback [current mixing at the input and voltage sensing at the output] to stabilize its input impedance. By examining one side of the differential input, this feedback mechanism can be easily understood. When the current I-IN increases it forces the transistor MP2 to conduct more current. Since the gate voltage of MP2 is fixed by the bias on the gate of MP3 its source voltage increases in proportion the injected current. Because the gate voltage of MN2 is also fixed its source voltage must decreased by the same amount. Almost constant input impedance is achieved because it is defined by the parallel combination of the equivalent source resistance of MP2 and MN2. The source impedance of MP2 and MN2 will oscillate around the bias value as the injected current is modulated. The ability of this receiver to stabilize its input impedance makes it a good choice for any distributed system where impedance matching is needed. By incorporating a proportional to absolute temperature bias circuit [PTAT] the receiver could also be designed to compensate for temperature variations.

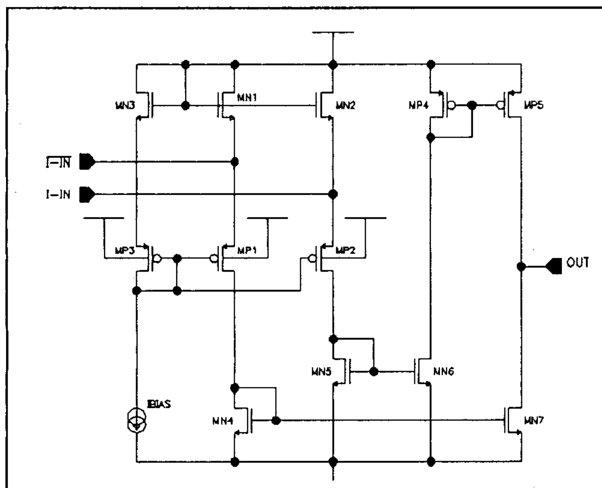

Figure 8 Differential Ishibe receiver schematic for inductively coupled interconnect

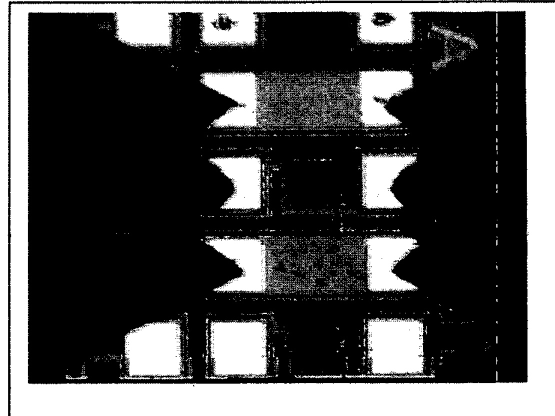

Figure 9 Die photo of coupled inductors

Inductive Coupling Measurements

An IC with stacked spiral inductor experiments was designed in TSMC 0.25μm technology and fabricated at MOSIS. S-Parameter measurements of the coupling between the stacked spiral inductors were made from 200MHz to 20GHz using an HP8510 Network Analyzer. A die photo of a set of stacked spiral inductors being measured is shown in Figure 9. The bottom inductor of the stack was designed in metal1 and the top spiral was designed in metal4. With this choice of metal levels, the spiral inductors were separated by almost 3μm – a gap that is achievable with the proposed physical structure presented earlier in this paper. The inductors were designed to have a high DC resistance (~50Ω) so that worst case measurements could be made.

Figure 10 shows S21 measurements made on two different chips across 50µm diameter, 10 turn, stacked spiral inductors. Even with large, resistive inductors, the transmission of signal through the coupled inductors was only attenuated by about 8dB.

Inductive Coupling Analysis

As with the analysis for capacitive coupling, several conclusions about inductive coupling can be drawn by considering the novel physical structure presented earlier along with the circuit discussions, the measurement results, and a few simple formulas for inductors.

Based on the measurements presented in Figure 10, there is an 8dB loss through a single set of stacked, coupled inductors. To form a complete inductively coupled system, the output of the transmitter would pass through two sets of coupled inductors and would experience a 16dB loss. In a 100Ω system with a 2.5V power supply, more than 2mA of current could be transmitted from the driver to the receiver. To save power, the receiver could be designed to use much less than a milliamp of current. For example, a differential receiver that requires 200µA ppk current would require the driver to supply a 125mV swing into a 100Ω differential impedance.

Discussion

The density of I/O that can be achieved with coupled elements of this size is incredible. With reference to the physical structure presented earlier, if a unit cell of 12 inductive elements surrounding the perimeter of the trench is stepped across a 9mm × 9mm die (assuming 75µm diameter inductors on a 100µm pitch) then 6075 AC interconnects and 506 power and ground pins could be fabricated on the die surface. For high-performance applications in the year 2011, this die size is far smaller than the die sizes predicted by [12], but the achievable I/O density is greater than the I/O density requirements. Thus inductive coupling may enable a current technological barrier to be overcome.

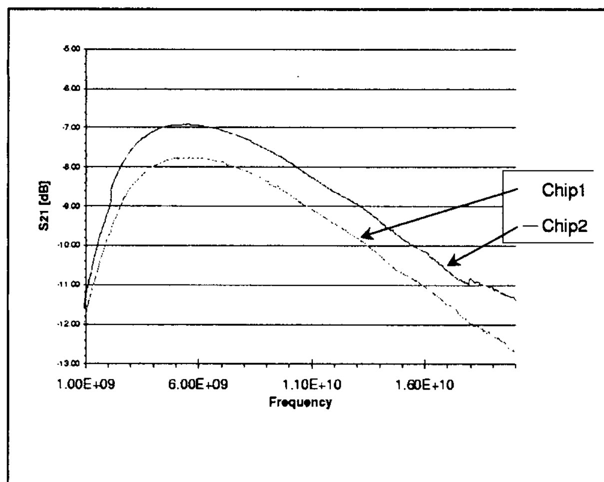

Figure 10 S-parameter measurements (S21) for 50µm diameter stacked, spiral inductors

Furthermore, achieving these high densities requires little change in the current manufacturing flows, apart from the construction of the solder bump trenches. For capacitively coupled interconnect the capacitor dielectric is simply the normal overglass in series with the expected air gap. A similar structure is used for inductively coupled structures. Large solder bumps can be used for stress relief if need be. If an underfil is desired, we anticipate that it can be incorporated in the bump trenches.

The circuit topologies used for transceivers are different from conventional ones, as discussed above. Further optimization is anticipated.

In the frequency domain, AC coupled interconnect can be thought of as a band-pass circuit. The acceptable pass band generally covers a decade of frequency. The cut-off frequencies can be manipulated by changing details of the physical structure.

Obviously, any package that could support over 5,000 signal I/O will require high density wiring. However, the package wiring does not have to match the pitch of the IC wiring, even in the inductive coupled structures.

Though the feasibility demonstrations were performed using silicon structures (for ease of fabrication in an R&D environment), there is no reason that this approach can not be used in ceramic or plastic packaging. For example, holes could be punched in the top layer of a ceramic package, when in green tape form, to later permit solder ball attachment. One advantage of inductive coupling is that it reduces the co-planarity requirements over capacitive coupling; potentially making even laminates, with their relatively rough surfaces, feasible.

So far, no fundamental barrier to exploitation has presented itself.

Conclusions

A new approach to building very high density, high bandwidth and low-power digital chip-to-package connections has been developed, in which digital signals are carried using contactless series capacitance and inductance structures. By being contactless, high densities can be achieved without the mechanical, compliance and rework complexities typically associated with fine pitch interconnects. Solder bumped DC power

and ground connections can be used, while keeping the opposing half capacitors or inductor spirals in close proximity, by burying the solder bumps in trenches in the package. Interconnect pitches down to 75μm are possible At a pitch of 100μm, for example, 6075 signal I/O and 506 power & grounds in a 9 x 9 mm die. New transceiver topologies are desired to best exploit this technology. Receivers are best designed to be NRZ tolerant, and current mode circuits have advantages in the inductively coupled structures. Experiments have been performed to demonstrate the feasibility of both the buried solder bump concept and the overall interconnect circuit structures.

Acknowledgements

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