Monolithic Copper Integrated Circuitry supporting Multi-layer MEMS

SRC Cu Design Challenge

Phase-I Report

North Carolina State University

December 31, 1999

Bruce Duewer, Alan Glaser, David Nackashi, John Wilson,

David Winick (lead)

Dept. of Electrical and Computer Engr.

1010 Main Campus Drive, 438 EGRC Building

NCSU Box 7914, Centennial Campus

Raleigh, NC 27695-7914

Abstract

In this Phase-I entry we explore post-processing of the UMC Cu chip for distributed micro-systems design. Microsystems technology involves the creation of sensors and/or actuators integrated with control circuitry. This is also sometimes termed systems-on-a-chip ("SoC"). Currently available processes for such systems either limit the designer to very simple mechanics (e.g., iMEMS[i]), or to a lateral separation of the mechanical and circuitry planes (e.g., MEMS-in-a-Trench[ii], or SmartMUMPs[iii]). For advanced micro-systems applications, such as distributed control of "smart" sensor/actuator arrays, better integration is necessary. The eventual availability of the UMC Copper process, in combination with our development of a post-process release sequence, will make viable the design of such systems. Higher melting points, electromigration resistance, Damascene etch barriers and CMP planarity make Copper attractive for post-processing. Our chip development efforts include design of a post-process sequence, structures for process monitoring of that sequence, structures for determination of copper thin-film mechanical properties, and a state-of-the-art micro-system array that will demonstrate feasibility of distributed sense and control in the UMC Cu process.

1. Executive Summary

The objective of this entry is to further the functionality and appeal of the UMC Cu process. With post-process extensions, we intend to demonstrate that the Copper process capabilities may be extended into the domain of elaborate microsystems design. In this report we describe our design of a chip that will be pivotal to this objective. The chip includes three separate components that each serve a different purpose. In order to allow development of rules and recommendations for future microsystem design in this process, we must know the mechanical characteristics of each of the thin films involved; consequently, the first set of components will be a series of characterization structures, both active and passive, to extract parameters such as latent stress, Young's modulus, and Poisson's ratio. The second set of structures are for process monitoring. Due to the unavailability of some process information and to deviations from our analytical models which may occur under laboratory conditions, we will need to include some structures that will aid us in tuning our release process. Concerns, such as over-/under-etch, material selectivity, and stiction, will be monitored optically under metrology microscopes. Finally, a robust and innovative micromirror array microsystem, based on process cornering done in this report, will prove feasibility of complicated microsystems implementation. Monolithic implementations such as this, prior to now, were only possible through costly custom per-project fabrication. And in this respect, UMC Cu may potentially fulfill three primary objectives of the MEMS community: lower cost, lower development time, and smarter devices.

Our approach, as you will see, is quite different from typical VLSI design. Given the task of process development, as well as component and system design, the majority of our layout is full-custom, with non-critical components taken from standard libraries. We develop our own device library for high voltage analog devices that will be used to drive the electrostatic mechanism of the MEMS. And we, likewise, custom design the circuitry necessary for analog-to-digital converters, self-calibrating position measurement current sources, and MEMS elements. The distributed control microsystem design is done at the behavioral level, and is geared to be as general purpose as possible. The array is designed with complete a micro-controller, to interface with an instruction ROM and other standard I/O devices to make system insertion widely configurable. Outside of the calibration circuit, the system does not need to be extremely fast (we are limited by mechanical speeds only approaching a few hundred kHz), so simple synchronous registered logic, with sequential state machines and lookups for micro-code, comprises the bulk of the control system. The variable instruction timing that results from the micro-code is inconsequential due to the expected relative speed of the Cu circuitry.

2. Background

In this section we present some technology definitions with respect to our objectives and foreseen advantages to the Copper process.

Microsystems

Systems on a chip, that involve collection, processing, and acting on non-electrical data are termed *microsystems*. These involve energy transductions via sensors and actuators, from and to, respectively, other energy domains. Microsystems are currently very difficult to design for three reasons. First, comprehensive design tools do not as yet exist. Second, fabrication methods must typically be modified and optimized for each new device design. Third, the designer must not only describe the interconnection of devices, but also understand the effects of fabrication and the basic transduction principles in order to design at the device-level, as well. And finally, the designer must take into consideration the operational environment and packaging requirements to maintain the integrity and sensitivity relative to undesirable energy transductions.

MEMS, or micro-electromechanical systems (sometimes referred to as *micromachines*), is a sub-category of micro-systems, in which the energy domains are electrical and mechanical. Available energy transduction principles include capacitance modulation, piezoresistivity, elastoelectric effect, photoelectric effect, and photovoltaic effect.

Multi-layer MEMS

Micromachining involves the release of microfabricated material structures (usually on a wafer) by selectively etching a chosen *sacrificial* material from the device. Micromachining comes in three flavors, according to the location of the sacrificial material: bulk, thin film, and free component. Each is explained below.

Bulk micromachining involves etching away (anisotropically) trenches in the crystalline substrate, and results in thin-film structures (generally membranes) that can freely deform into or out from the plane of the wafer, when exposed to mechanical stresses. Likewise, free component micromachining, such as LIGA, etches away the boundary between surface films and substrate. But does so to completion: the materials that make up the MEMS component are completely separated from the substrate, allowing the creation of a parts (generally relatively thick) that can be removed and undergo subsequent micro-assembly into a multi-part mechanical system. Both bulk and free component micromachining are inherently single-layer MEMS processes, as only a single lithography step is needed to pattern the mechanical layer. Nevertheless, it is possible to use these in combination with multi-layer techniques. It is also possible to combine the two by performing a *timed-etch* release of the sacrificial material.

In thin film micromachining, the chosen sacrificial material is one of the thin film materials. These materials are interspersed with layers of mechanical and electrical materials, such that when released, separations are created between mechanical regions of the device. Thin film micromachining can be further categorized according to the number of thin film layers. As the number of interspersed layers is increased, so too is the possible complexity of the resulting mechanical system. With only one (1) mechanical layer, designers limited to building deformable beams and membranes (just as in bulk micromachining). With two (2) mechanical layers, fixed hinges and axles can be created. Three (3) layers allows for free (horizontal or vertical) translation of those two-layer devices (e.g., for a crank-arm). And four (4) mechanical layers allows for translatable gears on shared axles.

Monolithic MEMS-VLSI

There are currently only a few fabrication services available that claim capability to construct surface micro-mechanics and electrical devices together within a single package. Among them are MCNC's SmartMUMPs, Carnegie Mellon University's VLSI release, Analog Devices' iMEMS, and Sandia National Lab's M^3S (Modular Monolithic MEMS) technology.

Analog Devices' iMEMS was the first to offer to the public a MEMS technology that supported both the mechanical components and the circuitry to control them. This technology was an extension to a standard n-well BiMOS process, in which a relatively thick *mechanical* polysilicon beam layer and accompanying *sacrificial* oxide spacer layer is constructed, after the electronics layers and before the metalization. All of the underlying wells and device channel profiles are designed with thermal budgets to support the processing necessarily involved in the mechanical layers. The iMEMS process is well suited for accelerometer designs, in which complex control systems can be located close to the mechanics. Nevertheless, this process does not eliminate the parasitics problem, as connections between the electronics and mechanics is only through N+ diffusion; metal is not allowed within the sensor area. Furthermore, applications and wiring density are limited by the availability of only a single metal interconnect layer and a single polysilicon mechanical layer.

Both SmartMUMPs and the M^3S technology extend this range of potential applications by giving the designer two or more mechanical polysilicon layers to work with. However, designs in these technologies are restricted to a severe lateral separation of the mechanics from electronic devices. Devices must be separated from the mechanics by either the walls of a substrate trench or by the solder bumping which connects two separate substrates.

CMU's technology research[iv] in this area involves a sequence of maskless dry etching steps to post-process the release of laminated beam structures from a conventional CMOS process. The result is a mechanical structure that is both physically and electrically close to the electronics. And fabrication of this structure does not impose the severe limit in wiring layers as was seen in the previous technologies. Unfortunately, this limit is instead shifted to the mechanics: this technology has returned us to only a single mechanical layer.

The ability to construct microsystems in electro-deposited Copper technology would offer several advantages over

the competing microsystem technologies. In addition to the electronic component advantages, we would also have multi-layer micro-electro-mechanical systems with the following:

- Multi-layer metal interconnect routing is available for advanced switching, RF, or microwave applications – not to mention, control circuitry for which one metal layer just isn't enough.
- MEMS arrays are not limited to perimeter-based control schemes, as bond wires or solder balls are not necessary for each and every connection to the controller.
- Packaging does not necessarily need to be concerned with separate regions of the chip, as environmental isolation is a function of the technology.

Electromigration resistance

For sensors, this means higher precision and larger operating ranges. For mechanics, faster heat dissipation.

High melting points

High electromigration resistance translates directly to high melting points. Aluminum melts at the high temperatures associated with anneal of mechanical polysilicon. Copper can withstand much higher temperatures than Aluminum, and in fact undergoes an anneal itself of near 300 C. Mechanical polysilicon anneals are typically around 1100 C, but have been successful down near 950 C. One of the goals of this project is to find a happy medium amongst these temperature boundaries if mechanical anneals become necessary.

Damascene etch barriers and Low-K dielectric

FSG dielectric can be selectively and isotropically etched in buffered HF, and SiN barrier layers can likewise be selectively etched in a bath of phosphoric acid. The combination of these etch step pairs present us the opportunity to control the depth to which we release our thin film stack--without resorting to timed etches. Thus a designer in this Monolithic Copper MEMS-VLSI Process will be able to arbitrarily trade off mechanical complexity for electrical wiring density in a particular cell. Furthermore, cells can be isolated from isotropic etch by using Copper shields or cap-layer structures.

CMP planarity

A planarized top layer makes it easier for post-processing lithography. Assuming no problems are found with inter-fab contamination due to the prior processing, fabrication of the MEMS layers on top might continue as if the VLSI layers were not there, as if it were a new substrate. And for cases of releasing the Copper layers, the planarity reduces the chances of the mechanics being affected by surface stresses in conformal shapes.

Non-epi substrate and Trench Isolation

These allow an easier design of high-voltage devices, or devices which require large spacing due to dopant migrations during post-processing. Electrostatic actuation is common in MEMS, and high voltage devices are required to generate the electrostatic drive potentials.

Other Possible Uses

In addition to the discussed MEMS applications, Copper is known to be a useful electrode material. A Copper-based microsystem process may also find application in biomedical areas[v].

3. Approach

There are two possible approaches to adding MEMS capability to the Copper chip. The first, is to deposit the

MEMS layers on top of the Copper layers. We started with a brief exploration of the this approach. In order for this to work, results from the UMC Cu process, preferably in un-diced wafer form, would subsequently be submitted to a MEMS fabrication house such as Cronos (formerly part of MCNC). The wafer would then undergo a series of modified MEMS process steps that would be compatible with the UMC Cu layers. The planarity of the Copper process, in conjunction with the higher thermal budgets relative to Aluminum, initially seemed favorable towards this approach. Nevertheless, there are several challenges we just cannot find answers to. The anneal budgets are still not close enough to the temperatures needed for mechanical polysilicon. A via interface between the two processes posed a major challenge, as Copper is a deep level impurity in silicon; Copper diffuses through SiO_2 in the presence of an electric field. The thermal coefficient of expansion of Copper is well above the other materials (bulk Cu is near 16.5e-6/C, compared to bulk Si of 4.1e-6/C) we would be working with, thus raising the likelihood of fractures. And we do not have enough information on the UMC Cu transistor wells and channels to extrapolate a dopant profile that would result from further anneals.

The second approach, which we go on to describe in the rest of this report, involves use of the Copper layers as mechanical, and the dielectric as sacrificial (in HF). While thermal coefficient differentials may result in some latent stress in the materials, an electro-deposited film is typically expected to be very low-stress, which is ideal for mechanical release. This approach will require fewer fabrication capabilities (we can perform a release in our own solid state laboratory), and will not require an entire wafer –only a chip.

Post-Damascene Supplemental Process Description

The process of releasing the micro-electromechanical structures designed in the copper process requires the removal of nine levels of sacrificial material. Each level is a deposited thin film of either polysilicon glass or silicon nitride. The figure below illustrates the process stackup along with a naming convention for identifying each of the copper, silicon dioxide and nitride layers. The removal of all silicon dioxide and silicon nitride levels down to and including Nitride 3 is required to fully release three mechanical copper levels of metal: M6, M5 and M4.

The etchants for the release of the copper structures were selected primarily on the basis of controllability and selectivity. Because the release process is fully manual, the etchant used for the removal of each layer must react at a rate slow enough to allow for a margin of error when dipping and removing the samples. In addition, the etchant is expected to attack the four sides of the sample. A slower, more controllable etchant will allow time to completely remove the targeted sacrificial layer without substantial removal of material from the sides of the sample. A highly selective etchant is also desirable to minimize the dissolution of copper or other non-targeted layers during the release process. In addition, a highly selective etchant increases controllability of the release process by slowing substantially once the targeted layer is removed. For example, the second step in the release process is to remove the top layer of silicon dioxide, SiO_2 Cap, from the sample. An etchant which attacks silicon dioxide at a much faster rate than silicon nitride will essentially "stop"once that top layer is fully removed. The same is true when removing the next layer, Nitride 6. An etchant which is highly selective towards nitride will slow substantially once the Nitride 6 layer is fully removed.

Removing the sacrificial material layer by layer is highly advantageous. The ability to stop the release process on any level allows the analysis of etch rates for each material, but most importantly, the analysis of each copper metal layer once released. Admittedly, the exact stress profile of each layer of copper is unknown. To calculate and eventually compensate for such deviations in the process, test structures will be placed within each level of metal designed for release. This includes the top metals, Metal 4 through Metal 6. These test structures are designed to bend in response to stress in any of the three spatial dimensions. The displacement of each structure can then be measured optically and an inherent stress profile for each level of metal can be calculated. Because the stress of one layer of copper can greatly affect the displacement of another layer of copper, the partial release capability described above is an important component to the release process.

Two primary etchants are under investigation for the removal of the silicon dioxide and the silicon nitride layers. Typically, hydrofluoric acid (HF) is used to remove silicon dioxide. In most micromachining release processes, the concentration is kept quite high. The speed that HF etches silicon dioxide is directly proportional to the concentration of the acid, i.e.., the stronger the concentration of HF, the faster the etch rate. Since it is generally desirable to remove all silicon dioxide from MEMS samples, the speed is only beneficial. In the case of an integrated MEMS-VLSI sample, it is NOT desirable to remove all silicon dioxide. As stated above, etchants will attack the sides of the samples during the release process. In order to prevent substantial removal of insulating SiO2 from the lower VLSI layers via the sides, a lower concentration of HF will be used for release. The highest concentration of HF available is 49%, which etches silicon dioxide at a rate of up to 36k angstroms per minute[vi]. By diluting the concentration down to a 10:1 ratio of deionized water to HF, this rate drops to 4.7k angstroms per minute. This 10:1 ratio will be the first etchant used to remove the silicon dioxide. If needed, the concentration can be lowered even further to slow down the process. All HF etching can be performed in a standard wet bench at room temperature.

To etch the silicon nitride layers, phosphoric acid is currently under investigation. Typically, an 85% concentration is used at a temperature of 160 degrees Fahrenheit. A reflux system will be used to return water to the diluted acid mixture. This will help maintain a constant concentration throughout the release. Etch rates on the order of 10nm per minute are expected in these conditions. An important factor in this process step is the complete removal of the previous silicon dioxide layer. "Hot" phosphoric acid is highly selective to nitrides versus silicon dioxides, therefore, any oxides left in the previous release will mask the nitride etch causing columns of nitride and other desirable effects. An overetch will be calculated to account for this problem occurring from incomplete etching due to oxide thickness variations and other sources.

Below is a candidate recipe for the release of the first four layers of Copper.

Step #0 - *Sample Preparation* - Cleaning

Wash the sample first with acetone, then with methanol. Place on a hot plate to dry for 10 minutes. The methanol will remove any residue left from the acetone rinse.

Step #1 - *Nitride Etch* - Remove the Nitride Cap

[redacted] layer of nitride will be remove with a timed wet etch using hot phosphoric acid (85%).
Time:
Temp: room T
Etch Stop: Oxide Cap

Step #2 - *Oxide Etch* - Remove Oxide Cap

[redacted] layer of silicon oxide will be removed with a timed wet etch user hydrofluoric acid (49%) at room temperature.
Time: 7.3 seconds
Temp: room T
Etch Stop: Nitride 6

Step #3 - *Nitride Etch* - Remove the Nitride 6 Layer

[redacted] layer of nitride will be removed with a timed wet etch using hot phosphoric acid (85%).
Time:
Temp: room T
Etch Stop: SiO2 6

Step #4 - *Oxide Etch* - Remove the SiO2 6 Layer

[redacted] layer of silicon oxide will be removed with a timed wet etch user hydrofluoric acid (49%) at room temperature. This releases the Metal 6 Layer.
Time: 31.2 seconds
Temp: room T
Etch Stop: Nitride 5

Step #5 - *Nitride Etch* - Remove the Nitride 5 Layer

[redacted] layer of nitride will be removed with a timed wet etch using hot phosphoric acid (85%).
Time:
Temp: room T
Etch Stop: SiO2 5

Step #6 - *Oxide Etch* - Remove the SiO2 5 Layer

[redacted] layer of silicon oxide will be removed with a timed wet etch user hydrofluoric acid (49%) at room temperature. This releases the Metal 5 layer.
Time: 31.2 seconds
Temp: room T
Etch Stop: Nitride 4

Step #7 - *Nitride Etch* - Remove the Nitride 4 Layer

[redacted] layer of nitride will be removed with a timed wet etch using hot phosphoric acid (85%). Time:
Temp: room T
Etch Stop: SiO2 4

Step #8 - *Oxide Etch* - Remove the SiO2 4 Layer

[redacted] layer of silicon oxide will be removed with a timed wet etch user hydrofluoric acid (49%) at room temperature. This releases the Metal 4 layer
Time: 17.4 seconds
Temp: room T
Etch Stop: Nitride 3

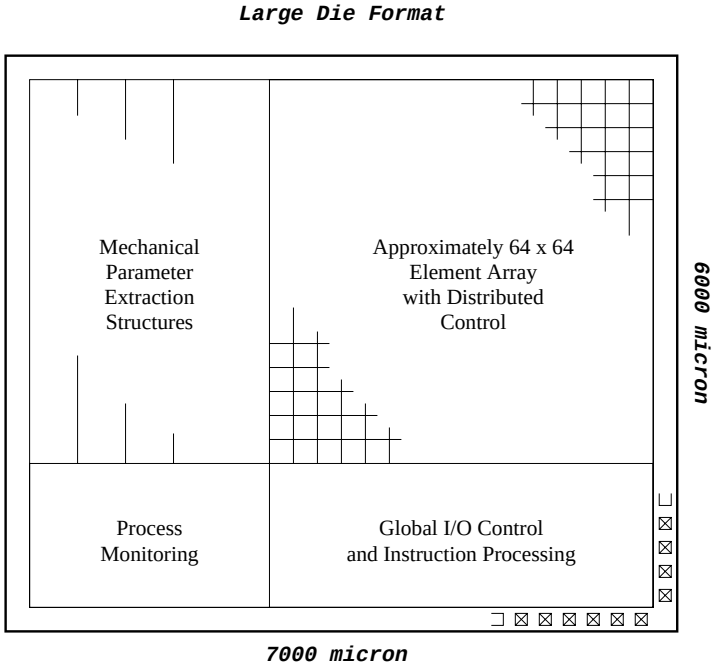
Step #9 - *Nitride Etch* - Remove the Nitride 3 Layer

[redacted] layer of nitride will be removed with a timed wet etch using hot phosphoric acid (85%). Time:
Temp: room T
Etch Stop: SiO2 3

Step #10 - *Oxide Etch* - Remove the SiO2 3 Layer

[redacted] layer of silicon oxide will be removed with a timed wet etch user hydrofluoric acid (49%) at room temperature. This releases the Metal 3 layer
Time: 17.4 seconds
Temp: room T
Etch Stop: Nitride 2

Cu-MEMS Chip Floorplan



Characterization Devices

Standard mechanical layer testcells will take up a significant amount of space on the chip. Unfortunately, they are necessary. And as the available space will not be enough for a complete set of characterization devices, we will have to layout carefully, fitting in as many as possible. Planned devices to be included are (organized according to parameter):

- For lateral yield stress: spring degradation of lateral comb actuators
- For Young's modulus: lateral resonators[vii]
- For inherent stress measurement: Guckel rings[viii] (tensile), doubly-clamped beams[ix] (compressive)
- For vertical gradient stress: Archimedes' spiral

Piston Micro-mirror Array Micro-system

Italicized constants used throughout this section:

a address bits (=8)
g general purpose i/o bits (=8)
s status bus output bits (=8)
i instruction opcode bits (=4)
c instruction conditional bits (=4)
d instruction data bits (=8)
p phase level bits (=8)
q add'l bits for error compensation (4 to 8, depending on space for D2A)
n bits to address row or column (n=d, so 8 per, resulting in a 256x256 array size limit)
N number of micromirrors per row or column ($N=2^n$)
P number of phase registers ($P=2^d$)

System Description:

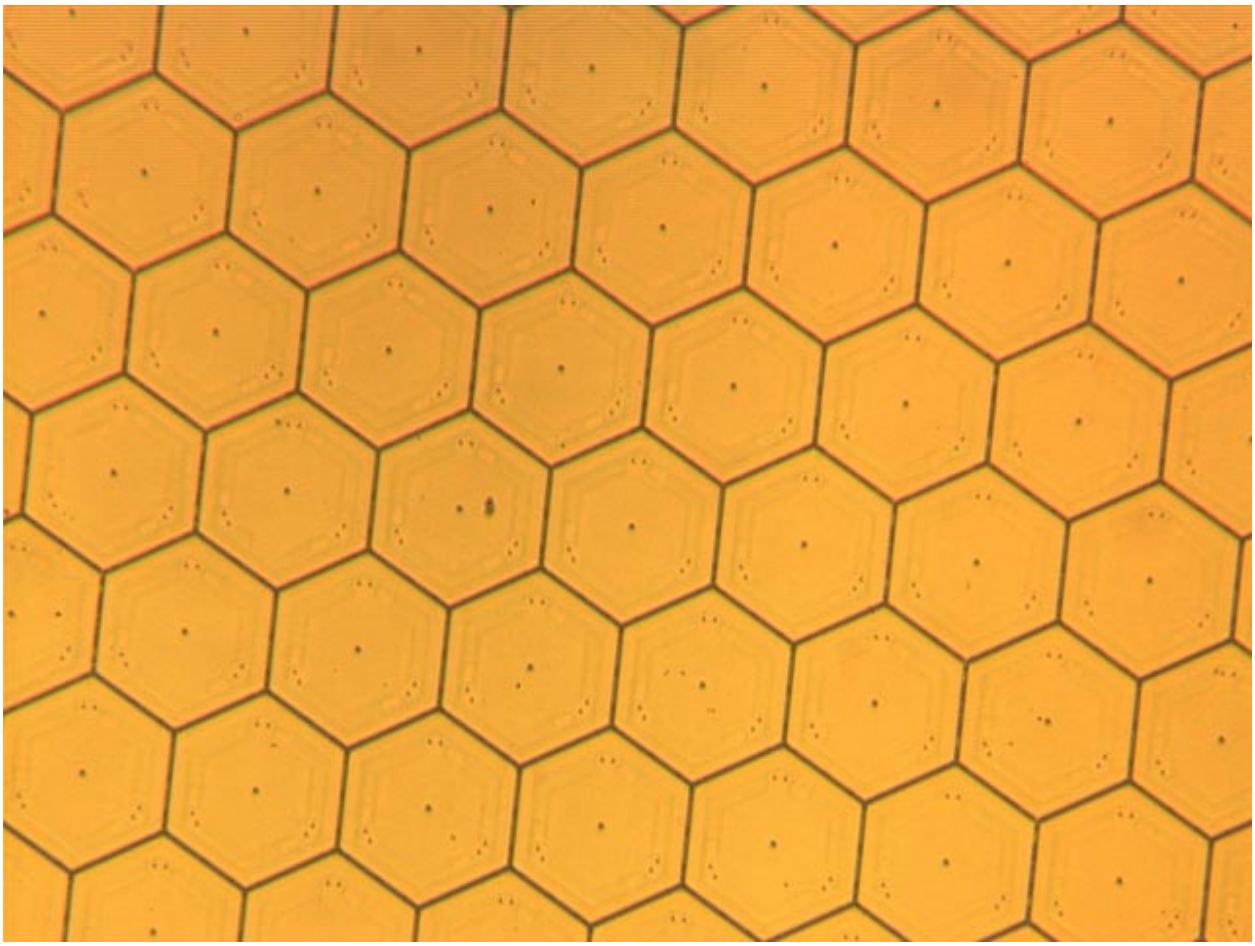
The described method of modulating an analog drive voltage based on measurements relative to other elements in an array is uniquely applicable to large arrays of small MEMS cells. It can not only be applied as it is here, to high-precision vertical positioning of mirrors (relative to a master mirror, which is itself measured optically relative to a system reference). In our demonstrator, we are using a distributed control scheme to correct for any mechanical errors that may be due to thin film discontinuities, transduction nonlinearities, lithography limits, or uncontrollable static charges. Extending robustness to any system design, the "master" device is not specified *a priori*; each element is capable of both "master" and "slave" operations. Because of this, our method of microsystem array control also has application in cases where elements can be controlled relative to any of their neighbors, rather than a single array master element.

This demonstrator architecture will surpass state-of-the-art in optical modulator technology. 2-dimensional modulators such as this are used in applications ranging from adaptive optics, to optical computing, to video display projection. State-of-the-art for 2-dimensional analog optical modulator systems on the market today are in liquid crystal technology (e.g., Meadowlark Optics' Hex127):

- liquid crystal variable retarders (for linear polarized light source)
- either amplitude or phase modulation to one optical wave
- 1.0 mm minimum pixel dimensions
- 127 maximum element count
- 12-bit controller resolution

Our modulator array will be capable of controlling an optical wavefront phase to at least this element count and resolution. And it will do so without requiring polarized light, and without a one-wavefront phase limit. The pixel dimensions are expected to be at least an order of magnitude smaller. Furthermore, we will add binary amplitude control to the system, along with the phase control; individual mirrors can be "turned off", directing light away from the system by tilting them to one side. Our array will have the following characteristics:

- Programmability objective for 256 phase levels. But greater than 8-bit control is necessary in order to compensate for errors, including the nonlinear voltage-to-displacement function in these MEMS micromirror devices. This will define the size of the D2A that will be placed in each cell, but it is expected to be 12- to 16-bits.
- Mirrors are capable of both vertical and tilt movements. Vertical movement is precise; tilt is on/off. This allows a user to implement both phase and intensity masks within a single modulator stage.
- Capacitive sense of mirror positions relative to neighbors (vertical placement), and automatic correction of each individual mirror, using localized control.
- Row- and column-enable addressibility of every movement operation, so any number of individual elements can be moved simultaneously to a new phase or a stored drive voltage.
- Calibration of any chosen "master" against external system inputs.
- Calibration of any chosen elements against any chosen "master".



We have already demonstrated, in polysilicon, the resolution advantages possible with MEMS. Above is the micrograph of a prior array design that we completed in order to demonstrate MEMS-based optical modulation using Sandia National Lab's SUMMiT VI process and in-house metalization. While MEMS holds advantages over competing technologies in this application, control systems currently must be off-chip; we have consequently found severe wiring limitations imposed are by available MEMS processes. Other researchers have also found these limitations in layout of micromirror arrays[x]. *Our design, described below, intends to leverage the Copper process to possibly demonstrate the first implementation of multi-layer MEMS that is monolithic and vertically integrated with a complete control system: a "microsystem", able to sense and respond both autonomously and under external control.*

Note also that our element and array control scheme is designed to accommodate multiple element designs. As the Copper films are as yet uncharacterized mechanically, we will layout several mechanical designs to fit within the array. As a result, we will have a greater chance of obtaining an ideally operable design, while at the same time not diminishing any functionality of the array (Should any of these devices fail, this would be detectable, as described below).

Element Mechanical Elevation

This design dictates that we release three Copper layers for the mechanics. That leaves the lower three layers for electronics. A process recipe for this release is described elsewhere in this document.

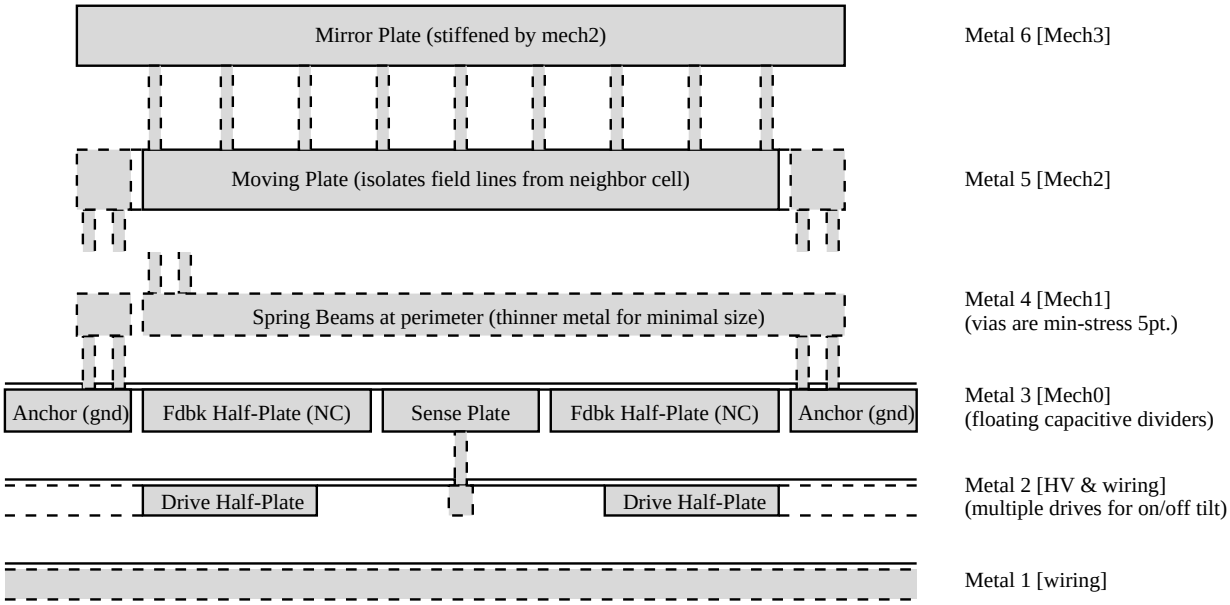
The vertical position of an element is controlled by voltage potential placed across the air-gap between Metal 5 [Mech2] and Metal 3 [Mech0]. As the metal on the moving plate is connected to Analog Gnd, and the non-

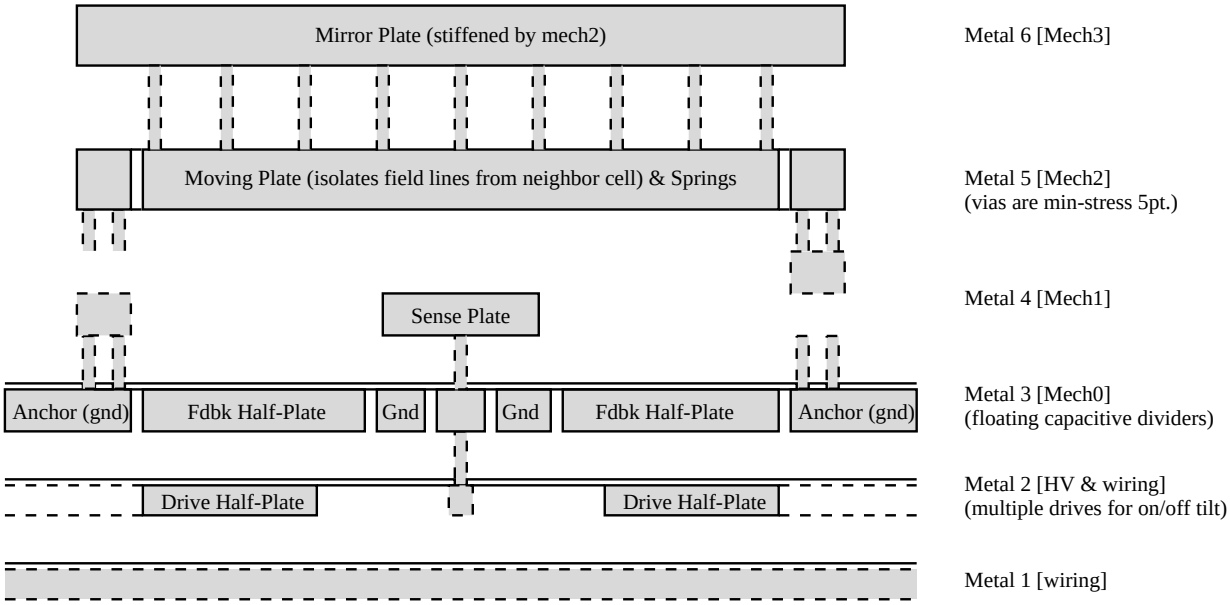
moving feedback plates are electrically floating (acting as capacitive dividers), the vertical position is a function of the analog voltage placed on the drive plates in Metal 2.

Normally, when the element is enabled, both of the drive plates ("half-plates") carry the same voltage. Tilting of the element is performed to "disable" the cell. When the element is disabled, the potential on the second drive plate is taken from an external power supply (see pinout), rather than the local D2A.

The electronic control system sits directly beneath each mechanical element. This process eliminates the need to laterally separate mechanical from electrical components.

- Square mirror elements cover entire cell area.
- Upper three metal layers are released (and therefore mechanical), leaving Nitride stop over Metal 3.
- Metal 6 (Mech3) is used for the mirror plate, and is stiffened by an array of vias to moving plate.
- Metal 5 (Mech2) is used for the moving plate. Square plate is smaller than Mirror plate, to help isolate field lines from neighboring cells; and connects to springs via tabs at the perimeter.
- Metal 4 (Mech 1) is used for the springs since it is the thinnest of the released metals (therefore lower voltage and smaller cell size). If the Phase-2 layout proves this not to be a limiting factor, we may decide to move the springs up to Metal 5 and use this layer for an improved sense plate design, thus also improving the device throw. Springs are straight rectangular beams, and connected at either end using 5-point via arrays, to minimize possibility of unusual stress characteristics, and to maximize likelihood of successful release.
- Metal 3 (Mech 0) is used for the anchors to the piston springs, which consist of Copper that is buried beneath the Nitride stop, and to prevent accidental over-etch from affecting structural integrity. This layer is also used for the electrically floating capacitive divider plates, and for the sensor plate.
- Metal 2 is used for high-voltage drive plates, two per piston cell; otherwise, both Metal 1 and Metal 2 can be used for wiring.





Input / Output Pads:

- Digital Power & Gnd (*??? pair* count)
- Analog Drive Voltage & Gnd (*??? pair* count)
- Calibration Current Level (analog input *pair*)
- Disable Voltage Level (analog input)
- Instruction Clock (input; can be adjusted to match resulting mechanical characteristics)

- Calibration Clock (input; can be adjusted to get good calibration data)
- Reset (active-low input)
- Instruction lines (*i*-bits input)
- Data lines (*d*-bits input)
- Address lines (8-bits, for connection to a 256-word program ROM)
- Write Enable (4-bits; to designate cycles that send output on GPIO lines instead of reading)
  0xxx= Result of Fetch instruction
  1001= Underflow error as result of a Calibrate instruction
  1010= Overflow error as result of a Calibration instruction
  1100= Invalid instruction
  1111= Still not calibrated (ORed result of every selected element; signals ext. logic to mask instruction to *Pause* and wait)
- Status lines (output; *s*-bits)
- General Purpose I/O lines (input/output; to control large ROMs, to set LEDs, or to input system calibration status)
- Master charge current (analog output *pair*)

Instruction Set Architecture (*i, c,* and *d* lines):

- *Pause*

0000 0000	xxxx xxxx

Note: A *Pause* does nothing, including preventing the PC from being incremented! (which differs from a *NOP*) This is to help us in the case where our calibrations take longer than the instruction cycle; if the WE=1111, then external logic can be used to mux in a Pause as the next fetched instruction, instead of what actually comes from the ROM.

- *Shift* in row/column select bits (4 bits each from data input pads)

???? ????	Row Bits	Column Bits

- *Load* to *MR* ("Master Row") or MC ("Master Column") registers from data field

???? ???	0= Row 1= Column	Row or Column Value

- *Set* "Master" to position in phase register P

???? ??	0x= set master only 10= also set non-selected elements 11= also set selected elements	Phase Register

- *Get (Pre-Increment/Decrement)* master cell position and store in phase register P

???? ??	00= No Change 01= Increment 10= Decrement	Phase Register

- Load Charge Current *Compensate* bits to master cell's calibration source circuit

???? ????	xxxx xxxx

- *Move* master cell to position (either low- or high-word) in data field

???? ???	0= Low Word 1= High Word	Drive Counter Partial Value (1 word)

- *Enable/disable* selected elements

???? ???	0= Disable 1= Enable	xxxx xxxx

- *Calibrate Selected / Non-selected* elements to "Master", storing calibration data locally at each enabled element
  Note that an element is "selected" if there's a 1 in its row/column in the RS/CS registers, and is "non-selected" if there's a 0.

???? ???	0=Non-Selected 1=Selected	xxxx xxxx

- Fetch *Status* Data from master cell to status lines

?????	Status Type (sent to lower 3 write enable lines) 000= calibration counter low-order word 001= calibration counter high-order word 010= drive voltage low-order word (*q*'s) 011= drive voltage high-order word (*p*'s) 10x= calibration current bits (and drive output pin from master's current source) 110= test even springs, and output cell state 111= test odd springs, and output cell state	xxxx xxxx

- Load GPIO *Mask* Register (reading from a bit set to output mode will return 0)

???? ????	Bit Modes

	0= Output (default) 1= Input

- Load *GPIO* Register (bits set to input mode will be unaffected)

???? ????	GPIO Output

- *Jump Conditional* on chosen GPIO register bit to address on data field.

???? ?	000= bit 0 001= bit 1 010= bit 2 ... 111= bit 7	EPROM Address

- *Jump Unconditional* to address on data field.

???? ????	EPROM Address

The cell state word (output to the status bus upon request), is of the following format:

bit7:	selected
bit6:	enabled
bit5:	calibration overflow / (not ready)
bit4:	direction
bits3-0:	spring 3-0 broken

Global Registers:

Elements are addressed for movement by two possible row and column schemes: (1) the global register "Master" (M) is decoded to address a single element, and (2) bit lines of the "Row Select" (RS) and "Column Select" (CS) registers are used to directly select multiple elements. The M register can be set from a value in the data field with a "Load" instruction. The CS and RS registers are loaded simultaneously, 4 bits each at a time, from the data lines with a "Shift" instruction. For cases where an element is selected by both the M and CS/RS registers, it will not be affected by a "Calibrate" instruction.

- Row Select bits (*N*)
- Column Select bits (*N*)
- Master Row (*n*)
- Master Column (*n*)

The phase registers are used to store the drive values of calibrated elements. It is up to the system designer to keep track of which elements correspond to which registers. The GPIO register can be used to extend addressibility to the instruction store (e.g., as chip select lines), but will not auto-increment from a PC overrun. In input mode, the GPIO bits can be used for conditional jump operations, to provide a means for system calibration. External latching of status bits into the GPIO would allow program execution conditionals on element states, as well as system states.

- Phase Registers (*P* of size $p+q$)
- General Purpose Register Mask (*g*)

- Program Counter bits (*a*)
- I/O Pad Buffers, as necessary (incl., Status and GPIO)

Local Registers:

Up/Down Counter Drive Voltage bits (*p+q)* Calibration Counter bits (no more than 16, or else can't fetch status) Previous Calibration Count bits (one level of history, for backing up) Calibration status bits (calibrating, direction, overflow/underflow, calibrated) Enabled/Disabled status bit

Global Buses:

A 16-bit bus, plus a few control/enable lines, will be all that is used to pass information to and from the elements in the array. This will enhance the scalability of the design.

Example Program Sequence Capabilities:

When designing the control system, we kept in mind both the application and educational desires we would like to see in the final result. For instance, we would like to be able to extract data that compares the open-loop to the closed-loop control of these elements. Here is a short list of program sequences that we would like to be able to put in the external ROM:

1. Set the entire array to phase phi=0 (calibrate system)
2. Move all mirrors down/up until at least one hits max/min voltage (find system range of motion)
3. Move all mirrors to a given voltage and measure error (calibrate element errors)
4. Calibrate at one voltage, increment/decrement to another, and then measure error (calibrate nonlinearity)

Approach to Analog Control at each Element:

The position sensing of the elements is done in parallel (each cell is responsible for its own). Upon a Calibrate instruction, each cell must cycle through the following sequence until either calibrated or unable to calibrate. The time for each cycle is determined by the instruction clock (i.e., next cycle starts at next instruction clock pulse). The instruction clock rate should approximate the mechanical settling time of an element, plus the time taken to compare calibration counts. It should also be greater than the time to set the D2A (via counter) and output a drive voltage. The micro-code will be simple and non-innovative; partial pseudo-code is shown below:

```
1.  If "calibrating" (i.e., if selected non-master)
        1.  Discharge ramp circuit
        2.  Latch current count into previous count buffer
        3.  Charge ramp circuit to threshold, and get a new current count
        4.  Compare master count to current count
        5.  If "undirected" (i.e., if second calibration cycle)
                1.  Set/reset "direction", based on comparison
                2.  clear "undirected"
        6.  If "improving" (the final calibration cycle, to determine if previous is
            closer than current to master)
```

1. compare master count to previous count
2. ...

7. Else
    1. If we've passed the master count , based on "direction" and "backing" and current comparison,
        1. invert "direction"
        2. If "backing" (cycles to move in opposite direction, to calibrate across instability region)
            1. set "improving"
        3. Else
            1. set "backing"
        4. if we are now worse off, back one step on D2A, and set "backing"
        1. else reset "calibrating"
    1. update D2A counter according to direction and "backing"
    2. if "backing" reset "backing" and "calibrating"
    3. Create the drive voltage, and wait until mechanical stabilization (wait for next instruction clock)
    4. ...

1. Else (i.e., if first cycle of calibration; note: each calibration cycle can take multiple instruction cycles)
    1. Set "calibrating" and "undirected", clear "backing" and "improving" (variables local to each element)
    2. If master
        1. Discharge ramp circuit
        2. Charge ramp circuit to threshold, and get count
        3. reset "calibrating"
    3. Else (if selected)
        1. Copy enable/disable bit from master
        2. Wait for mechanical stability and for count from master

Note: Since the ramp time is non-deterministic, the increment/decrement and D2A must be done on a separate (i.e., the next) cycle, to ensure its completion within the (instruction) clock period.

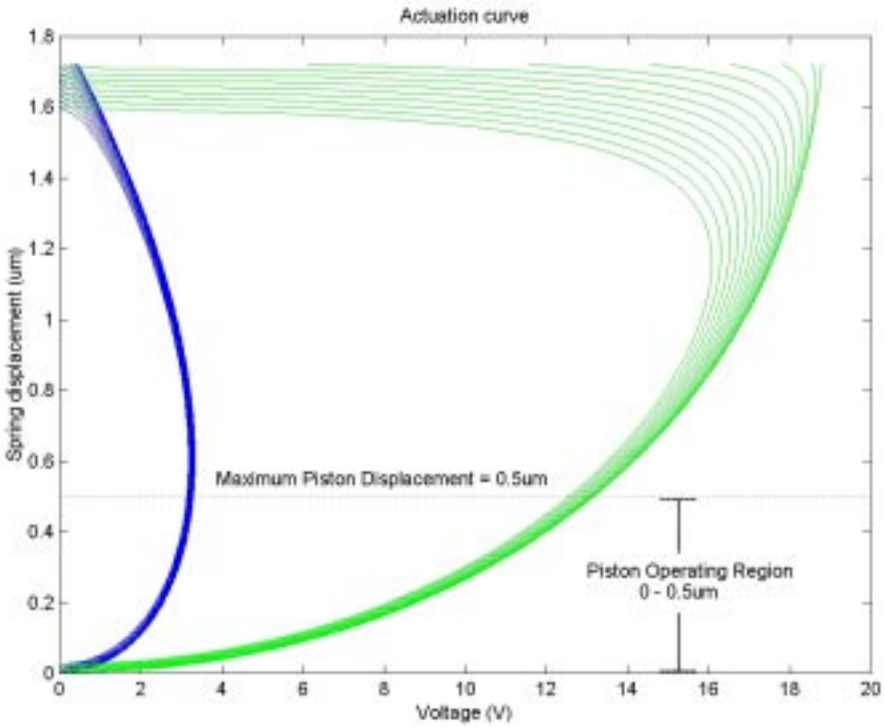
This method of calibration uses two changes in direction. The first is so this method can also work for elements with nonlinear hysteresis characteristics (e.g., pull-in of micromirrors beyond their stability range is not a problem). The second change in direction is done in order to add another half-bit to the precision; if the last drive step brought the element further away from the master, then simply backup to the previous drive value. The D2A input will saturate either at 0 or FF.

Absolute capacitance measurement is not needed since only vertical relative positioning is required. Constant-current ramping across the sense plates provides a means to compare two variable capacitances. Each cell is able to count the number of calibration clock cycles it takes to reach the (global) threshold on the cell's sense plate. It is able to compare this value with that of the master element, determine the direction to tweak the drive voltage, and if this direction changes, compare to the previous difference to determine whether to go back one step or to stop tweaking.

Cell Mechanics: Feedback capacitance

In a effort to overcome the inherent instability associated with electrostatically actuated MEMS pistons, we have implemented a stabilization technique using a series capacitor located on chip[xi]. Provided that the proper value for the capacitor is chosen, it will stabilize the mechanical displacement of the MEMS piston as the actuation voltage is increased. This stabilization keeps the piston from "pulling-in" its full mechanical displacement, upon sufficient applied voltage, and helps to provide smooth linear operation as required for this application. This series-series feedback provided by this capacitor is similar to the technique of emitter degeneration used in analog circuit design for the linearization of amplifiers.

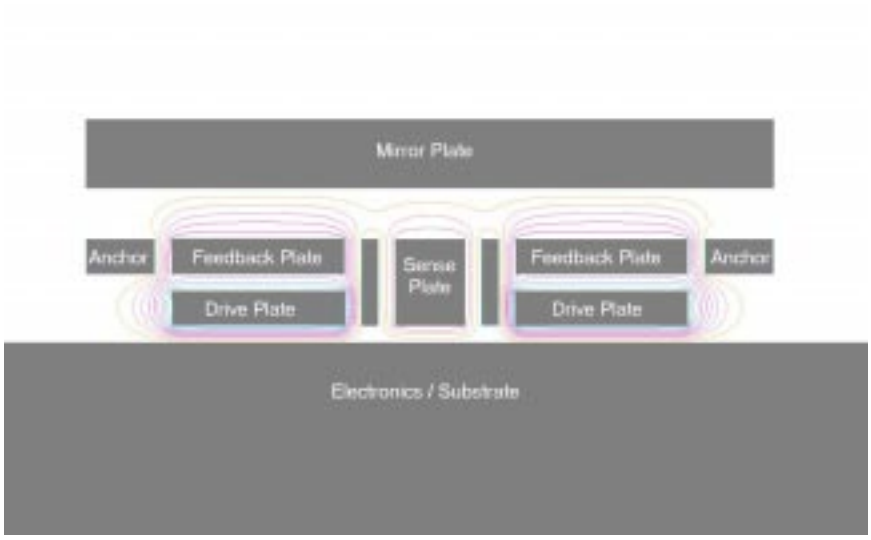
In the figure below there are two sets of displacement curves. These displacement verses voltage curves demonstrate how a MEMS piston operates if driven directly from a source, and how the addition of the feedback capacitor effects its actuation characteristics. The multiple curves, for both green and blue, are for different DC voltages on the sense plate. This offset on the sense plate produces a shift in the displacement curve for the MEMS piston. Offset voltage values for the sense plate are ranged from 0 to 1.4 Volts in 100mV steps. The blue curves on the left-hand side of the figure show how the MEMS piston actuates without the series capacitor, and the green curves in the right-hand side of the figure show how the MEMS piston actuates with the addition of the series feedback capacitor. By design, the maximum displacement of the MEMS piston is limited to 0.5um, and this portion of the operating region is indicated on the figure. Upon examination of these curves, the linearization effects of the feedback capacitor are easily observed, especially over the 0.5um operating region. Also, for optical applications it is best to have as linear a displacement characteristic as possible; therefore, the feedback capacitor not only keeps the piston from "pulling-in", but it also dramatically improves the operation of the piston. The trade-off when stabilizing with the addition of a series capacitor is in the size of the capacitor needed, and the proportionally large increase in needed drive voltage. By exercising the numerous metal layers available in this process the area cost of the feedback capacitor was eliminated and the ability to build dense arrays of these MEMS pistons was not sacrificed. The increased voltage cost is offset by a lower modulus in Copper, relative to typical materials used in fabricating MEMS pistons (e.g., polysilicon), allowing for extremely low actuation voltages. The needed drive voltage requirements are satisfied by the use of buffered MOS devices[xii,xiii] with long drains to help them withstand the large electric fields that will be present. Since the special MOS devices are only driving capacitors, the power dissipation is kept low. The curves shown in the figure below are representative of a particular device design. This design may be different from the final, and optimal, device design. However, for illustrative purposes these results are accurate.



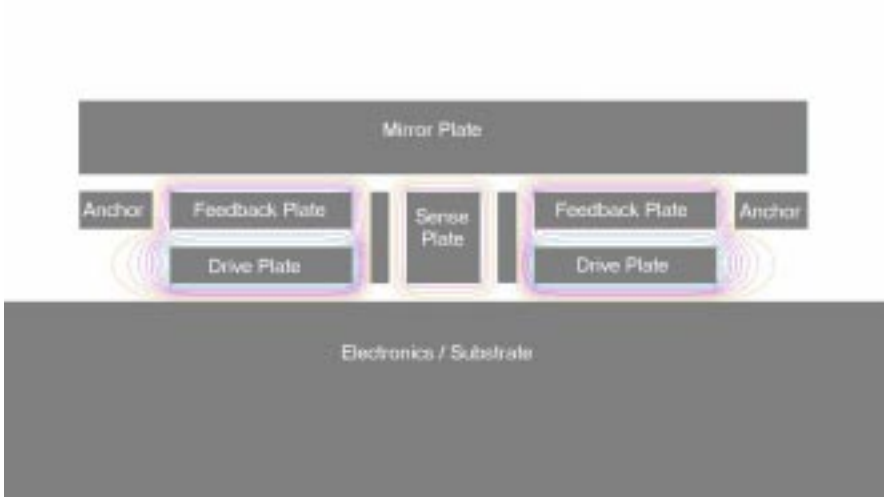
Displacement verses drive voltage with and without feedback capacitor.

Cell Electronics: Ansoft Field Solutions

In the design of MEMS devices, it is necessary to use low-level design tools or to write custom software: unlike the IC design industry, where CAD has matured greatly. Shown below are simplified examples of MEMS pistons where the field was found using an electrostatic field solver. In each solution, lines of equal potential are plotted for a given operating state of a MEMS piston that implements a sense plate for determining mirror height, and a series feedback capacitor for stabilization. The conductors that are not labeled are used for shielding the sense plate from the drive signal. The first figure shows the field solution for a piston in the “up”, or non-actuated position, and the second figure is the field solution for a piston in the “down”, or actuated position. The final and optimal MEMS piston design will vary from this simple design used for demonstrative purposes.



Equipotential lines for a simple MEMS piston in the “down” position.

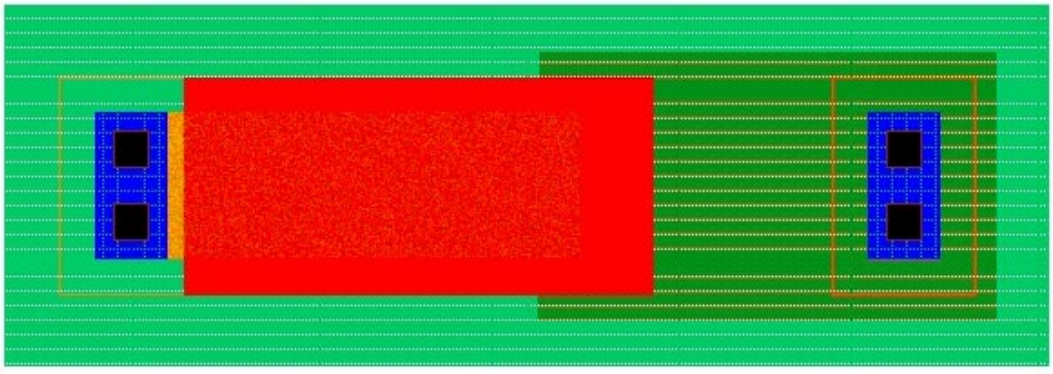


Equipotential lines for a simple MEMS piston in the “down” position.

Cell Electronics: High Voltage MOS Devices

As mentioned previously, the use of the series feedback capacitor requires that a larger drive voltage must be used to actuate the MEMS piston. Since the drive voltage requirement is on the range of 10 to 20Volts, and a fully integrated system is desired, special provisions must be made to insure that the on chip MOS devices can deliver the required drive voltage. Modifying the MOS device to handle these relatively large voltages requires the extension of the device’s drain and the addition of a buffering region, known as the SVX^x technique, between the drain and the

rest of the device. For a PMOS device this buffering region is made by the addition of a p-well region inside the n-well. The buffering region is the dark green area shown below. It has been demonstrated[ix,x] that devices in a 5V MOS process can be modified to handle in excess of 75V by using this technique; therefore, our requirements are attainable using this technique.



High-Voltage PMOS Device with buffering region shown in dark green.

Cell Electronics: Programmable Current Source

To insure that each MEMS piston is being discharged at the same rate it is necessary to make each current source tunable to compensate for on chip process and temperature variations. The programmable current source will have non-tunable value that will be chosen based on the size of the sense capacitor, the frequency of the sampling clock, and the desired accuracy. The tuning range, and tuning accuracy, will be determined based on expected process and temperature variations and desired accuracy. The example shown below has the ability to compensate a maximum of +/- 3% around the non-tunable current, with a resolution of 0.1%. This allows for a maximum mismatch in current sources of 6% across chip due to process and temperature variations.

The sequence for calibration, is as follows:

1. Master Controller addresses first Programmable Current Source Controller and places current source circuit into calibration mode. (Additional circuitry required for this function is not show in order to keep schematic clear.)

2. The additional circuitry handles routing of each current being tested to single known resistor. Since the same resistor is used for testing all current sources, the currents can be matched.

3. Appropriate values for each current source are stored locally.

4. Next current source is addressed and calibrated.

The operation sequence, is as follows:

1. Pre-Charge Pull-Up Device is activated to set sense capacitor to Vdd.

2. Piston position is set by D2A that drives High-Voltage Devices to actuate MEMS piston.

3. Discharge time of sense capacitor in determined and position error is determined.

4. Adjustments in piston displacement are made and steps 3 & 4 are repeated until desired accuracy is obtained.

5. Next MEMS piston is addressed and adjusted.

An important issue that cannot be ignored with this architecture is the loading effect induced by the capacitance of the current source on each sense capacitor. If the parasitic capacitance of the current source, pull-up device, and routing is not small relative to the sense capacitance it will be very difficult, if not impossible, to determine the displacement of the MEMS piston. It is important that the voltage being measured be sensitive to changes in displacement (i.e., the error of the sense capacitance). This sensitivity is defined below.

Sensitivity(Vx|Cerr) = Cserr / [Cs +Cserr + Cp]

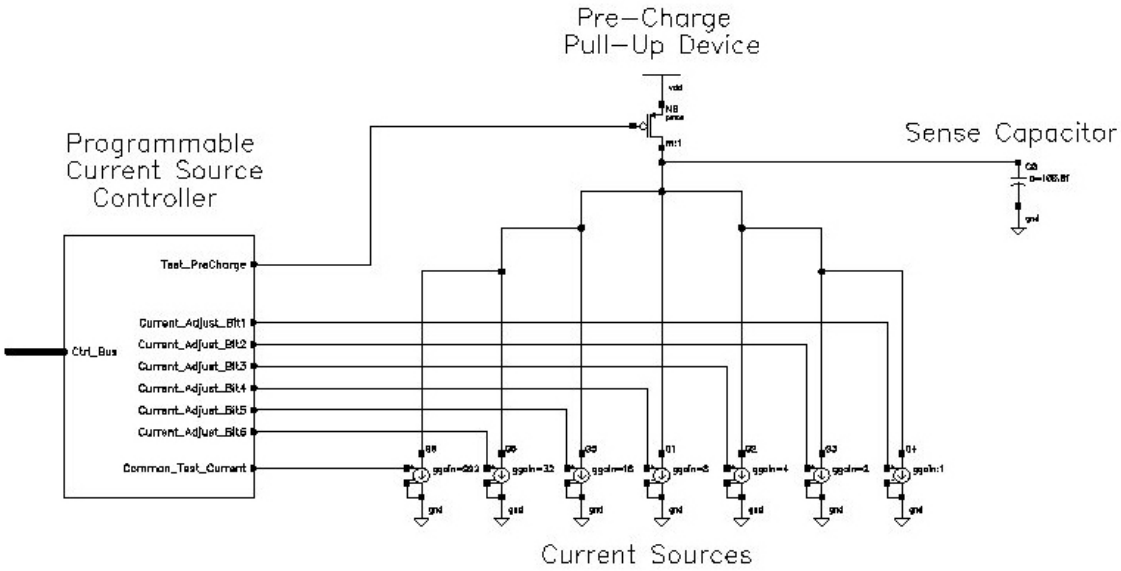
Where,

Vx = Voltage on sense capacitor

Cserr = Error capacitance that equates to displacement error

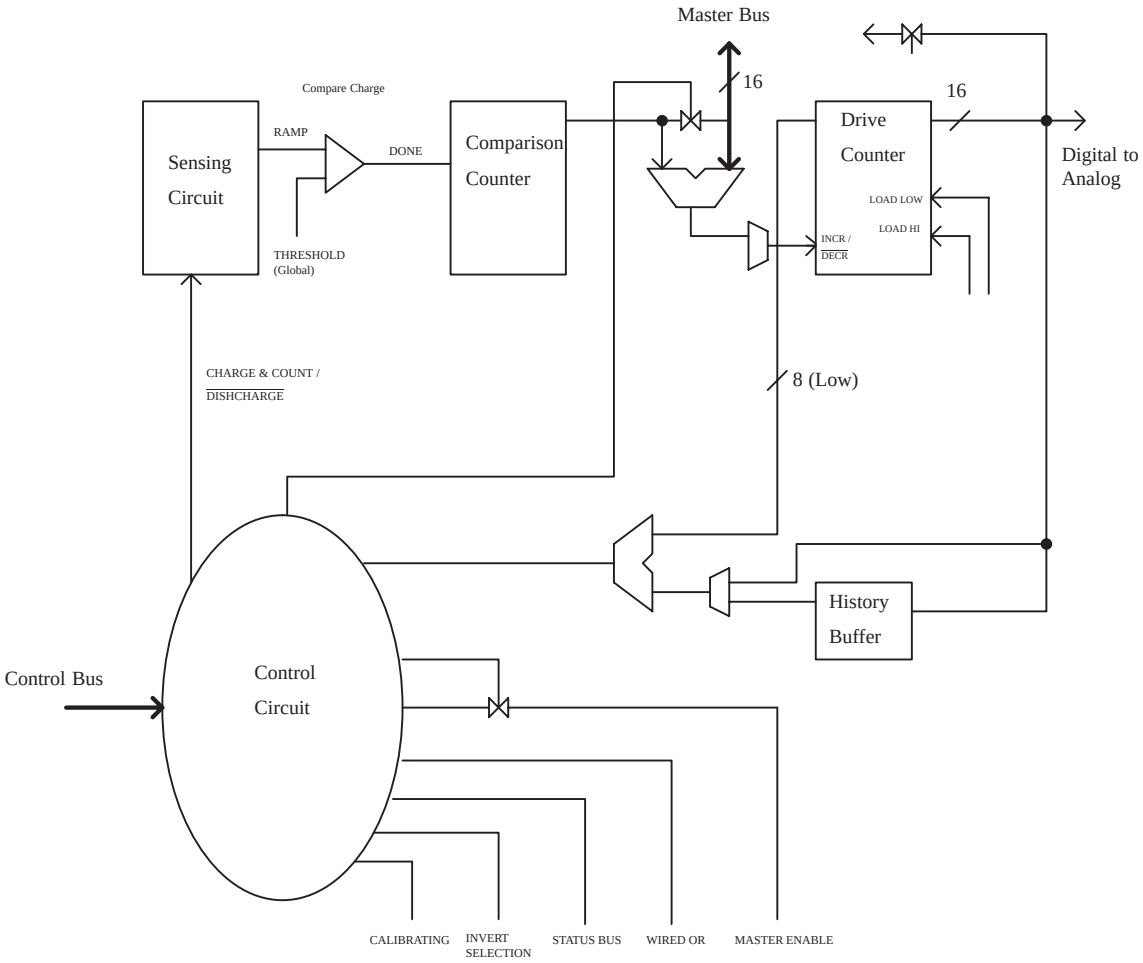
Cs = Nominal value of sense capacitance

Cp = Parasitic capacitances



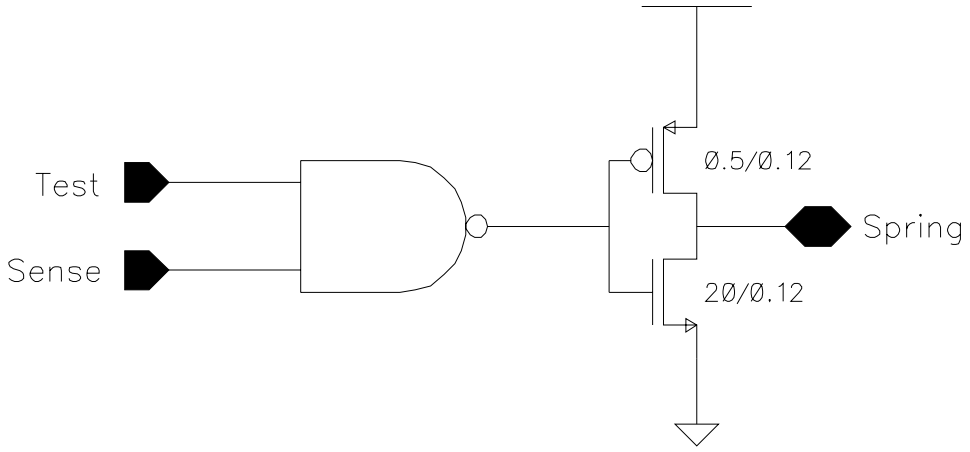
Schematic of Programmable Current Source and Controller.

4. Cell Schematic



1

Above is a diagram of the local control circuit for each cell. The capability for self-calibration to a reference value on the master bus is included, as well as an ability to generate a local electrostatic drive voltage. In addition, the local cell will be able to detect broken springs and stuck-down error states in the mechanics. The circuit below is inserted between the D2A and the base of each piston, for the purpose of these tests.



5. Summary

We believe we have on this chip enough to establish a set of design rules and a recipe for successful release of smart MEMS array designs. And, while chip size and time constraints prevent us from including elements that transduce energy from domains other than mechanical (e.g.: electro-optic, fluid flow, heat exchange, etc.), we believe our proof of feasibility to be extensible to microsystems in general. Our design will demonstrate a capability of UMC Cu for many future microsystems implementations.

Unique Achievements

In addition to this general objective, completion of this chip will achieve several other notable items that impact the chip design community:

- Mechanical Characterization of electroplated Copper
- MEMS and Cu-VLSI integration (Cu Damascene is best for both worlds; smart arrays of this density and size are impossible elsewhere, w/o extensive process optimization for each device design, as Texas Instruments did over their 10 year development of DMD; combined with post-processing, offers new markets for innovative devices)
- General Purpose Variable-Complexity Process (nitride acts as stop for each wet-etch, up to 5 releasable layers)
- First known smart micromirror array implementation, and control scheme suitable for many other smart array microsystems (where elements are able to react to external excitations)
- Creative use of dual actuation regions for adding amplitude modulation capability to a phase modulator array, and capacitive dividers for mechanical stabilization.

Efficiency

The monolithic nature, which we pursue with stacked mechanical and electrical devices, is inherently an efficient

use of silicon. Smaller MEMS elements are certainly desired for optical applications. While the limiting factor in our array design is the D2A, mechanical properties drastically change with scale. Mechanical scales will always lag behind IC scales, as models are difficult to find without empirical data. Our Phase-2 goal is to quantify the structural limits in the state of art IC process. Thus, we are attempting to quantify efficiency limits of mechanical implementations in this process, as well.

Testing

Studies were made in this report of critical components: the high voltage D2A, the calibration circuit, and the use of Copper springs. But we still expect to run into difficulties with the operation of the microsystem. We have for this reason included testing provisions, for any possible outcome states of the processing:

- ISA provides or calibration amongst elements, and to a system reference
- ISA fetch "Status" allows for external test of
    - spring breakage (detection on each)
    - current source accuracy (and correction)
    - basic functionality of global control readily seen by predictable instruction fetch cycles on bus
- Evaluation of optimal clocking and analog power rails will be possible through subsequent fetch of calibration counters, following forced positioning of cells ("Move" or "Get", followed by "Calibrate" and "Status" commands)

5. Acknowledgements

Many thanks go to Dr. Carlton Osburn for his advise and input, Dr. Paul Franzon for giving us time to work on this project, Joan O'Sullivan for her patience as we toured and made preparations for our cleanroom work, Toby Schaffer for our excellent Cadence support, Microcosm Technologies for access to their latest MEMCAD software, and UMC for their release of information that we needed to complete phase-1.

[i] http://imems.mcnc.org

[ii] Y. B. Gianchandandani, H. Kim, M. Shinn, B. Ha, B. Lee, K. Najafi, C. Song. “A MEMS-First Fabrication Process for Integrating CMOS Circuits with Polysilicon Microstructures.” MEMS 98. Proceedings., The Eleventh Annual International Workshop on , 1998 , Page(s): 257 –262.

[iii] http://www.memsrus.com/cronos/svcsmumps.html

[iv] G. K. Fedder. “Integrated Microelectromechanical Systems in Conventional CMOS.” ISCAS '97, Proceedings of 1997 IEEE International Symposium. Volume: 4 , 1997 , Page(s): 2821–2824.

[v] Darren T. Johnson, "The detection of sugars and amino acids calls for the use of copper as the sensor material on a silicon substrate.”

[vi] Williams, K.R.; Muller, R.S. "Etch rates for micromachining processing." Microelectromechanical Systems, Journal of. Volume: 5 4 , Dec. 1996 , Page(s): 256 -269

[vii] Biebl, M.; Brandl, G.; Howe, R.T. "Young's Modulus Of In Situ Phosphorus-doped Polysilicon." Solid-State Sensors and Actuators, 1995 and Eurosensors IX.. Transducers '95. The 8th International Conference on. Volume: 2, Page(s): 80 -83.

[viii] Guckel, H.; Burns, D.W.; Tilmans, H.A.C.; DeRoo, D.W.; Rutigliano, C.R "Mechanical properties of fine grained polysilicon-the repeatability issue." Solid-State Sensor and Actuator Workshop, 1988. Technical Digest., IEEE, 1988, Page(s): 96 -99.

[ix] Guckel, H.; Randazzo, T.; Burns, D. W. "A simple technique for the determination of mechanical strain in thin films with applications to polysilicon." J. Appl. Phys. 57 (5), 1 March 1985.

[x] Bifano, T.G.; Perreault, J.; Krishnamoorthy Mali, R.; Horenstein, M.N. “Microelectromechanical Deformable Mirrors.” Selected Topics in Quantum Electronics, IEEE Journal on. Volume: 5 1 , Jan.-Feb. 1999 , Page(s): 83–89.

[xi] Joseph I. Seeger, Selden B. Cray. “Stabilization of Electrostatically Actuated Mechanical Devices.” IEEE TRANSDUCERS, International Conference on Solid-State Sensors and Actuators, 1997 , Page(s): 1133 –1136.

[xii] M. Declercq, F. Clement, M. Schubert, A. Harb, M. Dutoit. “Design and Optimization of High-Voltage CMOS Devices compatiable with a standard 5 V CMOS Technology.” IEEE Custom Integrated Circuits Conference, 1993 , Page(s): 24.6.1–24.6.4.

[xiii] Hussein Ballan, Michel Declercq. "High Voltage Devices and Curcuits in standard CMOS Technologies.” 1999, Dordecht: Kluwer Academic Publishers, Page(s): 77-116.