6C.4 Chip-Package Codesign - Challenges and Directions

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Increasingly the package, and associated discretes, contribute critically to the overall circuit performance, rather than just providing a connection function. These performance issues are critical today and are fast becoming more complex than current CAD tool trends will be able to support. For example, in today's digital systems, the package design is an important part of the signal integrity equation, and a major determinant of board routing costs. The concentration is on signal integrity management. However, in tomorrow's systems, the promise of high density packaging presents novel integration opportunities that will require new design approaches beyond just managing signal integrity, other connectivity and performance issues will enter into play. For today's RF and analog systems, the package is part of the load and antenna environment and again presents a difficult signal integrity analysis. In tomorrow's systems, new technologies and higher performance/frequency requirements will require system modeling solutions far superior to those offered today. In both types of systems, the package design is starting to require the sophistication normally reserved for the IC design. It is time for the packaging CAD tools to recognize this trend and prepare for it. The first part of this talk will review these system design trends and give examples from work performed at NCSU and elsewhere. The second part of this talk will present the state of the art for CAD support for chip-package codesign and postulate that the continuation of current trends will not give satisfactory solutions for future systems. It is argued that a new approach is needed, one hinging on codesigning the package, chip and system in a unified chip-centric environment while maintaining suitable levels of abstraction to permit interaction across inter-disciplinary teams.