PIN ASSIGNMENT FOR HIGH-PERFORMANCE MCM SYSTEMS

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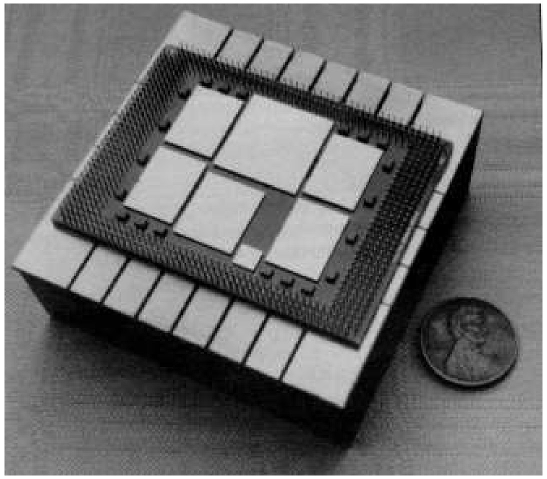
ABSTRACT

A very fast and efficient pin assignment strategy and algorithm for the early design phase of high-performance Multi-Chip-Modules (MCM) is proposed, which minimizes total wire length, while satisfying the timing constraints. Different delay models are used for on- and off-chip nets for an accurate delay estimation. The proposed pin assignment methodology is applied to a Superscalar Microprocessor design partitioned on an MCM to show that the final design most likely converges to a good result with only a few iterations.

System Design Optim. for MCM-D/Flip-Chip



New Ideas

- Partition CPU onto MCM
- Physical system design tools
- Optimize yielded cost
- Optimize interconnect mix

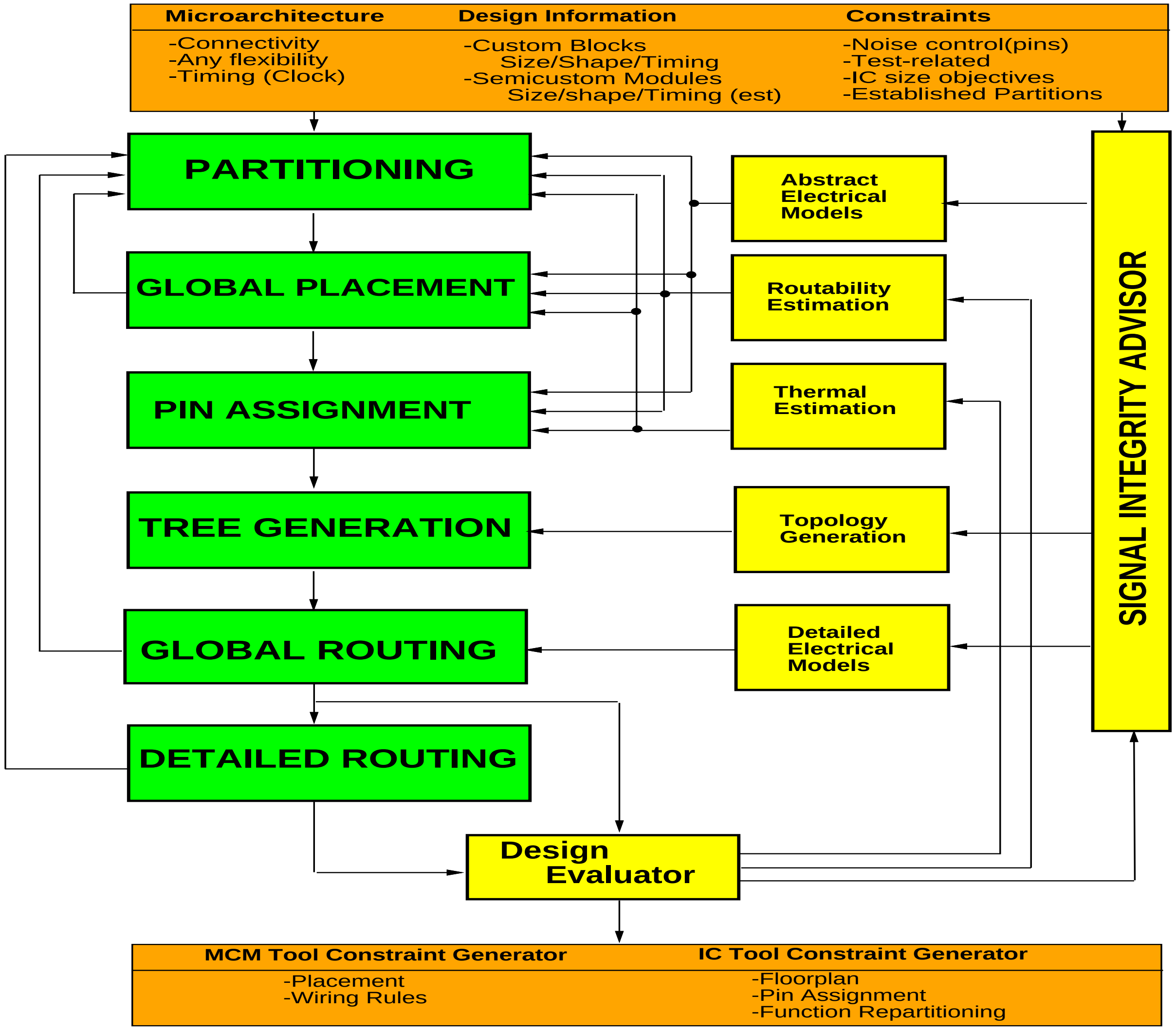
MCM Early Design CAD Tool Objectives

- meet all required timing and noise constraints,
- satisfy thermal and power requirements,
- be routable with minimum effort.

Early Design CAD Flow for MCMs

In the early design phase of high-performance custom or semi-custom MCM systems, the required tasks that must be completed include:

- Optimal Design *Partitioning* from a set of systems specifications,
- A *Global Placement* which would provide an hierarchical floorplan of the modules within the chips and the chips within the MCM,
- An efficient *Pin Assignment* that will ensure timing constraints and routing completion.
- A *Global Routing* that manages delay, signal integrity and congestion simultaneously.


Microarchitecture
-Connectivity
-Any flexibility
-Timing (Clock)
Design Information
-Custom Blocks
Size/Shape/Timing
-Semicustom Modules
Size/shape/Timing (est)
Constraints
-Noise control(pins)
-Test-related
-IC size objectives
-Established Partitions
PARTITIONING
GLOBAL PLACEMENT
PIN ASSIGNMENT
TREE GENERATION
GLOBAL ROUTING
DETAILED ROUTING
Abstract Electrical Models
Routability Estimation
Thermal Estimation
Topology Generation
Detailed Electrical Models
SIGNAL INTEGRITY ADVISOR
Design Evaluator
MCM Tool Constraint Generator
-Placement
-Wiring Rules
IC Tool Constraint Generator
-Floorplan
-Pin Assignment
-Function Repartitioning

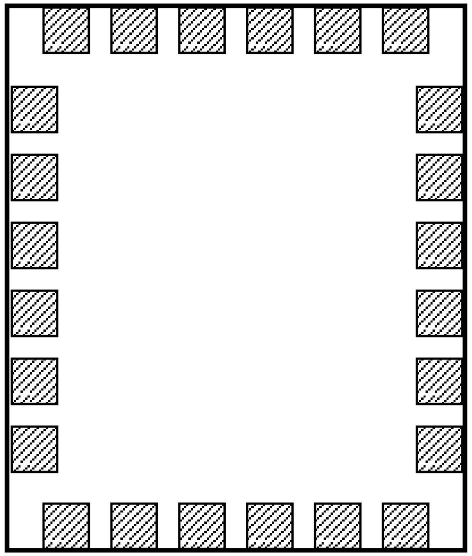
Need for Performance-Driven Pin Assignment

Performance Driven Pin Assignment performed at a very early stage in the design cycle is crucial to continued improvement in MCM system performance.

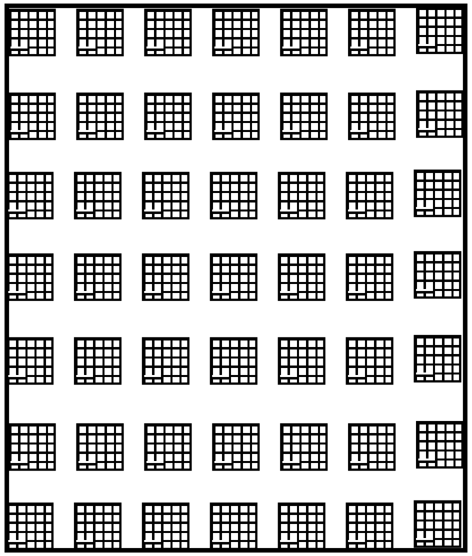
We propose a Pin Asssignment strategy that :

- Manages the complexity associated with high-pin count systems,
- Allows for timing constraints to be accounted for early in the design phase.
- Differenciates between on-chip and off-chip nets in order to maximize the probability of meeting the timing constraints.
- Supports different chip pad placement MCM technologies (periphery based, flip-chip/solder bump)

Supported Chip Pad Models



Periphery based
Chip Pad placement



Flip chip/solder bump
placement technology

Pin Assignment Strategy

- Represent design's physical layout on the dies and the MCM substrate through a 2-D array.
- Use pre-characterized delay models for on-chip and off-chip routed nets to estimate wiring delay.
- Prioritize all nets according to their timing slacks.
  $timing\ slack_v$ = maximum allowed delay of net_v *(based on design timing constraints)* - estimated net_v delay *(based on delay models and global placement)*, $\forall$ net $v \in$ design netlist.
- Find the Center of Gravity (CoG) of the blocks connected to each net
- Pick the first available pin of the block which is closest (manhattan distance) to the CoG.

Pin Assignment Algorithm

Input: Global Placement

Objective: Minimize total wire length

st. : Timing constraints

Step 1:

Distinguish between on-chip and off-chip nets.

Step 2:

Set up **Priority List**;

Sort Nets; (increasing order according to their timing slacks)

Create list P_v, where $slack_v < slack_{v+1}$, $\forall$ v ϵ (0 to NETMAX)

Step 3 (Main Loop) :

for all P_v nets

do :

- **if** P_v net is on-chip
  then :
  - Compute Center of Gravity of all blocks;
  - Assign pins on the periphery of the blocks;
- **if** P_v net is off-chip
  then :

  for all blocks(of P_v net) in the same chip
  do :
  * Compute Center of Gravity of all blocks;
  * Pick chip pad that is closest to the CoG;
  * Assign pins on the periphery of the blocks;

Step 4 :

for all P_v nets

call *evaluate(v)*;

Step 5 :

if *timing penalty(v)*=0 , $\forall$ v ϵ (0 to NETMAX)

then :

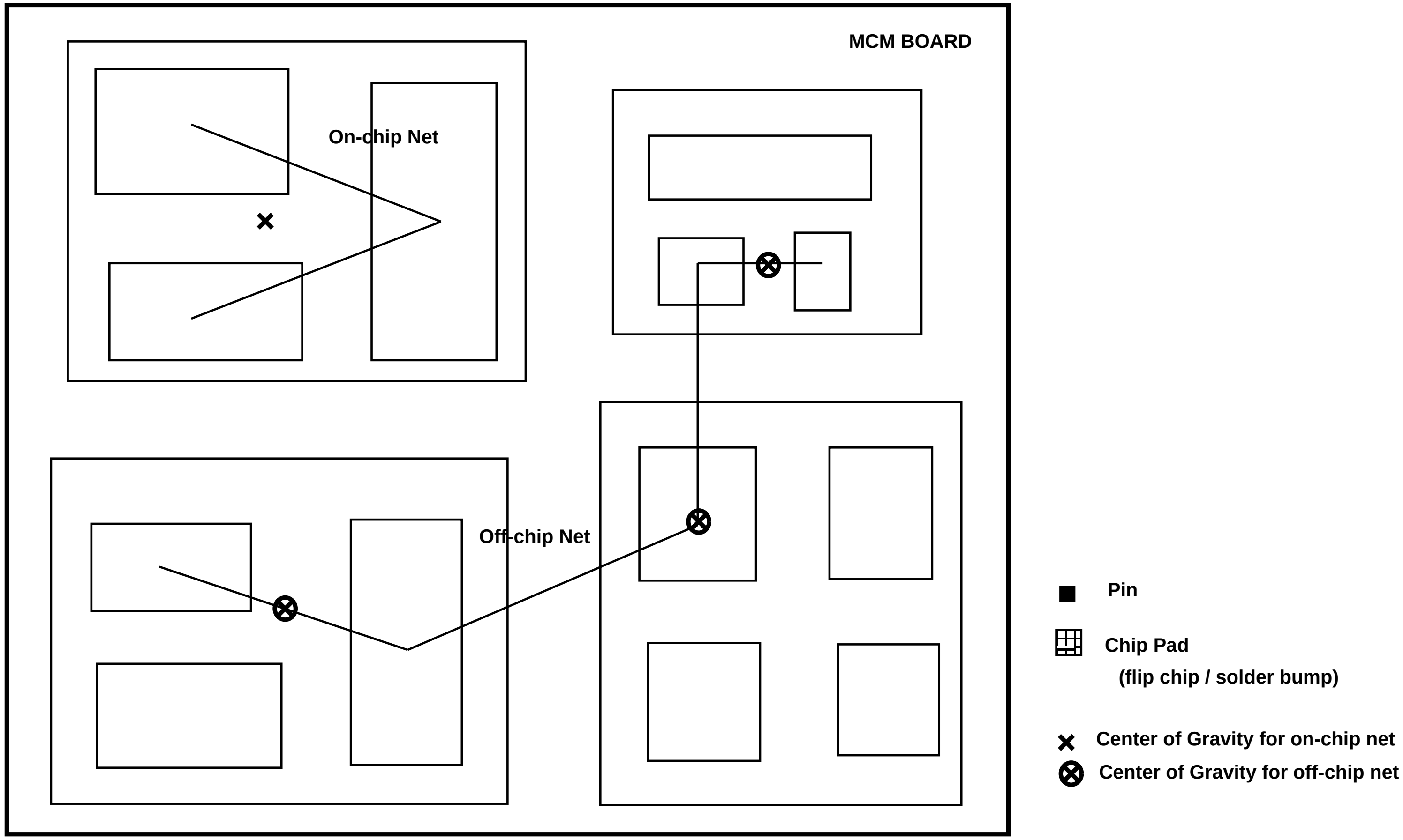
- stop;

else :

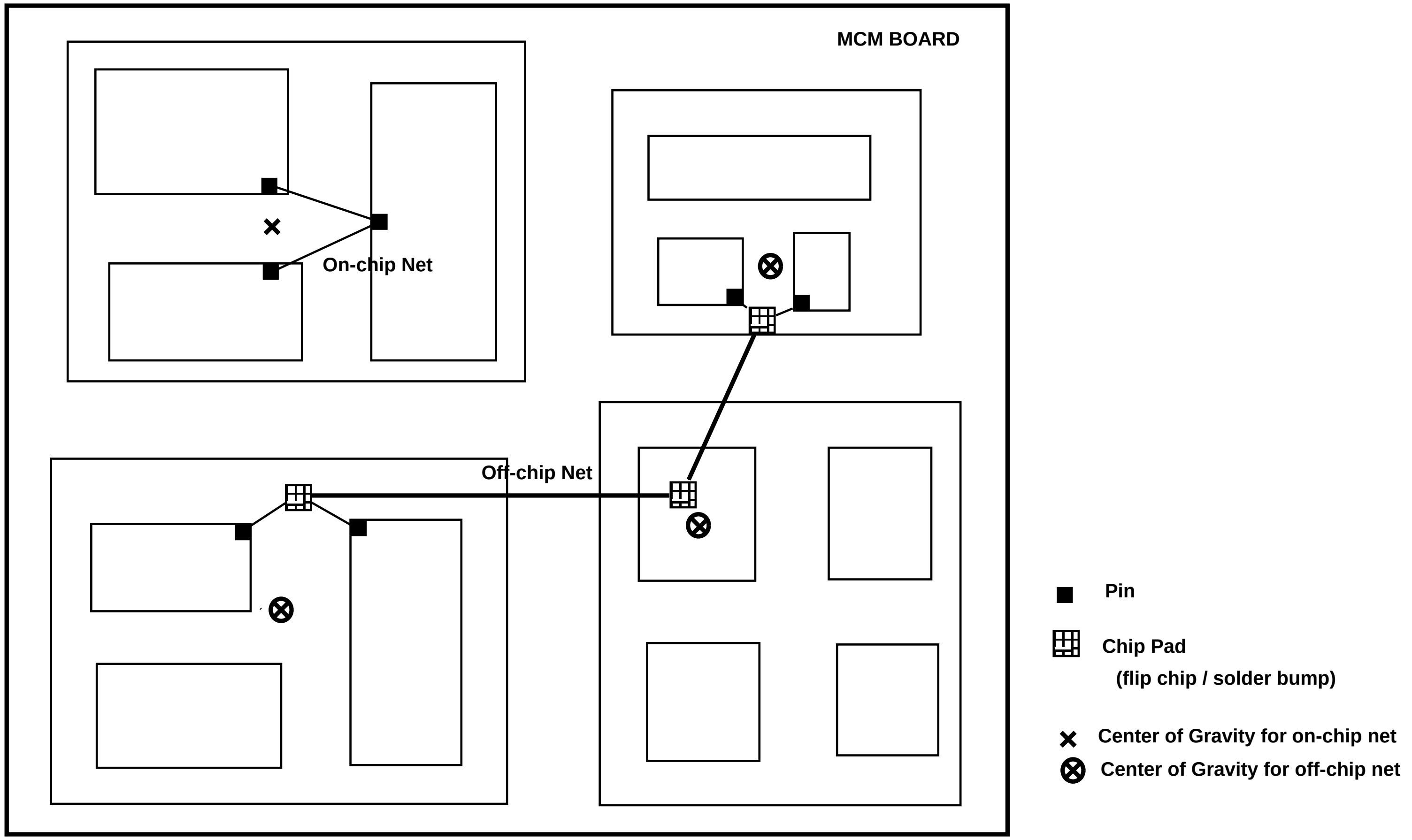
- **while** counter < maximum number of iterations
  do :
  - increase i (in the P_v List) of the nets that failed;
  - counter=counter+1;
  - go to *Step 3 (Main Loop)*;

Output: Global Placement with pins and chip pads assigned

Before Pin Assignment



After Pin Assignment



Evaluation of Pin Assignment Stage

The following procedure is performed to check if a net meets the timing constraints:

- **Generate tree for** net_v,
- **Calculate length** net_v ,
- **Estimate delay of** net_v**:**
  - **if** $net\ v$ is on chip
    use on-chip model *(distributed RC model)*
    else
    use off-chip model *(distributed RLC model)*
- **Calculate timing penalty**: $timing\ penalty_v$ = estimated net_v delay - maximum allowed delay of net_v .

Tree Generation

A "Rectilinear Steiner Tree with a Trunk" topology, provides a fast and reasonable approximation of the net's length.

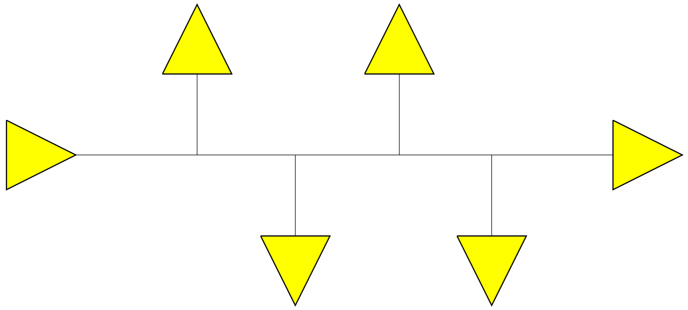
- Specify fixed vertices with respect to a set of reference x and y axes.
- Determine extreme points along the x and y axes to describe the enclosing rectangle.
- Form the trunk of the tree:
  Draw line bisecting the rectangle into two equal rectangles (either along the x-axis or the y-axis)
- Connect each of the fixed vertices to the trunk through stubs.

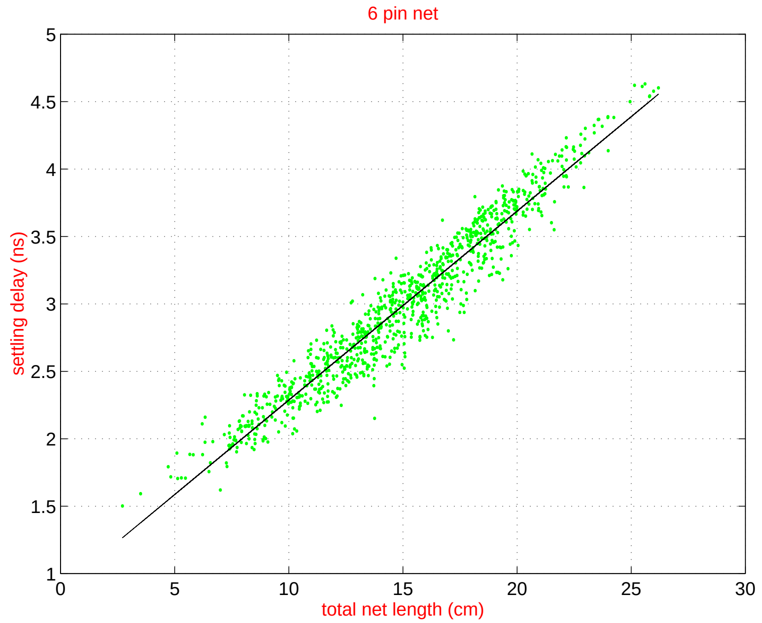
Abstract Electrical Modeling

Accurate Delay Estimation, based on

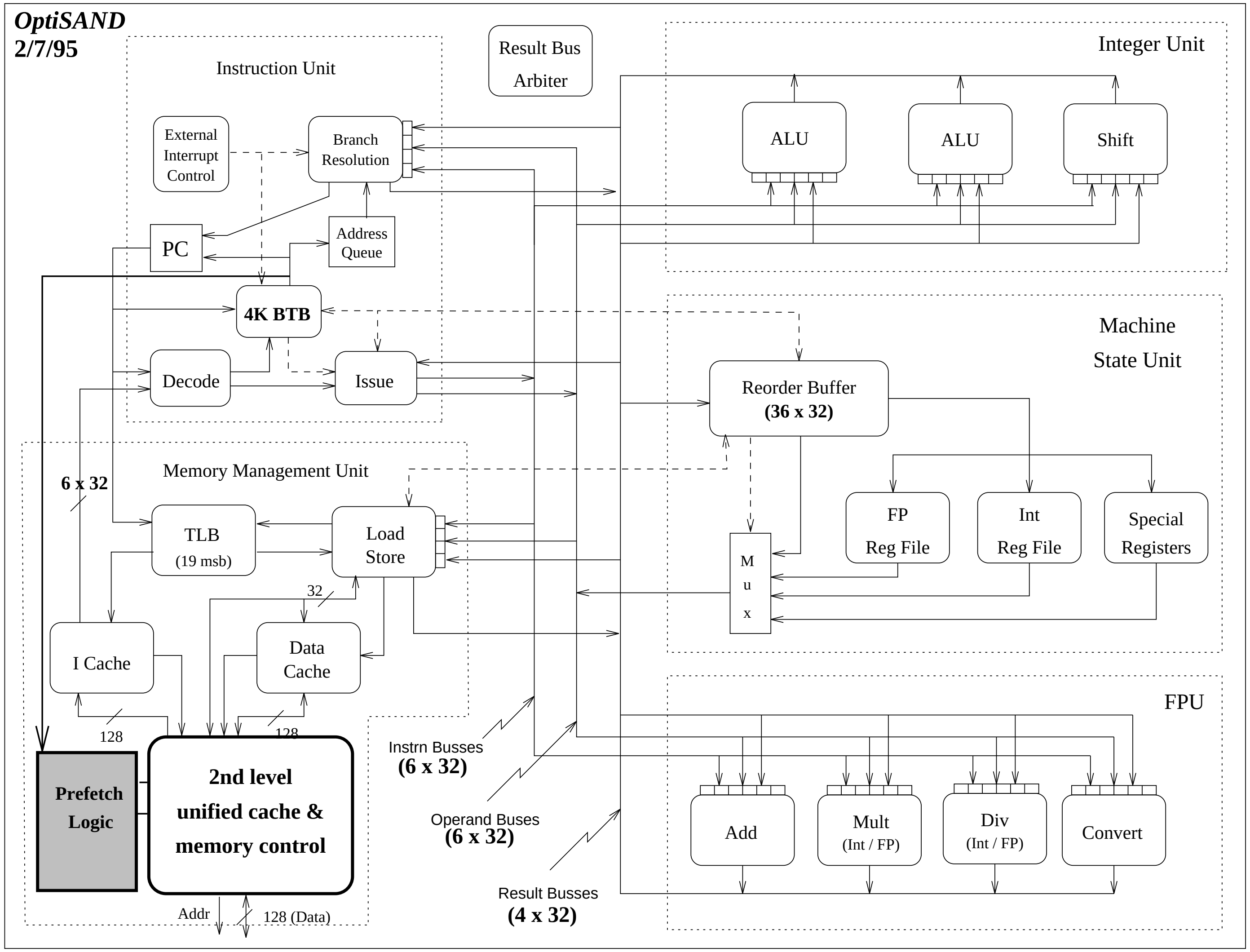
- Simulation-based precharacterization of each net class according to the number of pins.
  - Distributed RLC for off-chip nets. (lossy transmission lines)
  - Distributed RC model for on-chip nets.
- Generation of scatter plot (delay vs. net length).
- Fit into a linear equation.

6 pin net topology





Design Case Study



Experimental Results

Design case study: General Purpose Superscalar Microprocessor (OptiSAND)

- 28 blocks,
- 1018 signal nets,
- 6492 pins,
- varying net multiplicity (from 1 to 192).

After partitioning and global placement on an MCM, the design was introduced to the Pin Assignment Tool (Implementation of algorithm in about 800 lines of C)

- Assignment of all Pins and Chip Pads: 6 secs/CPU time,
- Execution of the main loop : 3 Times.

Conclusions

- A very fast and efficient pin assignment algorithm for the early design phase of high-performance MCM systems is proposed.
- The main objective is to minimize total wire length, while satisfying the timing constraints.
- Both chip pad placement technologies (periphery based, flip-chip/solder bump) are supported and both on-chip and off-chip nets are treated appropriately by using different timing delay models for each type in order to check if the pin assignment meets the timing constraints.
- This pin assignment strategy could also be used as an evaluation metric during the partitioning and global placement process providing early warning to potential design problems.

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