Simulation of High Speed Interconnects Using a Convolution-Based Hierarchical Packaging Simulator

Mark S. Basel, *Member, IEEE*, Michael B. Steer, *Senior Member, IEEE*, and Paul D. Franzon, *Member, IEEE*

***Abstract*—A specialized packaging simulator is presented which uses an impulse response model of the interconnect network to model high speed digital systems. Behavioral models of drivers and receivers are used. A hierarchical strategy is developed which uses point modeling of discontinuities and the concept of coupling groups to facilitate tradeoffs between accuracy and run time. A new impulse response/convolution technique is developed to efficiently handle large distributed interconnect networks. With this technique, impulse response thresholding provides a smooth transistion from delay modeling of interconnects to full distributed circuit simulation.**

I. Introduction

With the trend towards lower supply voltages, higher clocking frequencies, and denser interconnect, appropriate design and simulation techniques are essential in ensuring signal integrity. The verification of signal integrity of a packaged system requires that the entire interconnect system be simulated for many clock cycles. Only then can such events as a reflected crosstalk signal from a previous clock period affecting signals from the current clock period be captured. Efficient simulation requires that the modeling of transistor circuitry and of large distributed circuits be optimized to minimize computation time. In the conventional SPICE paradigm every transistor and parasitic element is treated individually along with discrete models of every element (a bend, a transmission line, etc.) of the interconnect network. The many simulation techniques applicable to interconnect simulation mostly are concerned with efficient incorporation of these models in transient simulation. With active circuits drammatic reduction of simulation time is achieved using behavioral models, such as IBIS models [1], for drivers and receivers.

In the past simple delay models of interconnects were sufficient and resulted in rapid simulation. Recently more sophisticated modeling has been required for critical nets. With more and more nets becoming important, and the greater sophistication required to capture simultaneous switching noise, the number of discrete interconnect elements to be included in simulations is increasing rapidly. It will clearly become impractical to handle all of the individual elements using iterative analysis. Furthermore, as the use of a variety of frequency domain modeling techniques (2-D and 3-D electromagnetic modeling, for example) are required, it will become increasingly difficult to develop SPICE compatible models. For this reason it makes sense to first treat the interconnect network in the frequency domain where the results of various interconnect modeling tools can be conveniently merged. By representing the interconnect network by an N port block, the advantages of behavioral modeling are extended to the interconnect network. In the frequency domain, numerical analysis of the interconnect network is both linear and algebraic and effects such as skin effect cannot be described in the time domain.

It is the purpose of this paper to present a simulation strategy which facilitates efficient simulation by enabling a trade-off between modeling accuracy and reduced simulation run time. A smooth transistion between delay modeling of interconnects to full distributed modeling is achieved through the use of thresholding of the impulse response of the entire interconnect network. The impulse response/convolution approach is essential to fully utilize the techniques presented here. However, traditional approaches suffer from aliasing problems due to the frequency domain-to-time domain transforms involved. In this paper a new convolution technique and error correction techniques are developed and the hierarchical packaging simulator is applied to several circuits to demonstrate the operation of the techniques presented.

II. Interconnect Modeling and Simulation—Background

The fundamental difficulty encountered when incorporating transmission lines in transient circuit simulation is that while circuits containing nonlinear devices or time dependent characteristics must be characterized in the time domain, transmission lines with loss, dispersion, and interconnect discontinuities are best simulated in the frequency domain. Many techniques have specifically addressed the incorporation of lossy transmission line models in a transient simulator. Almost all of the work has been focused on developing efficient methods to handle individual elements (coupled and uncoupled transmission lines) and little effort has been directed at the more general problem of efficiently handling the complete interconnection problem with its multiple elements. We are interested in general methods which are compatible with transient simulation

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M. B. Steer and P. D. Franzon are with the Electronics Research Laboratory, Department of Electrical and Computer Engineering, North Carolina State University, Raleigh, NC 27695-7911 USA.

M. S. Basel was with North Carolina State University. He is now with Integrated Silicon Systems Inc., Research Triangle Park, NC 27709 USA.

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with nonlinear devices. Thus four fundamental approaches are of interest: subcircuit modeling, the method of characteristics, asymptotic waveform evaluation (AWE), and convolution.

A. Subcircuit Modeling

Modeling a transmission line as cascaded RLC subcircuits is primitive, but is the method currently used by most transient simulators. In this approach each RLC circuit models a small section of the line. The problem here is that a modeled transmission line has an instantaneous response and, when excited by a pulse, exhibits excessive ringing [2].

B. Asymptotic Waveform Evaluation

The time required to simulate a large interconnected network can quickly become prohibitive using the conventional SPICE paradigm of modeling individual elements and applying iterative techniques to determine the circuit quantities describing the state of each. The asymptotic waveform evaluation method (AWE) reduces the size of the problem by first developing a reduced model. The complete network is first modeled in the frequency domain and a large s domain transfer function developed. The reduced model is a reduced order approximation of the transfer function and, in transient analysis, is modeled by controlled current sources. The net result is that a much smaller problem is presented to the transient simulator for iterative solution. The principle advantage to AWE is its speed. For a given interconnection system, AWE can produce waveform results from 100 to 1000 times faster than the conventional "every-element" SPICE approach [3].

Most AWE implementations [3] use a partial Padé approximation, although this can lead to instability and inaccuracy [4], [5]. Other approaches (known as stable moment matching methods) such as the Routh approximation [6] and the Padé—Hurwitz approximation [4] guarantee stability, but the simulated responses do not always resemble the original systems [7], [8]. Moment matching approximations have stability problems primarily because of the generation of right half plane poles during the approximation process. Work is being done on these problems by including optimized pole selection and enhanced numerical integration algorithms in the AWE method [9], [10].

Another problem with AWE arises from the fact that distributed networks do not have a finite pole-zero response (unlike the lumped element representation of a distributed structure) and so the reduced moment model does not include retardation (due to the finite time-of-flight). The consequence of forcing a finite response is that the circuit now has an instantaneous response and the inherent delay in distributed interconnection systems cannot be modeled. This problem has been addressed by approximating the frequency dependent characteristic impedance $Z_0(s)$ using the Padé method to approximate $e^{-l\Gamma(s)}$ [11]–[17], but this is only applicable to modeling line elements individually. With this information, the transmission line response can be evaluated correctly using AWE with each transmission line segment incorporated in the transient simulation as a separate element.

C. Method of Characteristics

The method of characteristics first introduced by Branin [18] has been used to simulate wave propagation in lossless coupled transmission lines and has recently been expanded to handle lossy possibly nonuniform dispersive lines [4], [19]–[22]. Since the method of characteristics is a time domain method, it is a simple matter to incorporate arbitrary nonlinear loads. The model also integrates smoothly with speed up techniques such as waveform relaxation [4].

The method of characteristics is a technique for turning the time domain coupled partial differential equations making up the telegraphers' equations into a system of uncoupled ordinary differential equations (ODE's). Physically the method of characteristics can be viewed as modeling an N coupled line section by a section of N uncoupled lines (one for each transmission line mode that can exist) which are coupled at the ends of the section by a linear circuit that couples the lines together. Such a simple interpretation is only possible for lossless lines, as then the ODE's can be solved directly resulting in a closed form solution [18]. For lossy lines the ODE's must be solved using numerical integration. Here the equations are solved by discretizing along the longitudanal and time axes and then the voltages and currents at time $t + \Delta t$ are calculated from the known values at time t. The process is repeated for the duration of the simulation time.

D. Convolution Methods

In convolution methods an interconnect system is described by its impulse response from each external terminal of the interconnect network to itself and to every other external terminal [23]–[26]. Transient analysis is achieved using convolution of this impulse response with the voltages at the terminals interfacing the interconnect network with the remainder of the circuit. Earlier implementations applied convolution to (possibly coupled) transmission line sections and use the conventional SPICE iterative analysis approach to handle other linear circuit elements.

For systems clocking at the high hundreds of MHz and above, the convolution technique appears to be the only viable approach as the frequency domain characterization of the interconnect network is used in its entirety. However, convolution can suffer from several aliasing problems related to dealing with responses that are neither time- nor frequency-limited and that can have large dynamic ranges. Aliasing errors such as non-causal effects, aliasing, and Gibb's phenomenon often lead to numerical convergence problems due to accumulated error as well as inaccurate simulation. The most serious of these problems is non-causal effects which are largely due to the artifical filtering required to band-limit frequency domain parameters. This is a problem with previous convolution-based techniques [2], [23], [25], [27]–[41]. These various methods differ in the way in which the frequency domain parameters are derived, the attention given to limiting the dynamic range of the response presented to the inverse Fourier transformation, and actions taken to limiting the time response and band-limit the frequency response of the network. All of the techniques can be adapted to function with a transient simulator. The

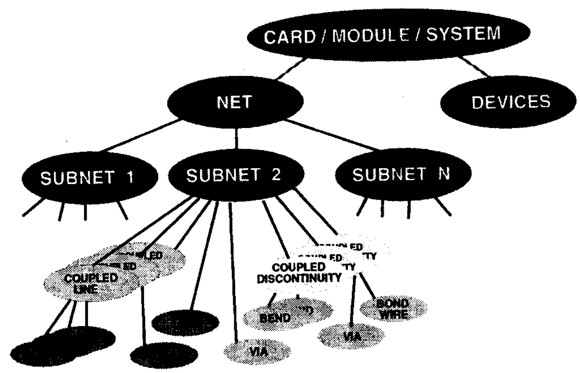


Fig. 1. Hierarchical description of an interconnect network.

techniques develop a Green's function relating the voltage or current response at one port of the interconnect network to the voltages at past times and at all ports of the network. In special situations it is possible to derive this impulse response analytically and exactly [2], [42], [43], but only for single line sections. Djordjevic *et al.* [36] limit the time response and dynamic range by introducing an augmentation network to terminate transmission lines in their approximate characteristic impedance. The inverse Fourier transform of the y parameters of this augmented network is calculated and the effect of the augmented network removed in transient analysis. Low-pass filtering was introduced in [44] to also achieve frequency limited responses. However, this does not have a physical interpretation and sometimes resulted in noncausal responses. This was refined in [26] to achieve natural bandpass filtering using packaging parasitics which low-pass filter the network parameters.

III. Hierarchical Network Modeling

The distinguishing feature of the work presented here is an hierarchical modeling and simulation paradigm; the essentials of which are as follows:

1) A point modeling approach for discontinuities, which, if speed-up is desired, enables small discontinuities to be ignored with minimum effect on accuracy. This was presented in [45].
2) Hierarchical representation of an interconnect network permitting various levels of complexity of interconnect simulation, see Fig. 1. This provides a tradeoff of simulation accuracy and simulation time by facilitating run time selection of, for example, whether a set of lines is treated as coupled (a coupling group) or uncoupled.
3) The entire linear interconnect network is modeled by first finding the y parameters of the linear network and then reducing it to that of a smaller network with nodes which are at the interface of the linear network and the nonlinear drivers and receivers. In this way most of the interconnect circuitry is treated as a linear algebraic problem rather than as an iterative problem, as it is in a traditional SPICE analysis.

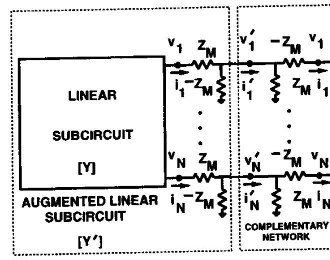


Fig. 2. N port distributed network partitioned into linear and nonlinear subcircuits.

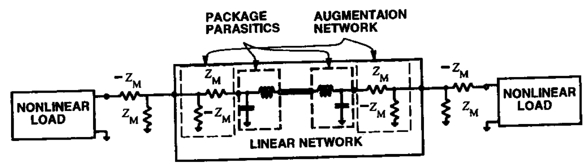


Fig. 3. Model of a single transmission line net with packaging parasitics and augmentation networks.

4) Impulse response thresholding is used to obtain efficient simulation by reducing the number of bins in the discretized impulse response. In the limit, with high level thresholding, there is a single bin corresponding to a delay line model of the interconnect.
5) Drivers and receivers are incorporated as behavioral models. From the interconnect impulse response it can be determined if these are instantaneously coupled or not. If they are instantaneously decoupled, which is often the case, then the behavioral models can be solved independently.
6) Calculation reuse is achieved by storing Z_0 and γ of transmission lines and the eigenvalues of the Z_0 and γ matrices of coupled lines.
7) The nodal admittance matrix is stored for discontinuities.

The above techniques have been implemented in a specialized packaging simulator called TRANSIM.

IV. Development of Convolution Method

A distributed network with arbitrary terminations can be partitioned into a linear subcircuit and a nonlinear subcircuit. The linear subcircuit is augmented by series and shunt resistances at each external terminal; they are matched by a complemenatry network, Fig. 2. In combination with packaging parasitics a low-pass filter is produced which naturally frequency limits the admittance response of the augmented network. By choosing the resistance near the characteristic impedance of the network, the response is also time-limited. This can be seen by studying the augmented line shown in Fig. 3.

Following the approach in [40], the effect of the termination network is removed by inserting a complementary network at each port so that a virtual short circuit is created between the load and the transmission network. As shown in Fig. 2, the circuit can then be partitioned into a nonlinear subcircuit, a complementary network, and an augmented linear subcircuit where v_j and i_j are the node voltage and current at port j, v_j' and i_j' are the voltage and current at the port j', and N is the number of external ports of the linear subcircuit. The voltages and currents are related by

$$v_i'(t) = v_i(t) - i_i(t)Z_m \qquad i = 1, N \tag{1}$$

and an estimate of v_i

$$\hat{v}_i(t) = i_i'(t)Z_m \qquad i = 1, N \tag{2}$$

where i_i is the current flowing out of the linear subcircuit at port i, or equivalently, the current flowing into the arbitrary termination at port i and so, in general, is a nonlinear function of v_i.

Now the total transient response of the augmented linear subcircuit to voltage sources at the ports of the network can be determined by convolving in time these voltages with the Dirac impulse voltage responses at each external port of the augmented network. Referring to Fig. 2, the total transient response at port i' of a transmission line system to voltages $v_j(t)$ is

$$i_i'(t) = -\sum_{j=1}^{N} \int_{-\infty}^{t} y_{ij}'(t-\tau) v_j'(\tau)\, d\tau \tag{3}$$

where

$$y_{ij}'(t) = \frac{1}{\Delta t} \boldsymbol{F}^{-1}[Y_{ij}'(\omega)] \tag{4}$$

is the impulse response at port i' and at time t to a Dirac delta source at port j and time zero, i.e., $y_{ij}(t) = i_i'(t)/v_j'(0)$. In (4) $\boldsymbol{F}^{-1}[\,]$ is the inverse Fourier transform and $Y_{ij}'(\omega)$ is the y parameter matrix of the augmented linear subcircuit. That is

$$\boldsymbol{Y}'(\omega) = (\boldsymbol{Y}^{-1}(\omega) + Z_M \boldsymbol{I})^{-1} \frac{1}{-Z_M} \boldsymbol{I}. \tag{5}$$

Finally, Δt is the time increment of $y_{ij}'(t)$ and is one half of the inverse of the maximum frequency component ($f_{\max}$) of $\boldsymbol{Y}'$, i.e. $\Delta t = 0.5/f_{\max}$, and T is the time span of the impulse response. T is equal to the inverse of the frequency increment, Δf, of the y parameters ($T = 1/\Delta f$). The virtual current in (3) can be eliminated by combining this equation with (2) to obtain

$$\hat{v}_i(t) = -Z_M \sum_{j=1}^{N} \int_{-\infty}^{t} y_{ij}'(t-\tau) v_j'(\tau)\, d\tau \tag{6}$$

V. Implementation of Convolution Method

The above algorithm for transmission line network analysis has been implemented in a specialized packaging simulator called TRANSIM. Nonlinear iterations are performed to match the node voltage $\hat{v}_i(n_t)$ given by (6) to the node voltage $v_i(n_t)$ used in (1) for all $\hat{v}$. In discrete, iterative vector form (1) becomes

$${}^k\boldsymbol{V}'(n_t) = {}^k\boldsymbol{V}(n_t) - {}^k\boldsymbol{I}(n_t) Z_M \tag{7}$$

where $\boldsymbol{V}' = [v_1' v_2' \cdots v_N']$, $\boldsymbol{V} = [v_1 v_2 \cdots v_N]$, and $\boldsymbol{I} = [i_1 i_2 \cdots i_N]$. (6) becomes

$${}^k\hat{v}_i(n_t) = Z_M \sum_{j=1}^{N} \left[\sum_{n_\tau=0}^{n_t} y_{ij}'(n_t - n_\tau)\, {}^k v_j'(n_\tau) + \sum_{n_\tau = n_t+1}^{N_T} y_{ij}'(n_\tau)\, {}^k v_j'(0) \right]. \tag{8}$$

That is

$${}^k\hat{\boldsymbol{V}}(n_t) = -\boldsymbol{\Lambda}\, {}^k\boldsymbol{V}'(n_t) - \boldsymbol{\alpha}(n_t). \tag{9}$$

The iterative process is completed by determining ${}^{k+1}\boldsymbol{I}(n_t)$ from ${}^{k+1}\boldsymbol{V}(n_t)$ by evaluating the nonlinear element. In (8) N_T is the number of time points in the period of interest, $t = \Delta t \cdot n_t$, and $\tau = \Delta\tau \cdot n_\tau$. In (9) $\alpha(n_t)$ is a vector with elements

$$\begin{aligned}\alpha_i &= Z_M \sum_{j=1}^{N} \left[\sum_{n_\tau=0}^{n_t-1} y_{ij}'(n_t - n_\tau) v_j'(n_\tau) + \sum_{n_\tau=n_t+1}^{N_T} y_{ij}'(n_\tau) v_j'(0) \right] \\ &= \sum_{j=1}^{N} \left[\sum_{n_\tau=1}^{N_t} g_{ij}(n_\tau)(V_j(n_t - n_\tau) - I_j(n_t - n_\tau) Z_m) \right]\end{aligned} \tag{10}$$

where $v_j'(n)$ is set to $v_j'(0)$ for $n < 0$. Note that α_i does not change from one iteration to the next. $\boldsymbol{\Lambda}$ is a matrix with elements $\lambda_{ij} = Z_M y_{ij}'(0)$. Iteration proceeds by choosing ${}^{k+1}\boldsymbol{V}(n_t)$ to minimize $|\boldsymbol{V}(n_t) - \hat{\boldsymbol{V}}(n_t)|$. That is

$${}^{k+1}\boldsymbol{V}(n_t) = {}^k\boldsymbol{V}(n_t) - \boldsymbol{J}^{-1}({}^k\boldsymbol{V}(n_t) - {}^k\hat{\boldsymbol{V}}(n_t)) \tag{11}$$

where $\boldsymbol{J}$ is the Jacobian of $({}^k\boldsymbol{V}(n_t) - {}^k\hat{\boldsymbol{V}}(n_t))$ with respect to ${}^k\boldsymbol{V}(n_t)$, and has elements

$$\begin{aligned}J_{il} &= \frac{\partial\, {}^k v_i(n_t)}{\partial\, {}^k v_l(n_t)} - \frac{\partial\, {}^k \hat{v}_i(n_t)}{\partial\, {}^k v_l(n_t)} \\ &= a_{il} + Z_M \left[\sum_{\substack{j=1 \\ j \neq l}}^{N} y_{ij}'(0) Z_M \frac{\partial\, {}^k i_j(n_t)}{\partial\, {}^k v_l(n_t)} \right] \\ &\quad -(y_{il}'(0) Z_M - (1 - a_l)) \frac{\partial\, {}^k i_l(n_t)}{\partial\, {}^k v_l(n_t)}.\end{aligned} \tag{12}$$

where $a_{il} = 1$ if $i = 1$ and 0 otherwise. The above considerably simplifies when the external ports are instantaneously uncoupled as is the case when the linear subcircuit is a transmission line network. Then $y_{ij}'(0) = 0$ for $i \neq j$, so that $\boldsymbol{\Lambda}$ is a diagonal matrix [46].

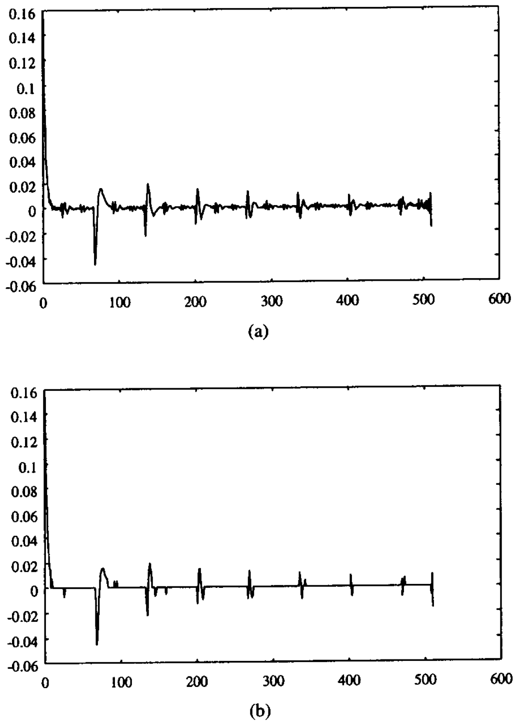


Fig. 4. Example of typical reflection impulse response. (a) With thresholding ($y'_{11}(t)$). (b) Without thresholding ($y_{11}(t)$).

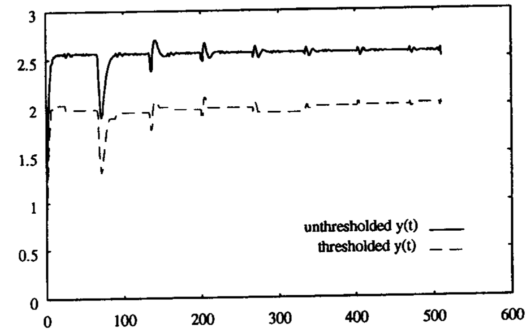


Fig. 5. Unit step convolved with thresholded and unthresholded $y_{11}(t)$ impulse responses.

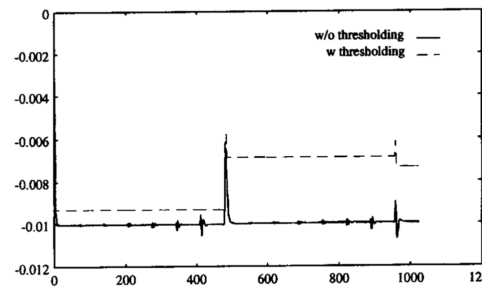


Fig. 6. Unit step convolved with thresholded, $y'_{12}(t)$ and unthresholded, $y_{12}(t)$, impulse response.

VI. Impulse Response Thresholding

One of the drawbacks of convolution techniques has always been the large number of floating point operations used for each time step. For interconnection structures modeled with time domain admittance parameters at least, the form of the transfer function lends itself to some short cuts when it comes to computing the convolution. The results below were obtained for a 20 cm long microstrip line on a substrate with $\epsilon_r = 4.2$ and with 30 Ω terminations. The width, height and thickness of the lines are 2.3 mm, 2 mm, and 0.2 mm respectively. The packaging parasitics are $L = 1$ nH and $C = 1$ pF. A typical time domain response, $y(t)$ (the impulse response) is shown in Fig. 4(a). It is apparent that most of the response hovers around the zero-axis with occasional spikes or impulses. This implies the use of thresholding by keeping those impulse responses with magnitude above a fraction v_r of the peak impulse response magnitude. An example of thresholding is shown in Fig. 4(b). In practice, thresholding can reduce the number of points in the impulse response from several thousand to a few hundred, and for lossy interconnections the number of points can reduce by a greater degree.

A. Errors Introduced by Thresholding

In thresholding the residual aliasing noise in the impulse response is mostly eliminated, but real data is discarded as well. The errors introduced can be significant for large threshold levels. Two techniques were investigated for reducing the errors introduced in this process.

1) DC Normalization: In the DC Normalization error correction method the long term (dc) difference between the response calculated using the original impulse response, $y(t)$, and that calculated using the thresholded reponse, $y'(t)$, is eliminated. When a unit step is convolved with $y_{11}(t)$ (Fig. 4(a)) the output is a transitory shape rising from zero and settling down to some steady-state value—the solid line in Fig. 5. When, however, $y'_{11}(t)$, is used the steady-state response is offset—the dashed line in Fig. 5.

To correct for this long term steady-state error, a correction factor can be applied to all the nonzero terms in $y'(t)$ so that the dc levels match. The correction factor is determined by performing the two convolutions, finding the average error between the two, and subtracting this average error from the nonzero terms of $y'(t)$. Thus, in the long term steady-state, the error is reduced.

2) Short Term Steady-State (STSS) Error Correction: Unfortunately the dc normalization error correction scheme is unable to correct for short term errors, and the addition of the error correction factor to all of the points in the thresholded response distorts the circuit response. The situation is most drammatic when considering the impulse responses corresponding to cross-talk and transmission. These impulse responses related to crosstalk and transmission are characterized as having clusters of impulses separated by regions of low level data. Fig. 6 shows the convolution of $y_{12}(t)$ (the original transmission impulse response) and $y'_{12}(t)$ (thresholded impulse rsponse) with a unit step. Using dc normalization to correct the thresholded impulse responses would lead to

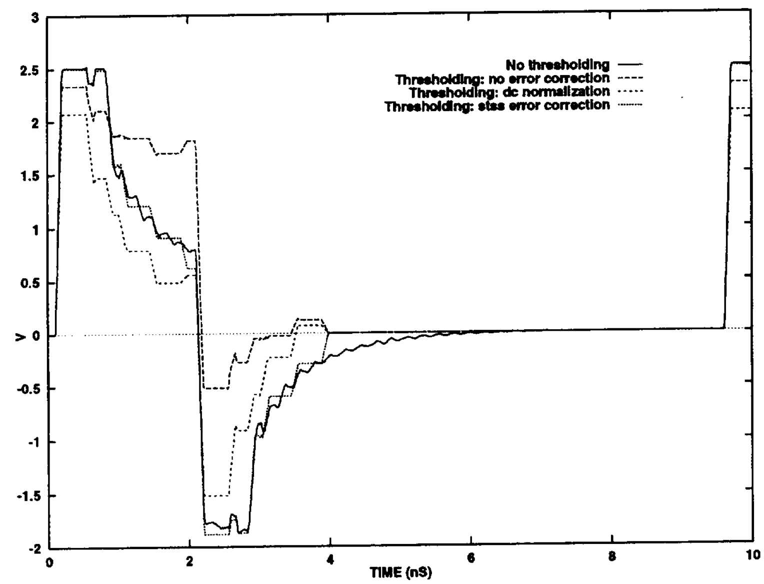


Fig. 7. Comparison of thresholding error correction methods for port 8 of the clock distribution circuit of Fig. 8.

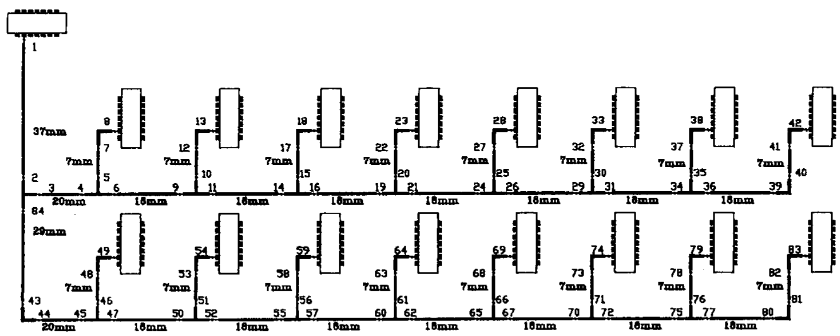


Fig. 8. Clock distribution circuit.

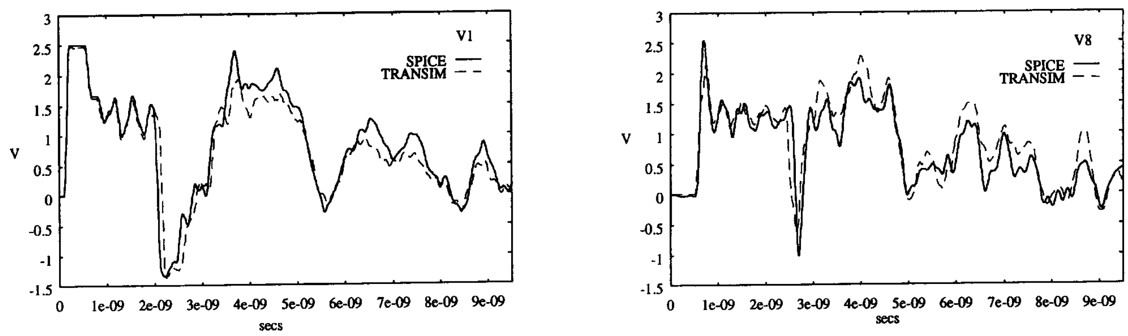
a circuit response which has obvious short term errors. In the STSS error correction method, running sums of $y(t)$ and $y'(t)$ (representing the unit step convolution) are calculated, and the short term errors are eliminated at the end of each cluster of impulses by adjusting the last bin.

An example of the effects of thresholding and the two methods of error correction are shown in Fig. 7 for the clock distribution circuit of Fig. 8. The graph shows the response at one of the loads due to a single pulse at the input to the clock distribution network. While the error introduced by thresholding is reduced by the dc normalization error correction scheme the short term errors are still significant. Errors are almost elminated using the STSS error correction method.

VII. Results and Discussion

Four circuits were considered in demonstrating the method outlined above: a circuit with a single microstrip (as discussed in Section I); three microstrips with bends; a clock distribution circuit; and a data bus circuit. The clock distribution network is shown in Fig. 8, the clock driver (U1) drives a distribution network consisting of two rows of devices. The circuit model has microstrip tee and bend models along with the planar transmission line and nonlinear loads. The output voltages for selected external ports are shown in Fig. 9 (V_1 and V_8) for both the SPICE and TRANSIM simulations. The coupled line example shown in Fig. 10 represents a section of data bus connecting two integrated circuits (represented by the sets of gates). Typical resulting waveforms, used in the analysis below, are illustrated in Fig. 11.

Since there are multiple waveforms resulting from each simulation, the worst case root mean square average case was chosen as being that netlist's error metric. Table I shows the worst case mean square average errors for various netlists. For most netlists the dc normalization method of threshold error correction produced relatively little improvement over having no error correction at all. There was a substantial improvement with the STSS method resulting in error reduction ranging from 38% to 88% with an average improvement of 68%. Thresholding has a drammatic effect on run time with little



(a) (b)

Fig. 9. Waveforms at ports 1 and 8 of the clock distribution circuit.

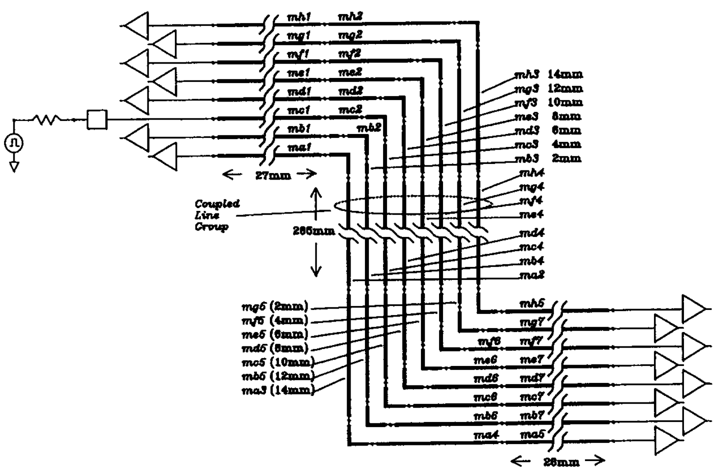


Fig. 10. Data bus.

effect on error provided that error correction is used. Table II shows the effect of varying the threshold parameters on the error and run time for the clock distribution circuit. By increasing the threshold parameter, in this case to 0.25, circuit simulation is reduced by a factor of 10 while introducing an error of about 1%. For a circuit consisting of just the top half of the clock distribution circuit a factor of 30 speed-up was achieved using a thresholding parameter of 0.25; this also lead to an error of around 1%. At high threshold levels the run time becomes dominated by the time to solve, reduce, and then augment the nodal admittance matrix. In the work presented here little attention was given to optimizing the linear circuit analysis time; this was not perceived to be a problem. In the future, modern sparse matrix technqiues, as well as augmenting the circuit during initial modified matrix formulation will be used.

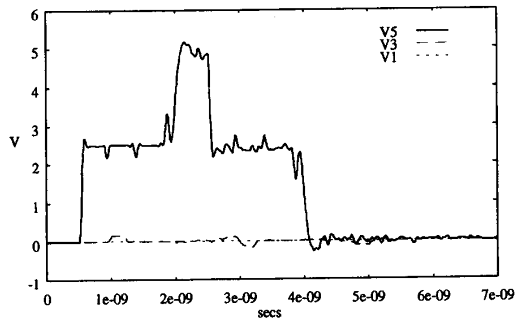
SPICE (both 3E2 and a commercial version) had convergence problems with complicated interconnect circuits with transmission lines. Convergence was eventually obtained after several runs tweaking some parameters (including subtle variations in line lengths). Execution times for various runs are shown in Table III. The three timing information columns show execution speed for SPICE3E2, TRANSIM without thresholding, and TRANSIM with thresholding.

In TRANSIM there are five computationally intensive areas (the percentages in parenthese refer to the times required to simulate the data bus circuit), which are as follows: build the complete nodal admittance matrix (4%); reduce the NAM producing the RNA (38%); augment the RNA with the augmentation network (14%); convert $y(f)$ to $y(t)$ (including STSS error correction) (4%); and perform the transient analysis (40%). The amount of time spent in each of these areas is highly dependent on the circuit being simulated.

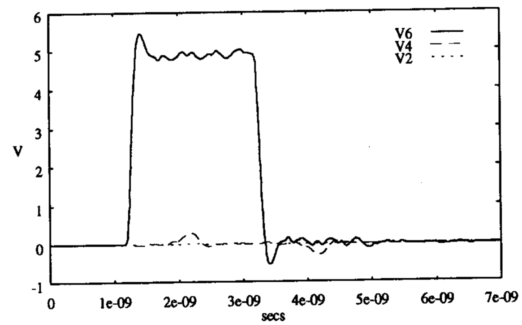
Convolution has proven to be a good method for simulating transmission lines. However, care is required in implementing it in SPICE like simulators to avoid accumulation of numerical error in the period between a transient being applied to the interconnect network and being observed at remote terminals.

VIII. Conclusion

The efficient specialized packaging simulation approach presented here is based on an impulse response/convolution technique. Efficiency is achieved by first developing a reduced



(a)



(b)

Fig. 11. Near (a) and far (b) end bus waveforms showing culprit and victim lines.

TABLE I

PERCENT ROOT MEAN SQUARE ERROR OF CIRCUIT SIMULATIONS USING 0.05 THRESHOLDING WITH DC NORMALIZATION AND STSS THRESHOLD ERROR CORRECTION. THE ERROR IS WITH RESPECT TO SIMULATIONS WITHOUT THRESHOLDING.

Circuit Figure	Description	No Error Correction %	DC Norm. Correction %	STSS Correction %
-	Microstrip	0.377	0.383	0.0233
-	Coupled Microstrip	0.134	0.135	0.0285
-	Microstrip w/bends	0.252	0.236	0.0365
8	Clock Distrib.	0.536	0.271	0.0336
10	Data Bus	19	7.65	4.76

TABLE II

MEAN ERROR AND RUN-TIMES FOR VARIOUS THRESHOLDING LEVELS FOR THE CLOCK DISTRIBUTION CIRCUIT. A THRESHOLDING LEVEL OF 0 CORRESPONDS TO NO THRESHOLDING.

Thresholding Parameter	Run-Time (s)	% Error
0	2169	0.00
0.025	1496	0.01
0.050	1369	0.03
0.075	1026	0.10
0.100	684	0.18
0.150	353	0.50
0.200	307	1.15
0.250	228	1.20

admittance description of the distributed interconnect network keeping only the nodes common to the active circuitry. No limitation is imposed on the frequency domain characteristics of the net except for the practical restraint that the outside

TABLE III

COMPARISON OF EXECUTION TIMES FOR SPICE AND TRANSIM FOR VARIOUS LEVELS OF THRESHOLDING AND ERROR CORRECTION ALGORITHMS. THE RIVERS AND RECEIVERS WERE MODELED AS BEHAVIORAL MODELS IN TRANSIM AND AS LINEAR LOADS IN SPICE 3e2 SINCE THIS TYPE OF NONLINEAR MODEL IS NOT SUPPORTED.

Description	SPICE 3e2	TRANSIM No Threshold	TRANSIM 0.05 Threshold
Single Microstrip	1.8s	16s	3s
Single Microstrip w/bends	86.7s	23s	12s
Clock Distrib.	3637s (60.5min)	2219s (37min)	1369s (23min)

nodes have reactive parasitic to band-limit the response of the network. If the parasitic loading is not present, then they are provided as this is preferred to artificially band-limiting the admittance parameters. Resistive augmentation ensures that the response of the net is also time limited. With both frequency and time limited responses, aliasing errors are virtually eliminated. Thresholding of the impulse response prior to convolution drammatically reduced simulation time and, with a short term steady state error correction scheme, little error is introduced.

Although developed for packaging simulation, the technique is also applicable to on-chip simulation.

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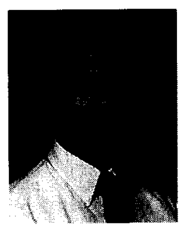

Mark Steven Basel (S'79–M'81) was born January 7, 1959 in East Lansing, Michigan. He received the B.S. degree in electrical engineering from Michigan State University in 1981. He received the M.S. degree in electrical engineering, and the P.h.D. degree in philosophy, both from the North Carolina State University, in 1986 and 1993, respectively.

He worked for the Boeing Aerospace Company in Seattle Washington as a systems analyst in 1981. From 1982 to 1985 he worked at IBM's Fishkill, NY facility, where he worked as a circuit designer involved in designing high speed wafer level integrated circuit test systems. He was admitted to the Doctoral program at North Carolina State University in 1987, and performed research in the area of Computer Aided Design. While writing his dissertation, he began work at Integrated Silicon Systems in Durham North Carolina, where he is currently involved in the development of integrated circuit verification software.

Michael Steer (S'79–M'78–SM'90) received B.E. and Ph.D. degrees from the University of Queensland, Brisbane, Australia, both in electrical engineering, in 1978 and 1983, respectively.

He is Associate Professor of Electrical and Computer Engineering at North Carolina State University. His research involves the simulation, and computer aided design of high speed digital systems; including, interconnect simulation, the behavioral model development of digital drivers and receivers incorporating simultaneous switching noise, the experimental characterization of multichip modules and printed circuit boards, the computer aided analysis and design of nonlinear microwave circuits and systems, parameter extraction using simulated annealing techniques, microwave measurements, and the design of millimeter-wave quasi-optical power combining systems. He has authored or co-authored more than 80 papers on these topics.

Dr. Steer is a senior member of the Institute of Electrical and Electronic Engineers. He is active in the Microwave Theory and Techniques (MTT) Society and the Components, Hybrids, and Manufacturing Technology (CHMT) Society. In the MTT society, he serves on the technical committees on Field Theory and on Computer Aided Design. In the CHMT society, he serves on the technical program committee on simulation and modeling of packaging for the Electronics Components and Technology Conference. In 1987 he was named a Presidential Young Investigator.

Paul Franzon (S'85–M'88), for a photograph and biography, see this issue, p. 58.