A Generic Architecture for Intelligent Networked Colocation in Concurrent Engineering*

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Abstract

As part of the Strategic Manufacturing Initiative, we are engaged in a coordinated interdisciplinary effort to investigate the issues involved in the development of a generic architecture for Intelligent Networked Colocation in Concurrent Engineering. We have identified and developed a generalized form of constraint network, together with companion reasoning methods, as an elegant and powerful technique that can be used as an enabling technology for Concurrent Engineering. We are currently focused on early system decision making, including the critical issues of providing advice to, and mediating negotiation among, the designer/clients of our system. As a proof of concept, a major current application focus is partitioning and placement for multichip modules in electronic design. By investigating application of our generic techniques to this subject area in depth, new methods will be determined that will apply both to this and to other areas of engineering design.

Objective

Concurrent Engineering[2] is an approach to design that takes into account not just the functionality of a product but also such life-cycle issues as manufacturability, testability, maintainability, and the like. Networked Colocation is an attempt to reduce the need for face-to-face meetings among life-cycle team members by using software not only to relieve the logistic and scheduling difficulties but also to reduce the problem complexity perceived by team members. Our long-term research is directed at investigating the issues involved in developing Intelligent Networked Colocation Advisors (INCAs) and of interfacing them to clients, which can be humans or computer-based design agents.

Plan

Our research is aimed at producing a generic INCA architecture which can facilitate effective collaboration among groups of clients. Input to the INCA includes details of decisions, requests for information about the values (or ranges of possible values) for design parameters, requests for justification for these values or ranges, and so on. Output from the INCA to the clients includes answers to the requests, notification about any life-cycle requirements that have been violated, suggestions for overcoming the violations, and the like. Under certain circumstances the set of objects over which constraints can be defined can be dynamically expanded by either a client or the INCA.

Our approach relies on an extremely general notion of a *constraint*. To us, a constraint is *any* declarative statement that restricts the values that may be assumed by a group of one or more parameters. A frame-based constraint is one in which parameters can be either scalars or frames – complex structures that can be organized in an inheritance hierarchy. In contrast to other constraint-oriented approaches to design, our approach is general enough to support componential, as well as parametric, design tasks. Our research is driven by a hypothesis: that networks of frame-based constraints of sufficient expressivity are the right basis on which to develop a generic INCA architecture.

Our INCA applications are written in a declarative frame-and-object-based constraint language known as Galileo4, which — together with its ancestors Galileo1, Galileo2, and Galileo3 — was developed as part of this project.

Current Areas of Investigation

Several issues critical to this enabling technology underlying all INCAs are under active investigation in the current phase of the project. Notably among these, we are addressing the corporate cultural aspects of concurrent engineering through support for negotiated resolution of design conflicts[1, 3, 4], using notions of economic utility theory. Also, we have now begun to use genetic algorithms as part of our method for both constraint solving and advice generation[5, 6, 7].

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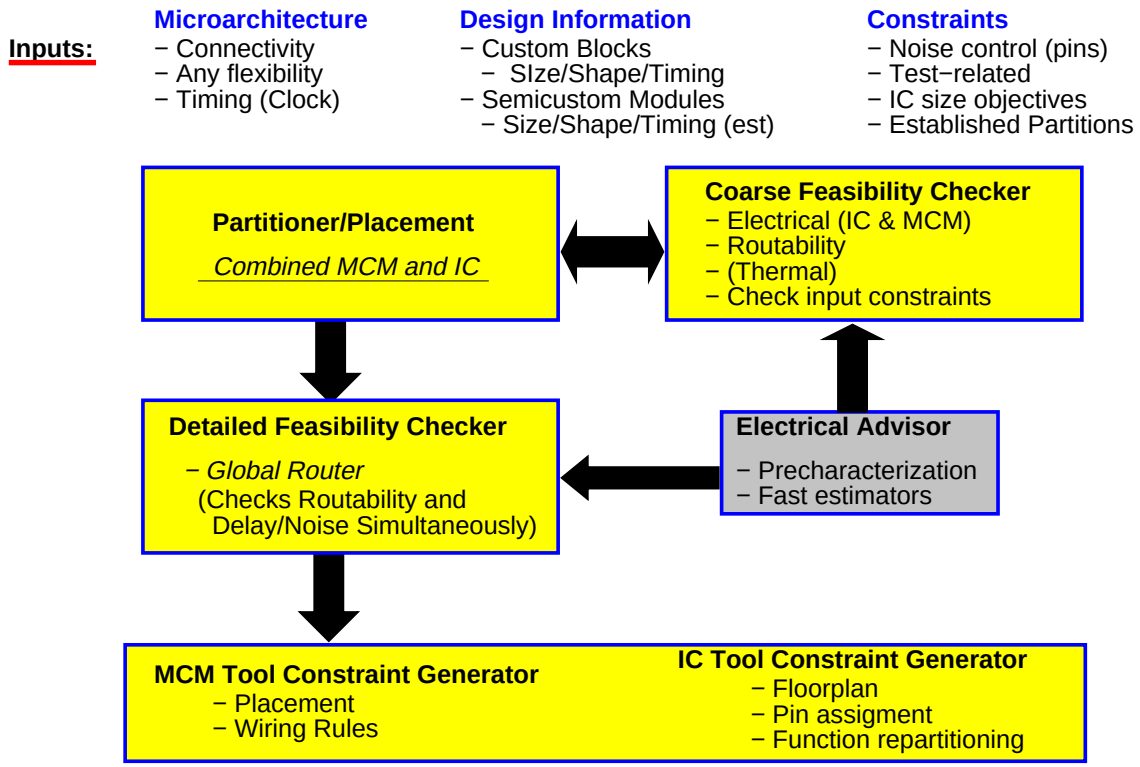

Figure 1: CAD Tool Flow.

0.1 CoDesign of Packages and ICs

In a high speed electronic system, the printed circuit board (PCB) or multichip module (MCM), the package, and the integrated circuit (IC) must all be designed concurrently [8]. In this section, we present two projects that are working towards this end:

1. Tools for combined partitioning, floor-planning, and pin-assignment for custom and semi-custom ICs on a multichip module.

2. Tools for co-synthesis of logic and interconnect.

The status of these two tools are described in turn.

0.2 Combined Partitioning and Floorplanning

The CAD flow is given in Figure 1. The objective of this tool is to determine partitioning, floorplanning, and pin assignment so that manufacturing-related feasibility constraints are optimized. It targets high performance multichip module technology. Particular emphasis is given to maximizing timing-related constraints and routability. Accurate electrical and routing estimators are used towards this goal. The output of the tool is a set of constraints for the follow-on IC and MCM design tools.

0.3 Co-Synthesis of Logic and Interconnect

In a new-start project, we are investigating the automatic co-synthesis of logic and packaging. The key is to adjust the scheduling phase of the synthesis to account for the effects of interconnect.

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